Single Step-up DC/DC Controller

Features

- **2.5 to 5.5V Input Voltage Range**
- **Adjustable Frequency: Maximum 1MHZ**
- **Incorporates Soft-Start Function**
- **Built-in Short-Circuit Detection Circuit (SCP)**
- **Low Operating Current: Maximum to 1mA**
- **Low Shutdown Current: Maximum to 1㎂**
- **Package: SOP-8, MSOP-8, TDFN2x2-8 and TSSOP-8**
- **Under-Voltage Lockout**
- **Lead Free and Green Devices Available (RoHS Compliant)**

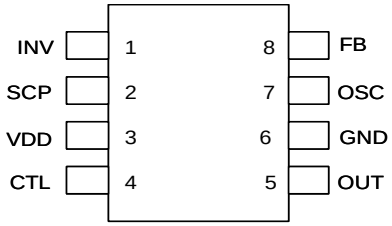
Applications

- **LCD Display Power Source**
- **Camcorders VCRs, MP3, and Digital Still Camera**
- **Hand-held and Communication Instruments**
- **PDAs**

General Description

The APW7078 is a single PWM, step-up DC-DC controller with low operating voltage application integrating soft-start and short circuit detection function. The oscillator switching frequency on chip can be operated by terminating OSC pin to connect capacitor and resistor for adjustable operating frequency. Soft-start is adjusted with the external capacitor, which sets the input current ramp. Besides, the external compensation FB pin will apply the flexibility in the dynamic loop status, which allows using small and low equivalent series resistance (ESR) ceramic output capacitors.

Pin Configuration



Ordering and Marking Information

APW7078 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-8 X : MSOP-8 O : TSSOP-8 QB : TDFN2x2-8 Temperature Range I : -40 to 85 C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7078 K : APW7078 XXXXX	XXXXX - Date Code
APW7078 X : W7078 XXX XX	XXXXX - Date Code
APW7078 O : APW7078 XXXXX	XXXXX - Date Code
APW7078 QB : 7078 • X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 7	V
V_{IO}	Input / Output Pins	-0.3 to 7	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Junction Temperature Range	-40 to 150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply Voltage	2.5	-	5.5	V
V_{INV}	Error Amplifier Invert Input Voltage	-0.2	-	1	V

Recommended Operating Conditions (Cont.)

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
V_{CTL}	Control Pin Input Voltage	-0.2	-	V_{DD}	V
C_{SCP}	SCP Pin Capacitor	-	0.1	-	µF
R_T	Timing Resistance	1.0	3.3	10	kΩ
C_T	Timing Capacitor	100	-	270	pF
F_{SW}	Oscillator Frequency	200	600	1000	kHz

Electrical Characteristics

(T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified)

Symbol	Parameter	Test Conditions	APW7078			Unit
			Min.	Typ.	Max.	
ENTIRE DEVICE						
V_{DD}	Supply Voltage		2.5	-	5.5	V
I_{DD}	Supply Current	V_{DD}=2.5V to 5.5V	-	0.7	1	mA
I_{SD}	Shutdown Current	CTL pin open or VDD	-	0.1	1	µA
D_{MAX}	Maximum Duty Cycle	R_T =3.3K, C_T =270pF	80	85	92	%
UNDER-VOLTAGE LOCKOUT PROTECTION						
V_{TH}	VDD Startup Threshold Voltage	-	2.0	-	2.4	V
V_R	Hysteresis voltage		-	150	-	mV
SOFT-START						
V_{SS}	Voltage at Soft-Start Completion	-	0.7	0.8	0.9	V
I_{CS}	Soft-Start Charge Current	V_{SCP} =0V	-0.7	-1.0	-1.5	µA
V_{SS}	Voltage at Soft-Start Completion	-	0.7	0.8	0.9	V
I_{CS}	Soft-Start Charge Current	V_{SCP} =0V	-0.7	-1.0	-1.5	µA
SHORT CIRCUIT PROTECTION (SCP)						
V_{SCP}	Threshold Voltage		0.7	0.8	0.9	V
I_{SCP}	Charge Current	V_{SCP} =0V	-0.7	-1.0	-1.5	µA
SAWTOOTH WAVEFORM OSCILLATOR (OSC)						
F_{OSC}	Oscillator Frequency	R_T =3.3kΩ, C_T =270pF	500	600	700	kHz
F_{DV}	Frequency Stability for Voltage	V_{DD}=2.5V to 5.5V	-	2	5	%
F_{DT}	Frequency Stability for Temperature	T_A=-40°C to 85°C	-	5	-	%

Electrical Characteristics (Cont.)

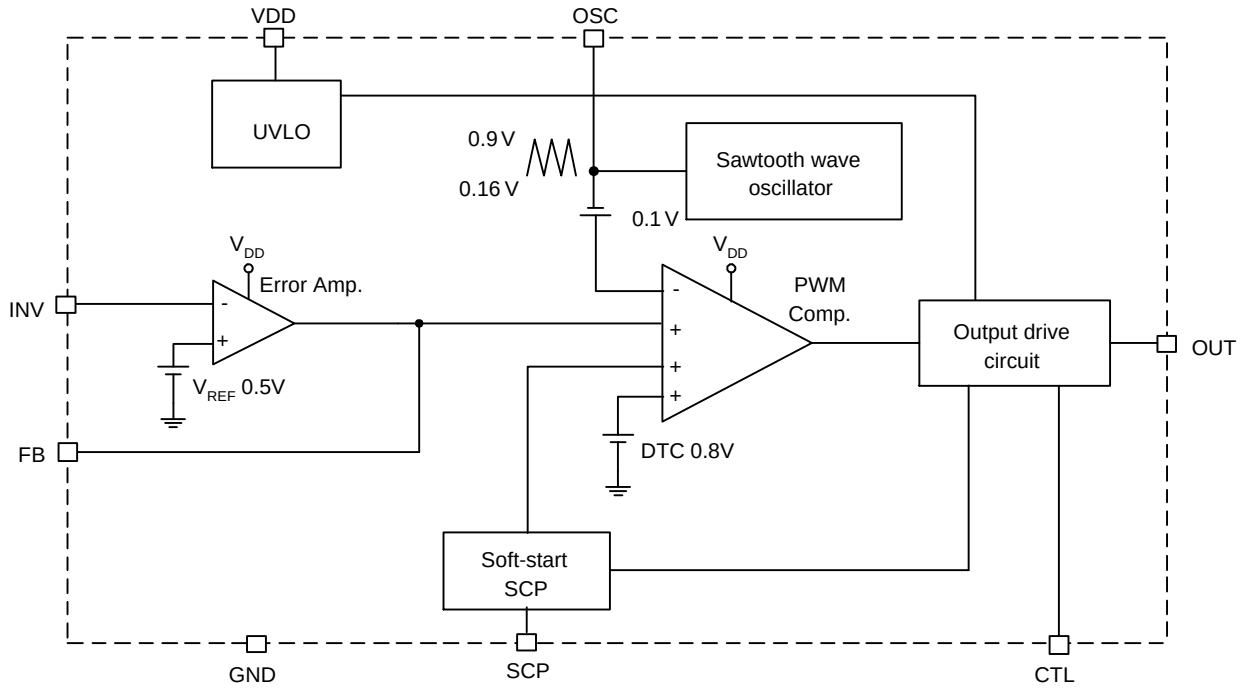
(T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified)

Symbol	Parameter	Test Conditions	APW7078			Unit
			Min.	Typ.	Max.	
ERROR AMPLIFIER						
V_{REF}	Reference Voltage	V_{FB}=INV	0.493	0.5	0.508	V
	V_{REF} Stability	V_{DD}=2.5V to 5.5V	-	5	20	mV
	V_{REF} Variation with Temperature	T_A =-40°C to 85°C	-	1	-	%
gm	Transconductance		1000	1300	1600	µA/V
I_B	Input Bias Current	INV=0V	-	-	1	µA
V_{OH}	Output Voltage Range	-	1.6	1.8	-	V
V_{OL}		-	-	-	0.01	V
	Output Source Current	INV=0V,FB=0.5V	-150	-180	-210	µA
	Output Sink Current	INV=1V,FB=0.5V	140	170	200	µA
PWM CONTROLLER DRIVER						
I_{SOURCE}	Output Source Current	Duty<5%, OUT=0V	-150	-200	-	mA
I_{SINK}	Output Sink Current	Duty>5%, OUT=5V	150	200	-	mA
CONTROL BLOCK						
V_{IL}	Control Voltage	Active mode	-	-	$0.2V_{DD}$	
V_{IH}		Switch-off mode	$0.8V_{DD}$	-	-	

Pin Description

PIN NO.	SYMBOL	I/O	FUNCTION
1	INV	I	Internal 0.5V reference voltage. Use a resistor divider to set the output voltage.
2	SCP	-	Soft-start and short-circuit detection, connects a capacitor from the pin to ground.
3	VDD	-	Power supply input pin for IC voltage.
4	CTL	I	Output control pin. Low = operating mode; High = shutdown mode.
5	OUT	O	External MOSFET driving pin.
6	GND	-	Ground pins of the IC.
7	OSC	-	Setting capacitor and resister to provide oscillation switching frequency adjustment.
8	FB	O	Error amplifier output pin. Setting circuit for IC compensation.
Exposde Pad	GND	-	Connect this pad to GND (pin6).

Block Diagram



Application Schematic

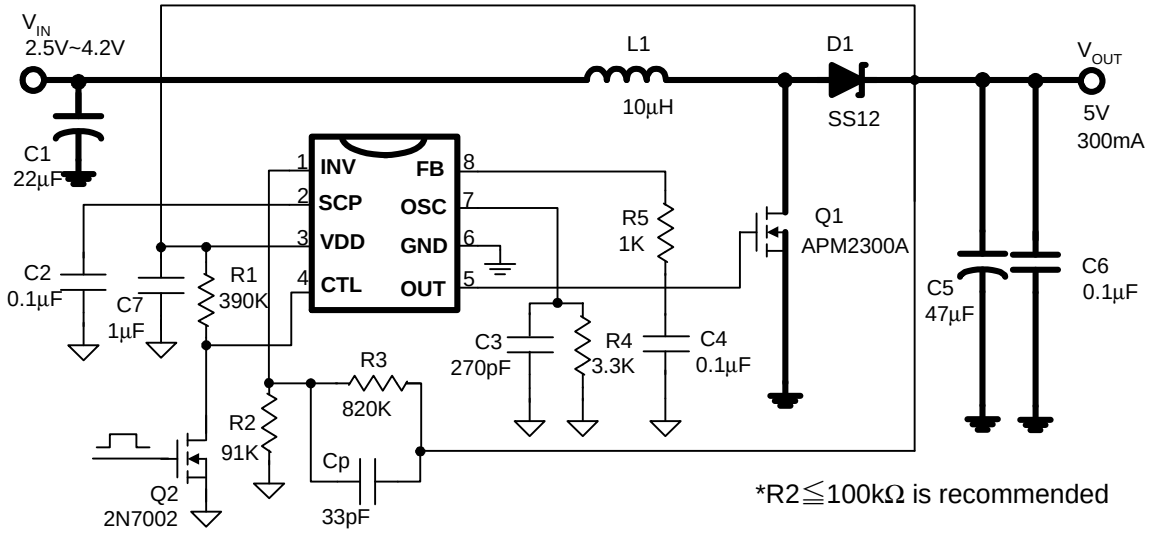


Figure 1: APW7078 Step-up Application for Adjustable Voltage

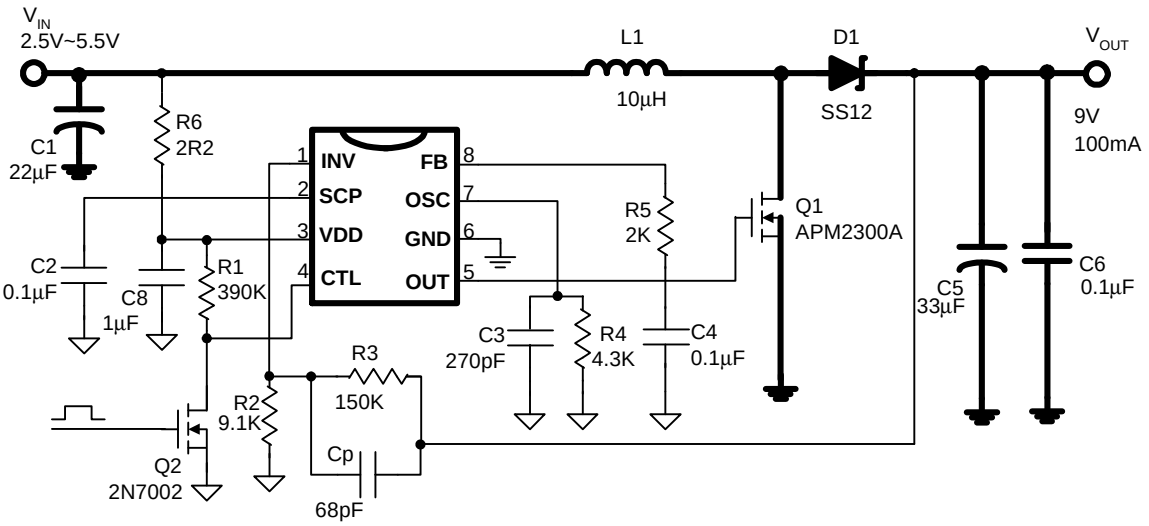


Figure 2: APW7078 Step-up Application for Adjustable Voltage

Application Schematic

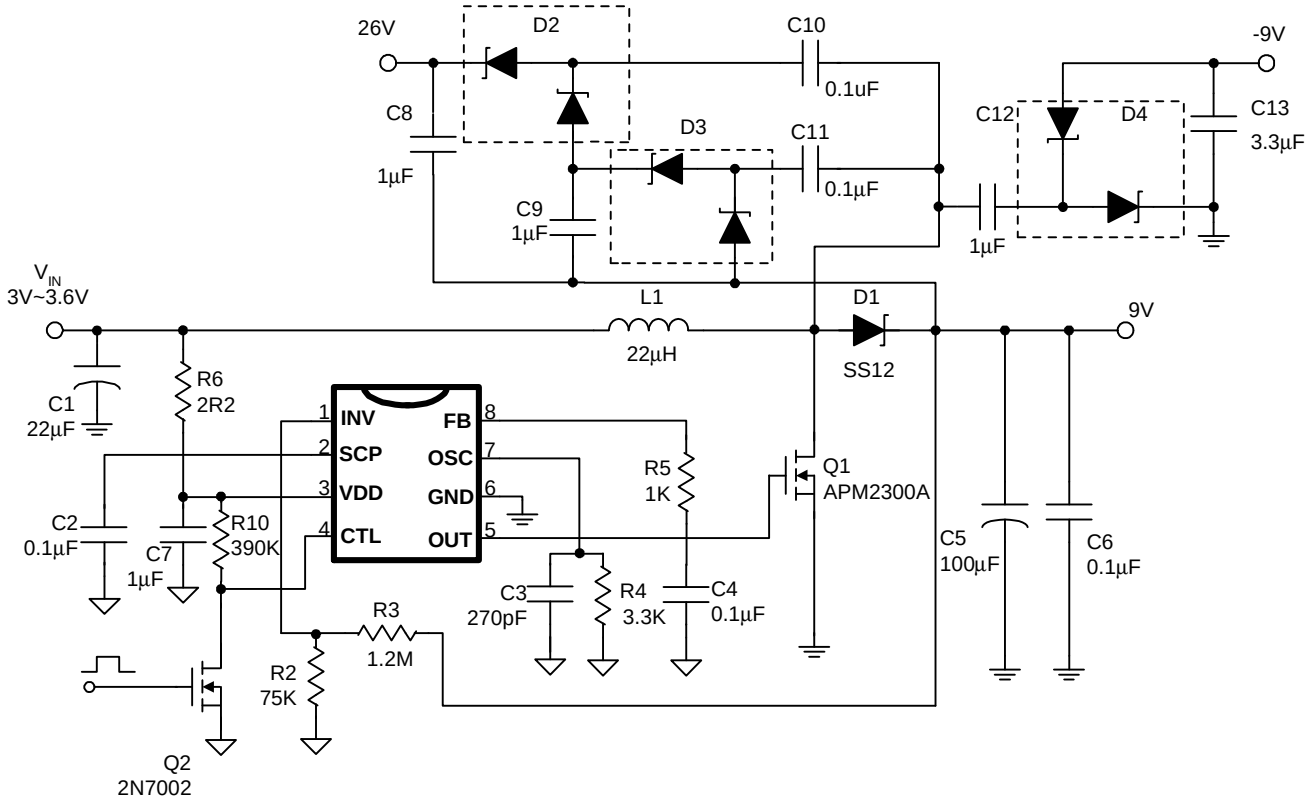
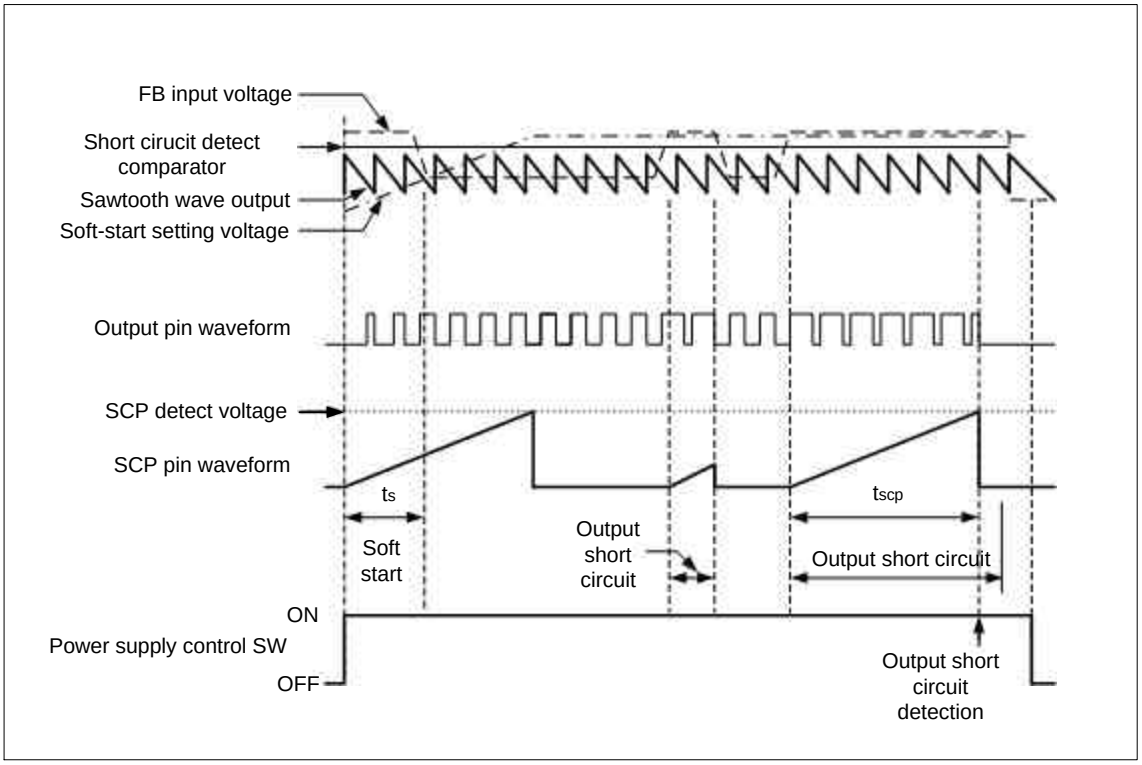


Figure 3. APW7078 Multiple-output for TFT LCD Panel Power

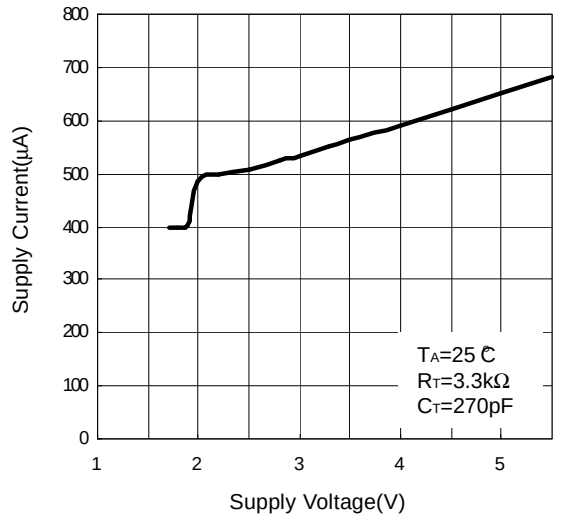
Timing Diagram



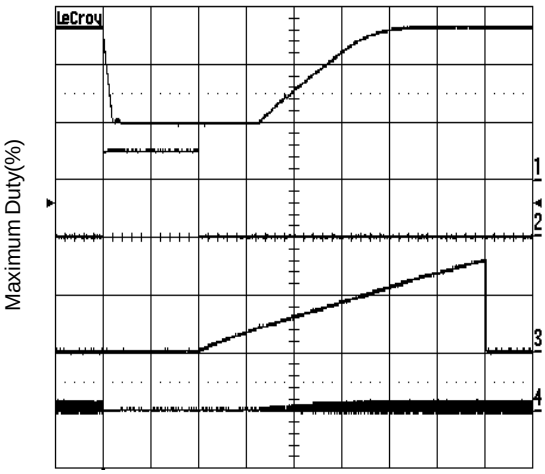
Typical Operating Characteristics

(T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified)

Supply Current vs. Supply Voltage

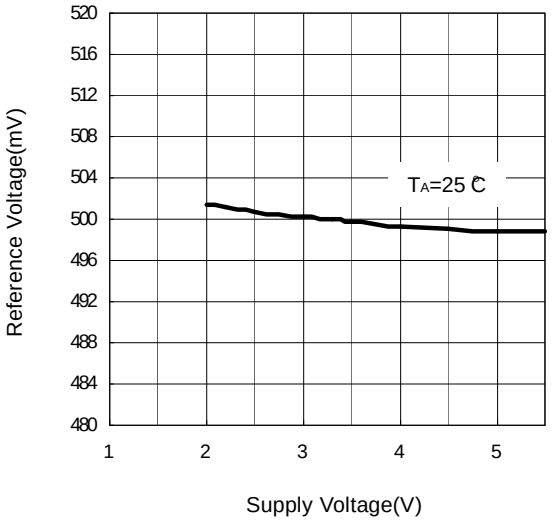


SHDN and Release

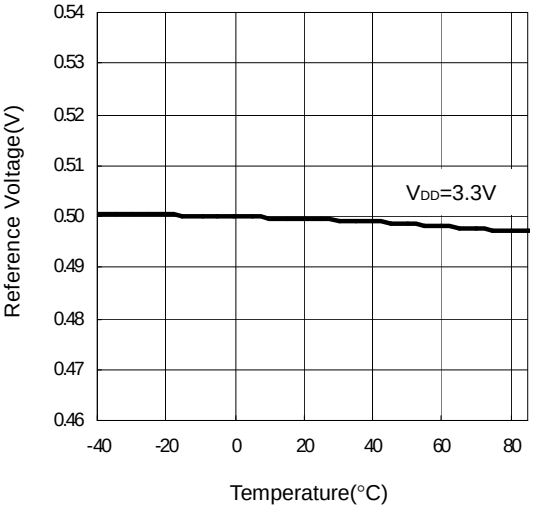


CH1=V_{OUT} 2V/DIV TIME=20ms/DIV
CH2=V_{CTL} 2V/DIV
CH3=V_{SS} 0.5V/DIV
CH4=I_L 1A/DIV

Reference Voltage vs. Supply Voltage



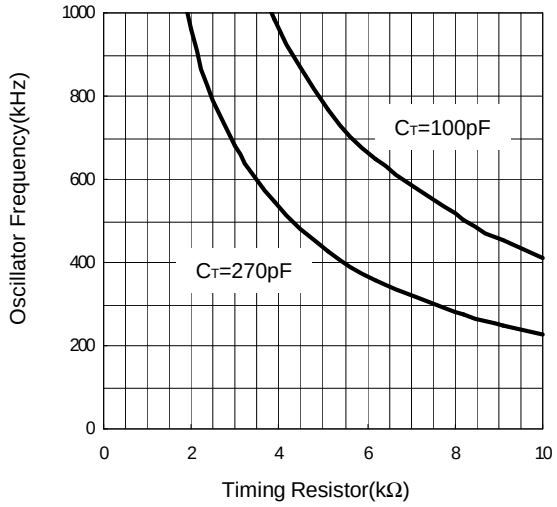
Reference Voltage vs. Temperature



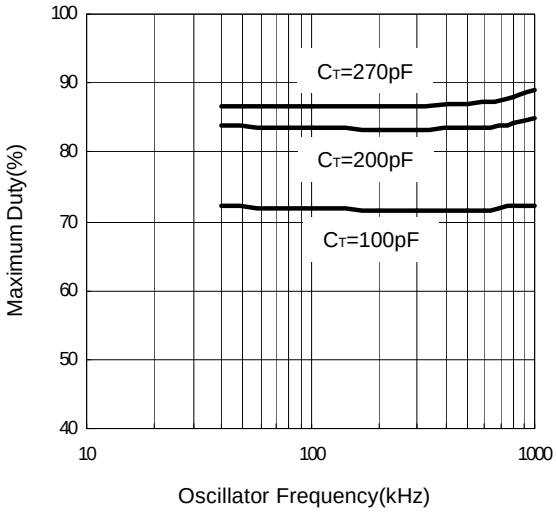
Typical Operating Characteristics (Cont.)

(T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified)

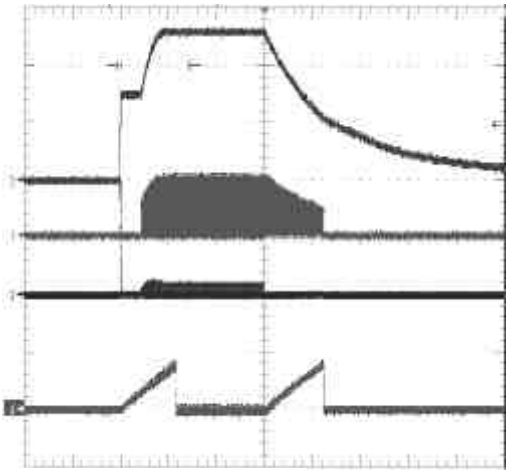
Oscillator Frequency vs. Timing Resistor



Maximum Duty vs. Oscillator Frequency

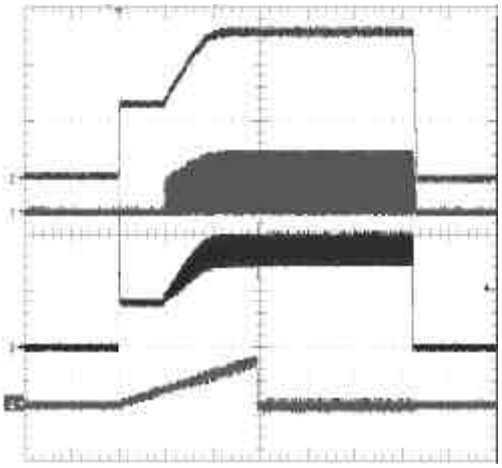


Power on and off under light load



I_{OUT}= 5mA, TIME=40ms/DIV
CH1=V_{OUT} 5VDIV
CH2=V_{OUT}=V_{DD} 2V/DIV
CH3=I_L 0.5A/DIV
CH4=V_{SS} 1V/DIV

Power on and off under heavy load

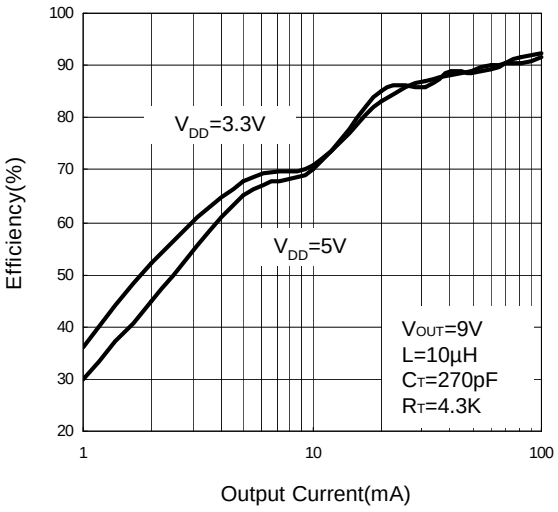


I_{OUT}= 400mA, TIME=40ms/DIV
CH1=V_{OUT} 5VDIV
CH2=V_{OUT}=V_{DD} 2V/DIV
CH3=I_L 0.5A/DIV
CH4=V_{SS} 1V/DIV

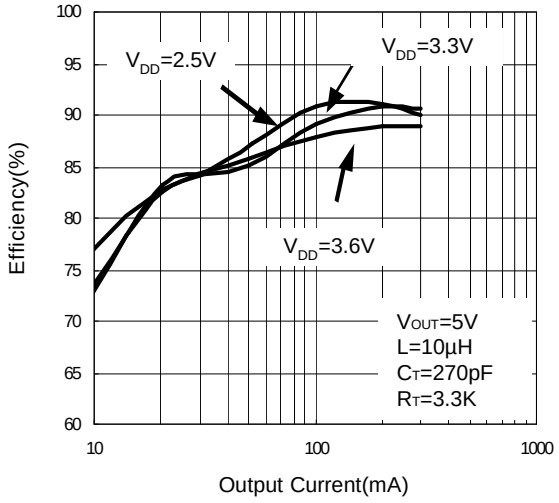
Typical Operating Characteristics (Cont.)

(T_A = 25°C, V_{DD} = 3.3V, unless otherwise specified)

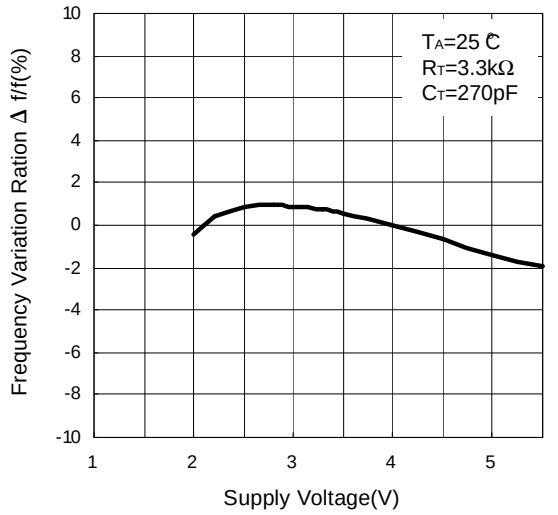
Efficiency



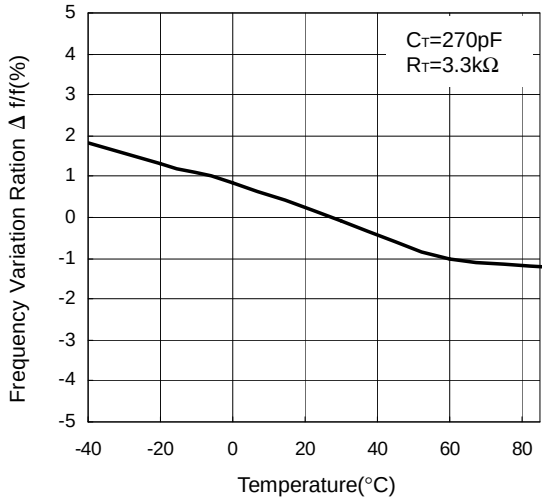
Efficiency



Frequency Variation Ratio vs. Supply Voltage



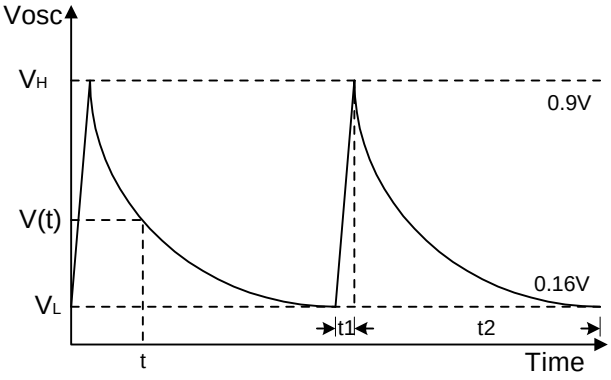
Frequency Variation Ratio vs. Temperature



Function Description

Setting Oscillating Frequency

The oscillator circuit generates a triangular sawtooth wave with a peak of 0.9V and through 0.16V using the timing capacitor (C_T) and the timing resistor (R_T) that are connected to OSC pin. This oscillator can provide oscillating frequency up to 1MHz.



$$i = c\frac{\Delta V}{\Delta t}$$

$$t_1 = C_T \cdot \frac{0.9V - 0.16V}{2mA} = 370 \cdot C_T$$

$$V(t) = V_H \cdot e^{-\frac{t}{R_T C_T}}$$

$$t_2 = R_T C_T \ln(V_H / V_L) = 1.72 \cdot R_T C_T$$

$$T = t_1 + t_2 = C_T(370 + 1.72R_T)$$

Setting Output Voltage

The output voltage is set using the INV pin and a resistor divider connected to the output is shown in the Typical Operating Circuit. The internal reference voltage is 0.5V with 2% variation, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$V_{OUT} = \left(1 + \frac{R3}{R2}\right) \times 0.5V$$

To avoid the thermal noise from feedback resistor, the resistance R2 is smaller than 100kΩ and 1% variation is recommended.

Error Amplifier

The error amplifier detects the output voltage of the switching regulator and outputs the PWM control signal. The voltage gain is fixed, and connecting a phase compensation resistor and capacitor to the FB pin (pin 8) provides stable phase compensation for the system.

PWM Comparator

The voltage comparator has one inverting and three non-inverting inputs. The comparator is a voltage/pulse width converter that controls the ON time of the output pulse depending on the input voltage. The output level is high (H) when the sawtooth wave is lower than the error amplifier output voltage, soft-start setting voltage, and idle period setting voltage.

Output Circuit

The output circuit is a typical push-pull configuration to drive an external NMOS transistor directly. It can provide a 200mA source/sink to/from OUT (pin 5).

Soft-Start and Short Circuit Detection

Soft-start operation is set by connecting capacitor C_{SCP} to the SCP pin (pin 2). Soft-start prevents a current spike on start-up. On completion of the soft-start operation, the SCP pin (pin 2) stays low and enters the short circuit detection wait state.When an output short circuit occurs, the error amplifier output is fixed at 1.8V and capacitor C_{SCP} starts charging.

After charging to approximately 0.8 V, the output pin (pin 5) is set low and the SCP pin stays low. Once the protection circuit operates, the circuit can be restored by resetting the power supply. Short circuit detection time can be calculate as below:

$$t_{SCP} = 0.8 \times C_{SCP}(\mu F)$$

Under-Voltage Lock Out (UVLO)

Transients during powering on or instantaneous glitches in the supply voltage can cause system damage or failure. The circuit prevents malfunction at low input voltage detects a low input voltage by comparing the supply voltage with the internal reference voltage. On detection, the circuit fixes the output pin to low. The system recovers when the supply voltage rises back above the threshold voltage of the malfunction prevention circuit.

Function Description (Cont.)

Layout Consideration

Switching Noise Decoupling Capacitor

A 0.1µF ceramic capacitor should be placed close to the VOUT pin and the GND pin of the chip to filter the switching spikes in the output voltage monitored by the VOUT pin.

Feedback Network

In APW7078 application, the feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the GND pin. If no analog ground plane is available, and then this ground must tie directly to the GND pin. The feedback network, resistors R2 and R3, should be kept close to the FB pin, and away from the inductor.

Input Capacitor

The input capacitor CIN in VIN must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 1µF capacitor can be placed in parallel with C_{IN}, close to the VDD pin, to shunt any high frequency noise to the ground.

Demo Board Circuit Layout

Inductor

To minimize copper trace connections that can inject noise into the system, the inductor, switch, and schottky diode should be placed as close as possible to minimize the noise coupling into other circuits.

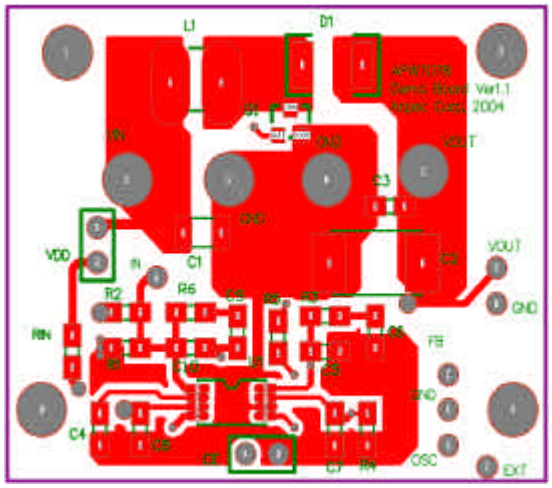
Output Capacitor

The output capacitor, C_{OUT}, should be placed close to the diode and output terminals to obtain better smoothing effect on the output ripple. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency.

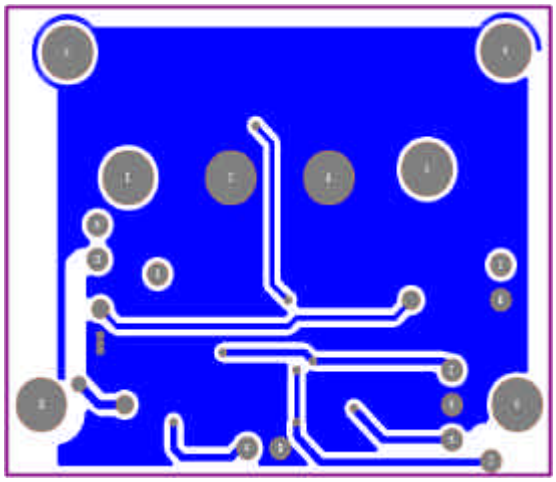
Ground Plane

One point grounding should be used for the output power return ground, the input power return to the ground and the device switches the ground to reduce noise. The input ground and output ground traces must be thick enough for current to flow through and for reducing the ground bounce.

Top Layer

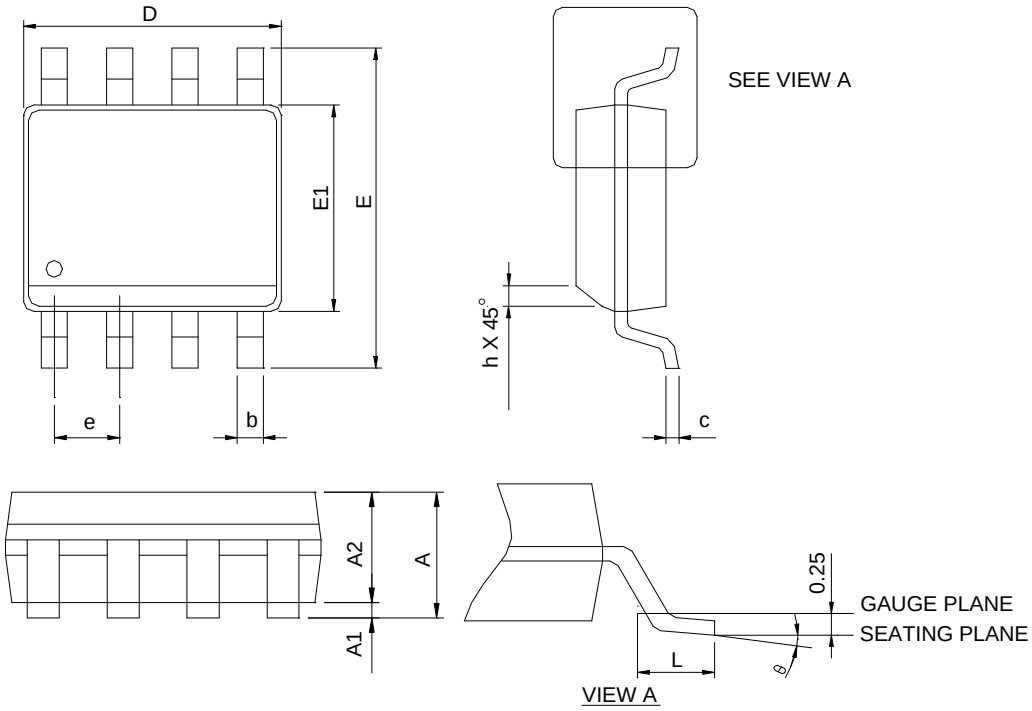


Bottom Layer



Package Information

SOP-8

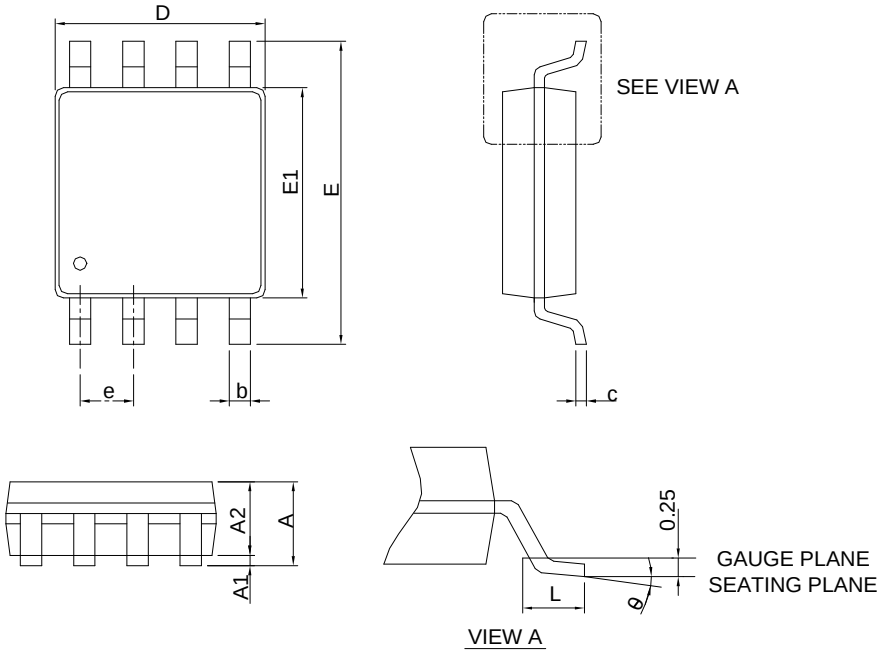


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

MSOP-8

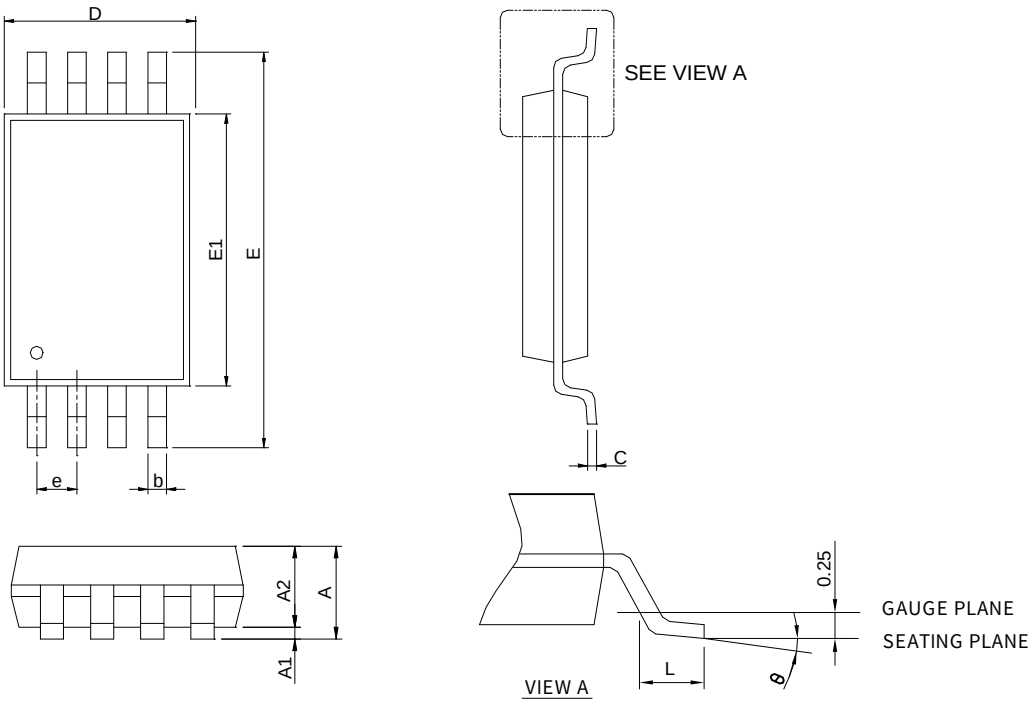


SYMBOL	MSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA.
2. Dimension " D " does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension " E1 " does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 5 mil per side.

Package Information

TSSOP-8

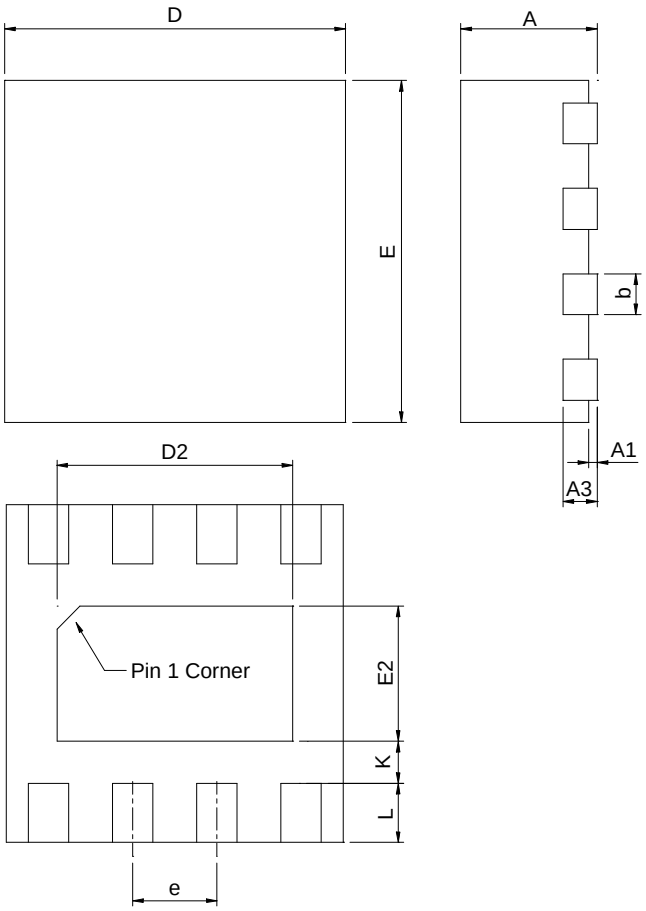


SYMBOL	TSSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0 °	8 °	0 °	8°

Note : 1. Follow JEDEC MO-153 AA
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

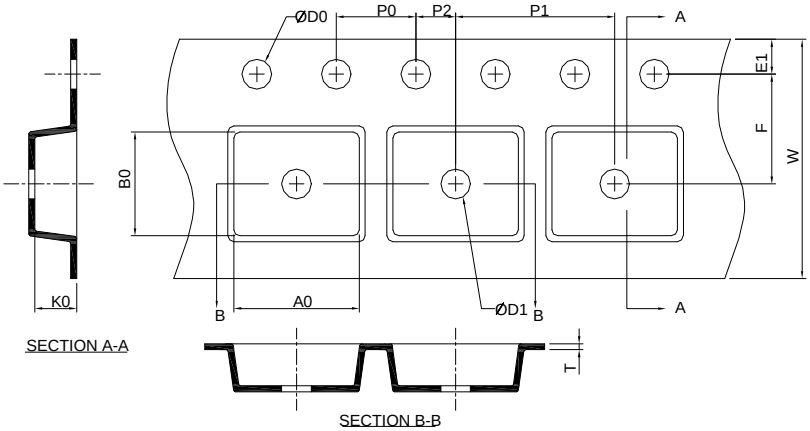
TDFN2x2-8

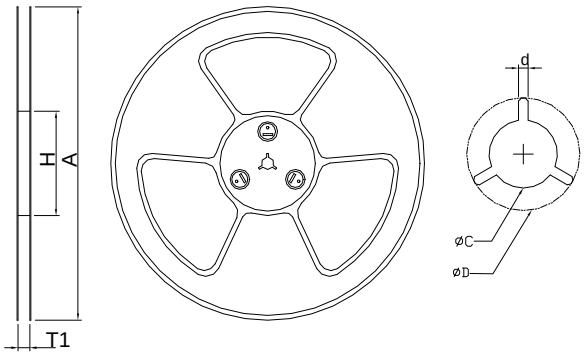


SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	A	H	T1	C	d	D	W	E1	F
MSOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.90±0.20	3.40±0.20	1.60±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20

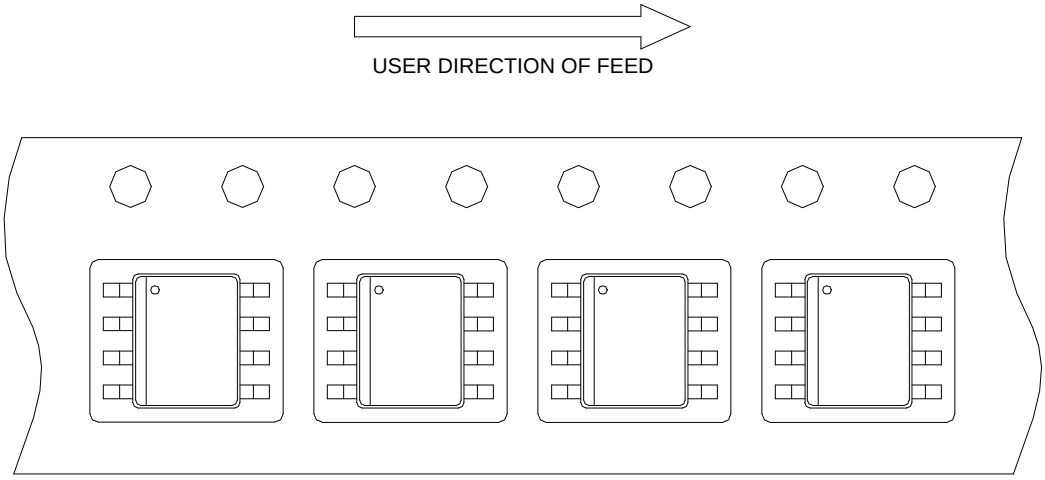
(mm)

Devices Per Unit

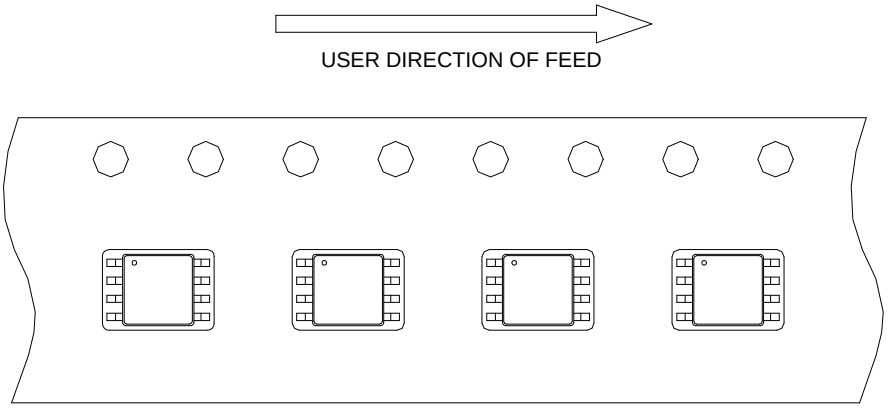
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
MSOP- 8	Tape & Reel	3000
TDFN2x2-8	Tape & Reel	3000
TSSOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8

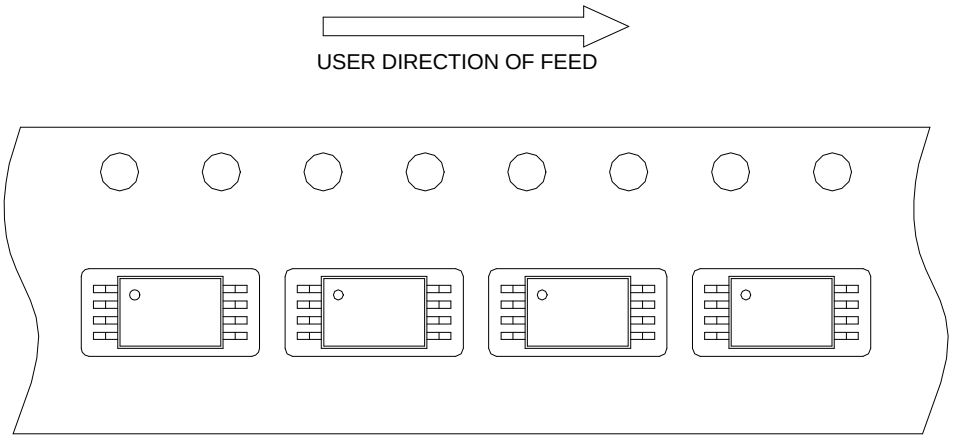


MSOP-8

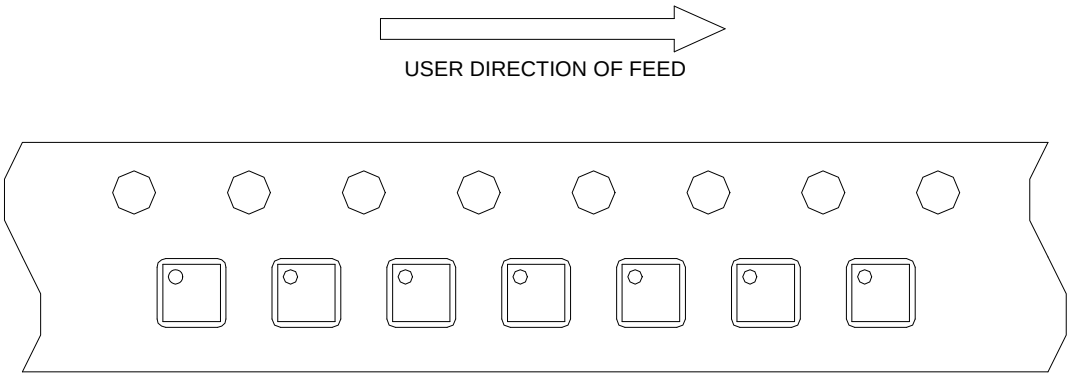


Taping Direction Information

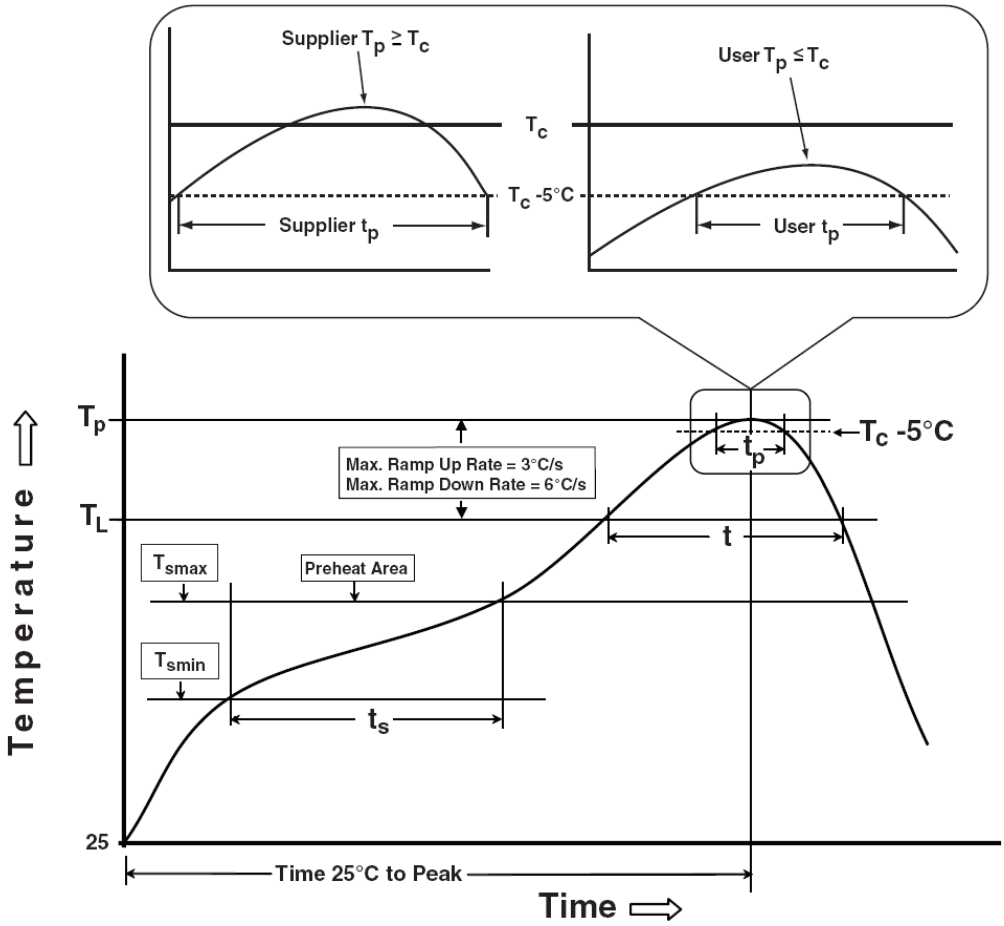
TSSOP-8



TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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