

Step-Up Converter and LDO Combo

Features

- Built-In a 500mA LDO and Synchronous Step-Up DC-DC Converter
- Built-In PWM/PFM Operating Mode
- Provided Dual Input Power Sources
- Connect FB to OUT for 3.3V Output Voltage or GND for 2.5V Output Voltage or an External Resistor Divider for Adjustable Output Voltage.
- Fixed 300kHz Operating Frequency
- High Efficiency Up to 94% at 200mA Output Current
- 0.6V to 4.5V Operating Voltage
- 1V Start-Up Input Voltage
- Low Battery Voltage Detection
- Reverse Voltage Protection
- Internal Synchronous Rectifier
- Automatic Detection Input Voltage
- Compact SOP-8P and TSSOP-8 Packages
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Dual Mode Power System
- USB Peripheral
- Camcorders and Digital Camera
- Hand-Held Instrument
- PDAs

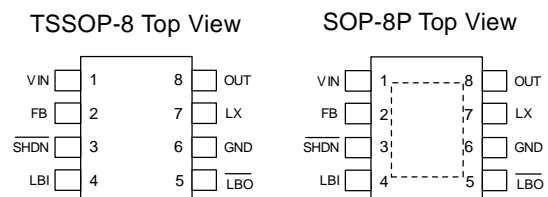
General Description


The APW7075 is a PWM/PFM, high-efficiency, and step-up DC-DC converter with an integrated LDO input switch for dual mode application. During battery mode operation, the APW7075 acts as synchronous rectifier and step-up DC-DC converter with a fixed or adjustable output voltage. When the VIN pin sense 5V input voltage, the APW7075 is switched to LDO operation mode, maintaining the constant output voltage.

The input voltage ranges from 0.6 V to 4.5V for step-up DC-DC converter. The start-up is guaranteed at 1V and the device operates down to 0.6V. When the device is at LDO operating mode, the suitable output voltage 3.3V and loading current 500mA for maximum power consumption are guaranteed.

The APW7075 is suited for dual mode and portable battery powered appliance with low-battery detector. In dual-mode applications, the APW7075 draws power from any available 5V USB connection and reverts to battery power when the USB power is removed.

Pin Configuration



 = Thermal Pad
(connected to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

| | | |
|--|--|------------------|
| <p>APW7075 □□□-□□□</p> <div style="margin-left: 40px;"> <p>└─ Assembly Material</p> <p>└─ Handling Code</p> <p>└─ Temperature Range</p> <p>└─ Package Code</p> </div> | <p>Package Code KA : SOP-8P O : TSSOP-8</p> <p>Temperature Range C : 0 to 70°C I : -40°C to 85°C</p> <p>Handling Code TR : Tape & Reel</p> <p>Assembly Material L : Lead Free Device G : Halogen and Lead Free Device</p> | |
| APW7075 KA : | <table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;">APW7075 XXXXX</td> </tr> </table> XXXXX - Date Code | APW7075 XXXXX |
| APW7075 XXXXX | | |
| APW7075 O : | <table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;">APW7075 XXXXX</td> </tr> </table> XXXXX - Date Code | APW7075 XXXXX |
| APW7075 XXXXX | | |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|------------------|-------------------------------------|-------------|------|
| V _{OUT} | Supply Voltage (OUT to GND) | -0.3 to 6.0 | V |
| V _{IO} | Input / Output Pins | -0.3 to 6.0 | V |
| T _A | Operating Ambient Temperature Range | 0 to 85 | °C |
| T _J | Junction Temperature Range | 0 to 150 | °C |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _S | Soldering Temperature, 10 Seconds | 260 | °C |

Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|------------------|--|---------------|------|
| R _{θJA} | Thermal Resistance – Junction to Ambient | | °C/W |
| | SOP-8 | 124 | |
| | SOP-8-P | 80 | |
| | TSSOP-8 | 160 | |

Electrical Characteristics

$V_{BAT} = 2V$, $FB = OUT$ ($V_{OUT} = 3.3V$), $R_L = \infty$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.

| Symbol | Parameter | Test Conditions | APW7075 | | | Unit |
|------------------------|--|--|---------|------|-------|----------|
| | | | Min. | Typ. | Max. | |
| STEP-UP SECTION | | | | | | |
| V_{BAT} | Minimum Operating Input Voltage (Note1) | | 0.6 | - | - | V |
| | Operating Voltage | | 0.6 | - | 4.5 | V |
| | Start-up Voltage | $R_L = 3k\Omega$ | - | 0.9 | 1 | V |
| F_{SW} | Operating Frequency | $V_{OUT} = 3.3V \times 96\%$ | - | 300 | - | kHz |
| D_{MAX} | Maximum PWM Duty Cycle | $V_{OUT} = 3.3V \times 96\%$ | - | 90 | - | % |
| POWER MOSFET | | | | | | |
| $R_{DS(on)-N}$ | Active Switch ON Resistance | $I_{LX} = 100mA$ | - | 0.3 | 0.6 | Ω |
| $R_{DS(ON)-P}$ | Synchronous Switch on Resistance | $I_{LX} = 100mA$ | - | 0.6 | 0.9 | Ω |
| CONTROL | | | | | | |
| V_{OUT} | Output Voltage | $FB = OUT, I_{LOAD} = 0mA$ | 3.234 | 3.3 | 3.366 | V |
| | | $FB = GND, I_{LOAD} = 0mA$ | 2.45 | 2.5 | 2.55 | V |
| | Output Voltage Range | External divider | 2.5 | - | 5.5 | V |
| $V_{OUT(drop)}$ | V_{OUT} Dropping Voltage (Note 2) | $V_{OUT} = 3.3V, C_{OUT} = 100\mu F$ | - | - | 150 | mV |
| T_{SS} | Soft-Start Time | $V_{OUT} = 3.3V$ | - | 30 | 100 | ms |
| V_{REF} | FB Input Threshold | $I_{LOAD} = 0mA$ | 1.176 | 1.2 | 1.224 | V |
| I_{FB} | FB Input Current | $V_{FB} = 1.4V$ | - | 0.03 | 50 | nA |
| | Operating Current (Note3) | $V_{OUT} = 3.3V \times 96\%, I_{LOAD} = 0mA$ | - | 70 | 140 | μA |
| | | | | | | |
| | Shutdown Current | $V_{SHDN} = 0$ | - | 0.1 | 5 | μA |
| I_{SHDN} | SHDN Input Current | $V_{SHDN} = 0$ or V_{OUT} | - | 0.07 | 50 | nA |
| \overline{SHDN} | Logic LOW (V_{IL}) | | - | 0.8 | 0.3 | V |
| | Logic HIGH (V_{IH}) | | 1.4 | 0.8 | - | V |
| | LBI Input Hysteresis | | - | 10 | - | mV |
| V_{LBI} | LBI Threshold | | 0.588 | 0.6 | 0.612 | V |
| I_{LBI} | LBI Input Current | $V_{LBI} = 0.8V$ | - | 1 | 50 | nA |
| $V_{\overline{LBO}}$ | \overline{LBO} Logic Low | $V_{LBI} = 0, I_{SINK} = 1mA$ | - | 0.2 | 0.4 | V |
| $I_{\overline{LBO}}$ | \overline{LBO} Off Leakage Current | $V_{LBO} = 5.5V, V_{LBI} = 5.5V$ | - | 0.07 | 1 | μA |

Electrical Characteristics (Cont.)

Unless otherwise noted these specifications apply over full temperature, $3.9V \leq V_{IN} < 5.5V$, $C_{OUT} \geq 10\mu F$, $\overline{SHDN} = V_{IN}$, Typical values are at $T_A = +25^\circ C$.)

| Symbol | Parameter | Test Conditions | APW7075 | | | Unit |
|-----------------------------|----------------------------------|--|-------------|-----------|-------------|---------|
| | | | Min. | Typ. | Max. | |
| LDO SECTION (Note 4) | | | | | | |
| $V_{IN(upper)}$ | Upper V_{IN} Threshold Voltage | V_{IN} increasing | 3.75 | 3.9 | 4.05 | V |
| $V_{IN(lower)}$ | Lower V_{IN} Threshold Voltage | V_{IN} decreasing | 3.65 | 3.8 | 3.95 | V |
| V_{TH} | V_{IN} Threshold Hysteresis | | - | 100 | - | mV |
| V_{OUT} | Output Voltage | | $V_{OUT}-2$ | V_{OUT} | $V_{OUT}+2$ | V |
| I_{LIM} | Current Limit | $V_{IN} = 5V$ | - | 1 | - | A |
| I_{SHORT} | Short Current | $V_{OUT} = 0V$ | - | 110 | - | mA |
| I_{OUT} | Load Current | | 500 | - | - | mA |
| V_{DROP} | Dropout Voltage | $I_{LOAD} = 500mA$ | - | 0.6 | 0.9 | V |
| I_q | Quiescent Current | No load | - | 800 | 1000 | μA |
| | | $I_{LOAD} = 500mA$ | - | 1.1 | 1.5 | mA |
| REG_{LINE} | Line Regulation | $4V < V_{IN} < 5.5V$, $I_{LOAD} = 0mA$ | - | 4 | 10 | mV |
| REG_{LOAD} | Load Regulation | $V_{IN} = 5V$, $0mA < I_{LOAD} < 500mA$ | - | 20 | 30 | mV |

Note1: The min. operating voltage is dependent on the duty cycle.

Note2: The dropped output voltage is that the input power (V_{IN} pin) is switched to battery power (LX pin), when the V_{IN} power is removed.

Note3: Device is bootstrapped (power to the IC comes from OUT). This correlates directly with the actual battery supply.

Note4: If the LDO mode is used, the output voltage should be under 3.8V.

Function Pin Description

VIN (Pin 1)

Input supply voltage for dual-mode application. Connect a schokkty diode (current rating >500mA) to USB port or 5V adapter. If the LDO mode is not used, ties the VIN pin to the ground.

FB (pin 2)

Internal 1.2V reference voltage. Connect to OUT for 3.3V output. Connect to the GND for 2.5V output. Use a resistor divider to set the output voltage from 2.5V to 5.5V.

SHDN (pin 3)

Shutdown input. High = operating mode; Low = shutdown mode.

LBI (Pin 4)

Low-battery comparator input. Internally set to trip at 0.6V.

LBO (pin 5)

Open-drain low battery comparator output. Connect $\overline{\text{LBO}}$ to OUT through a 100k Ω resistor. Output is low as $V_{\text{LBI}} < 0.6\text{V}$. Open-drain device is turned on during shutdown.

OUT (pin 8)

Power output. OUT provides bootstrap power to the IC.

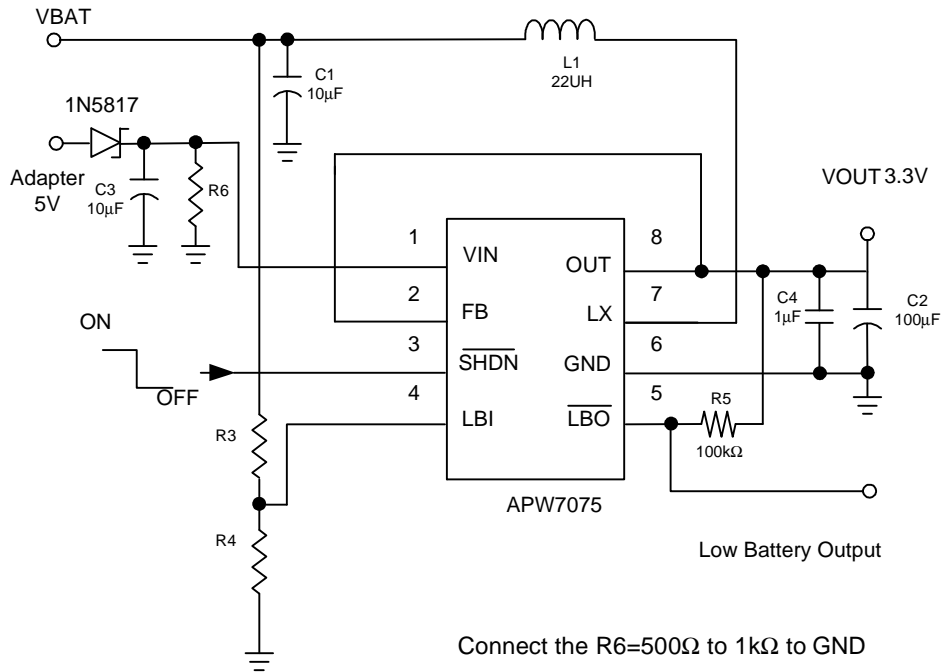
GND (Pin 6)

Ground pins of the circuitry and all ground pins must be soldered to PCB with proper power dissipation.

LX (pin 7)

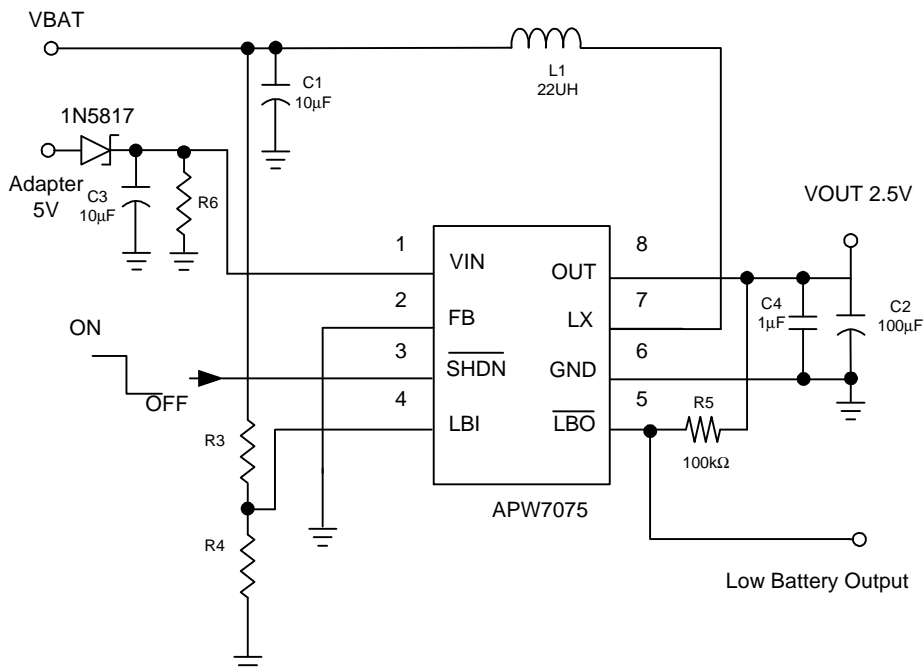
N-channel and P-channel power MOSFET drain connection.

Application Schematic



Connect the R6=500Ω to 1kΩ to GND

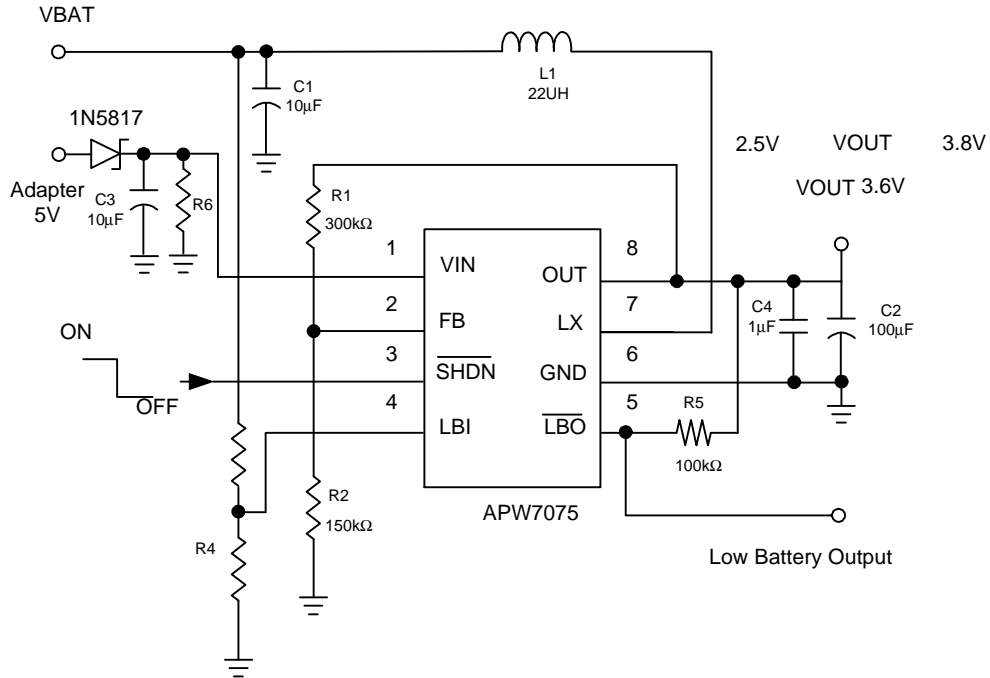
Figure 1. Dual Model : 3.3V Output Voltage



Connect the R6=500Ω to 1kΩ to GND

Figure 2. Dual Model : 2.5V Output Voltage

Application Schematic (Cont.)



Connect the R6=500Ω to 1kΩ to GND

Figure 3. Dual Model: Adjustable Output Voltage

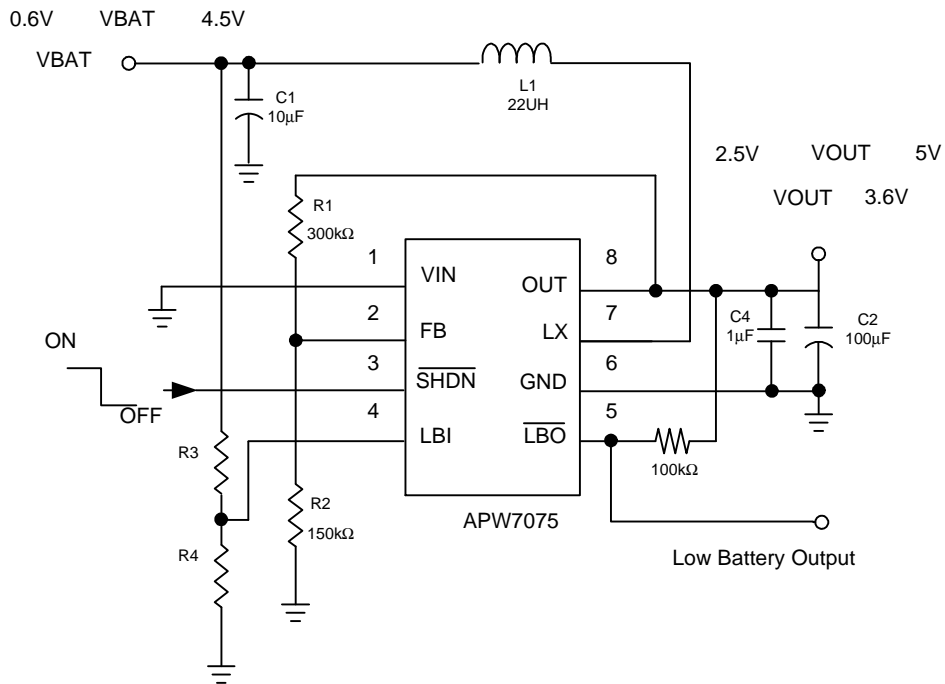
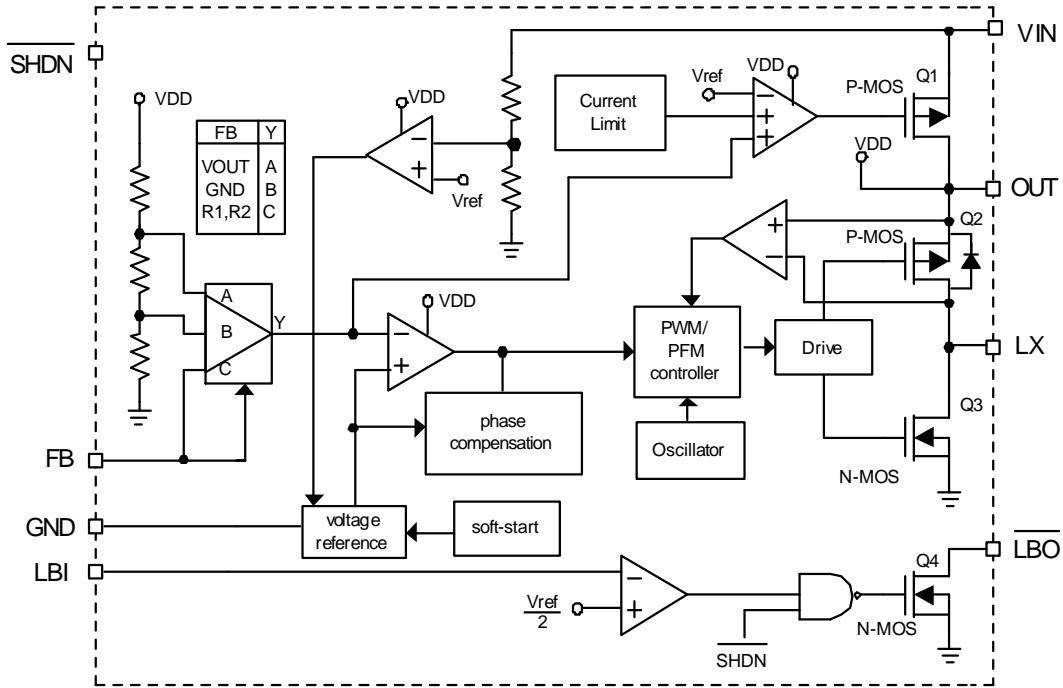
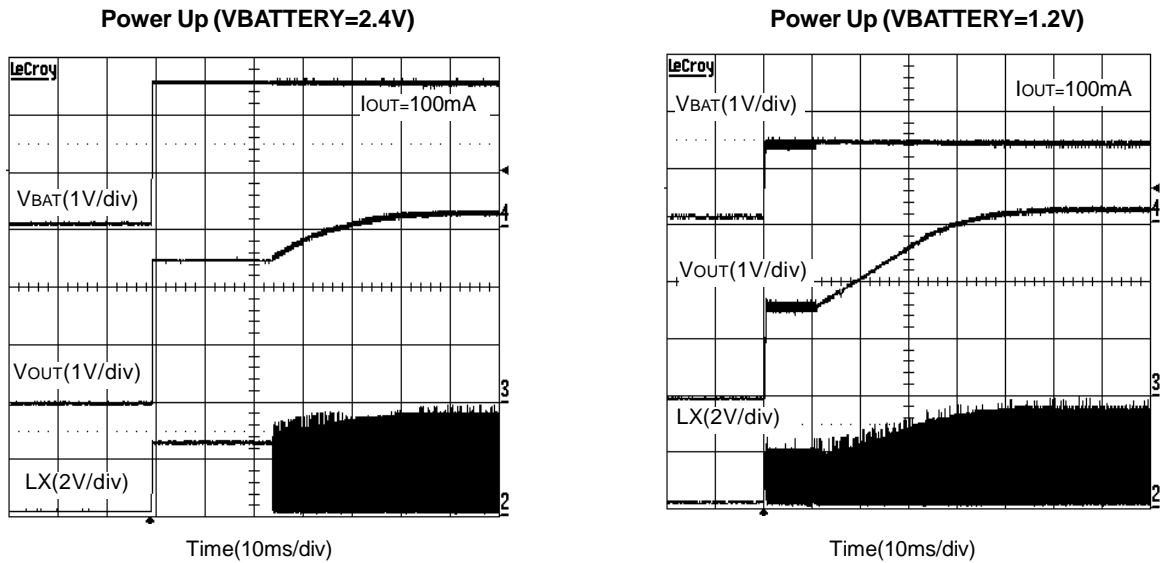


Figure 4. Single Boost Converter

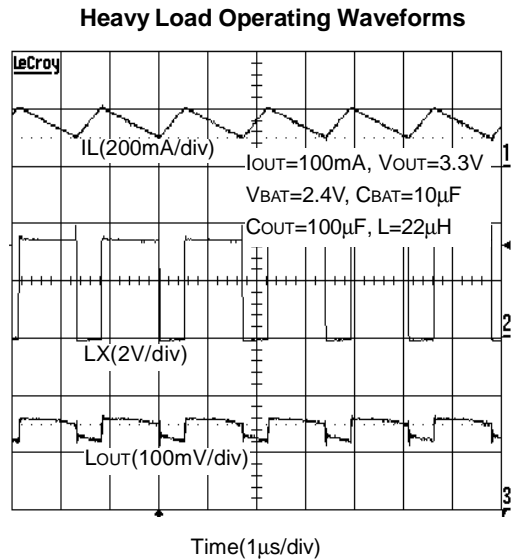
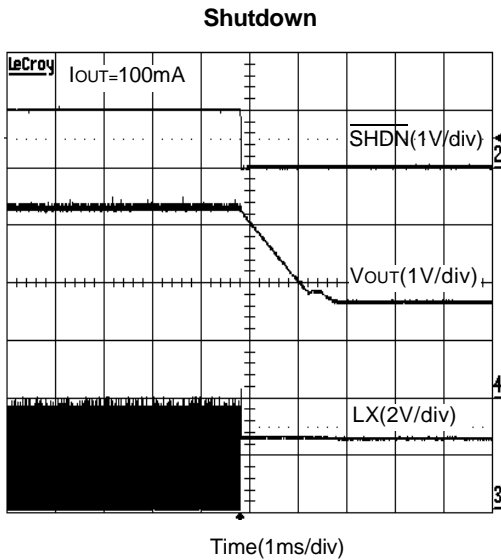
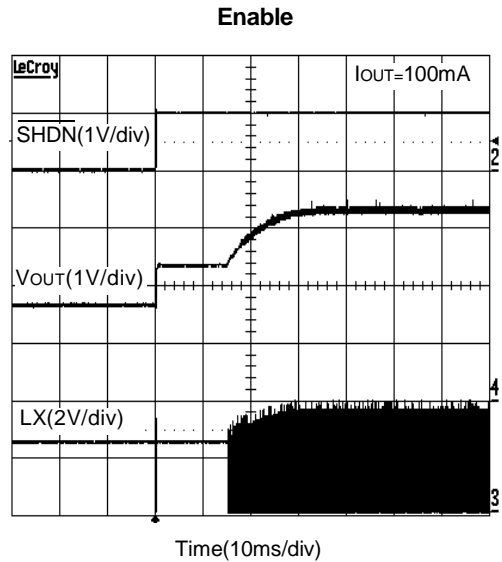
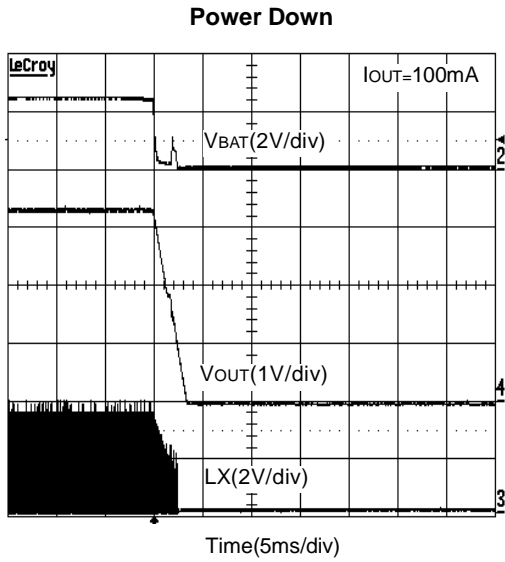
Block Diagram



Typical Operating Characteristics

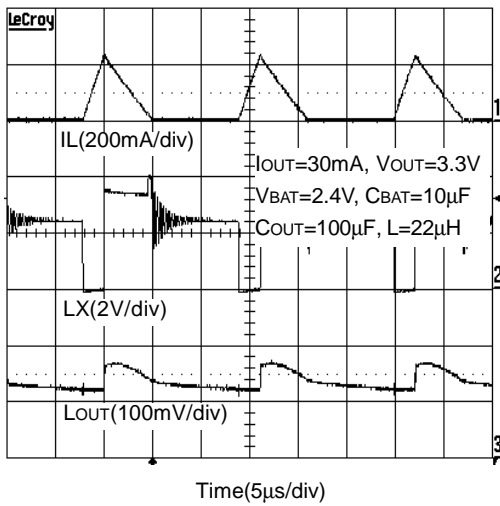


Typical Operating Characteristics (Cont.)

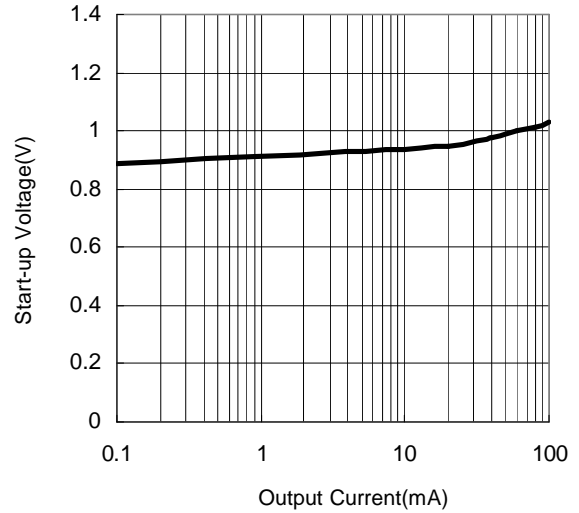


Typical Operating Characteristics (Cont.)

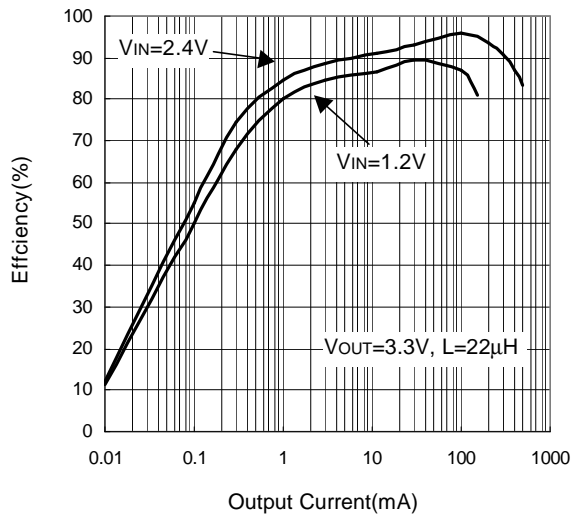
Light Load Operating Waveforms



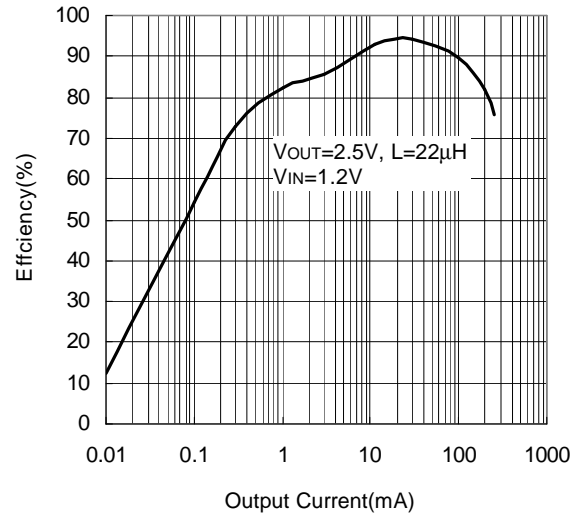
Output Current vs. Start-up Voltage



Efficiency vs. Output Current

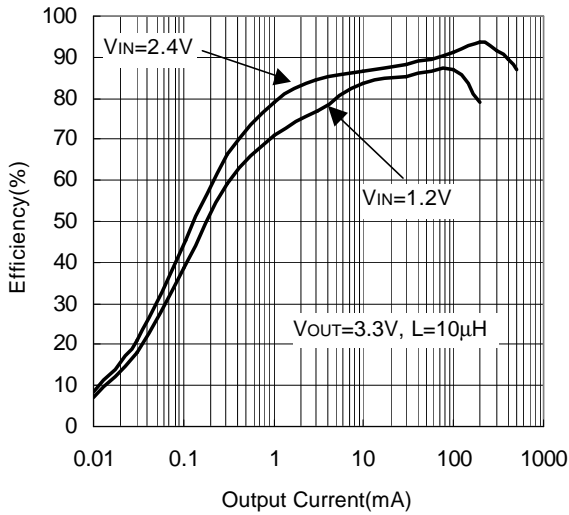


Efficiency vs. Output Current

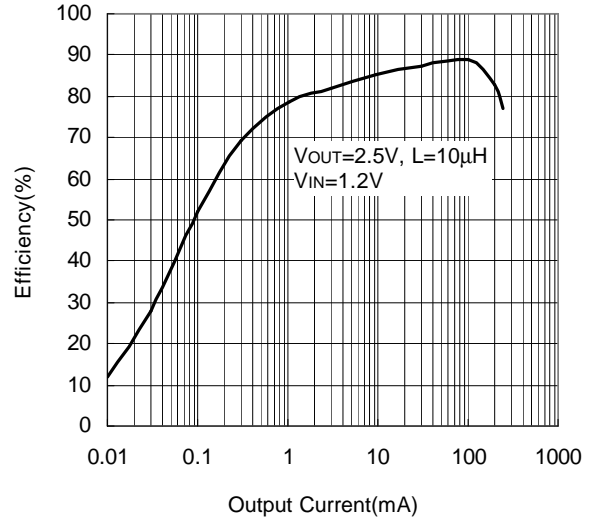


Typical Operating Characteristics (Cont.)

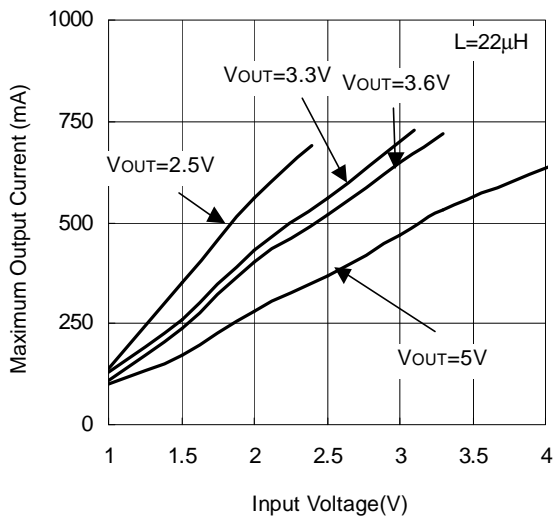
Efficiency vs. Output Current



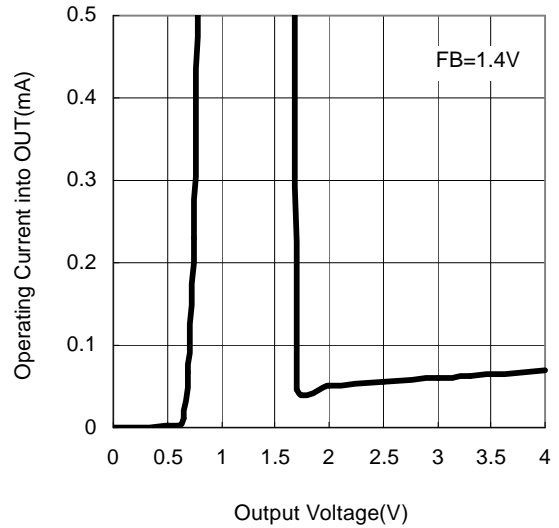
Efficiency vs. Output Current



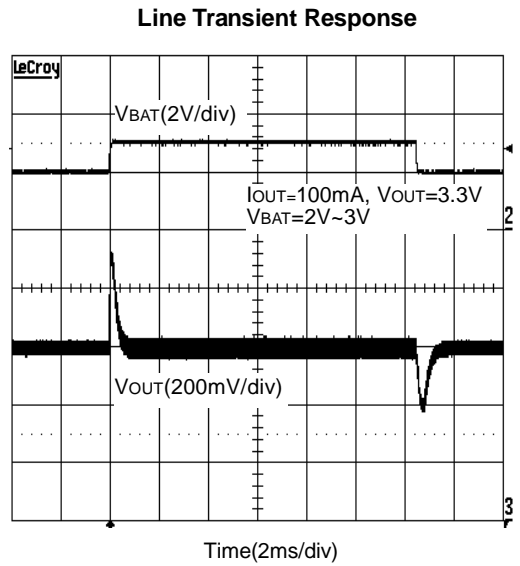
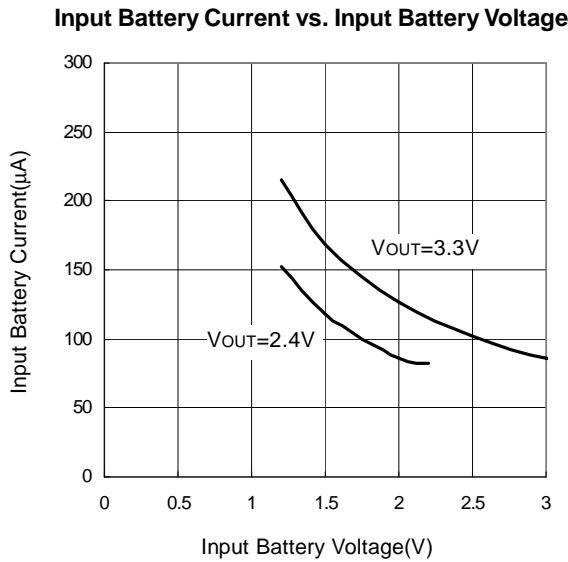
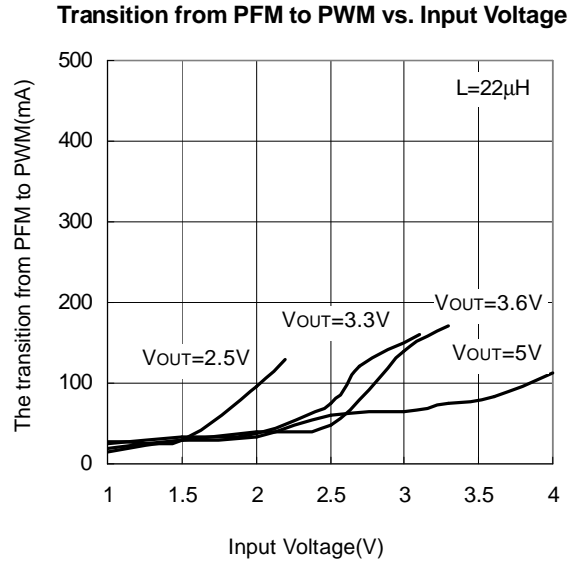
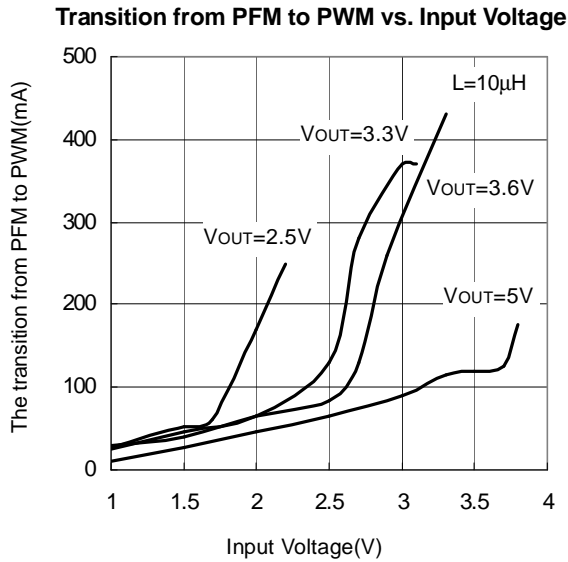
Maximum Output Current vs. Input Voltage



Operating Current into OUT vs. Output Voltage

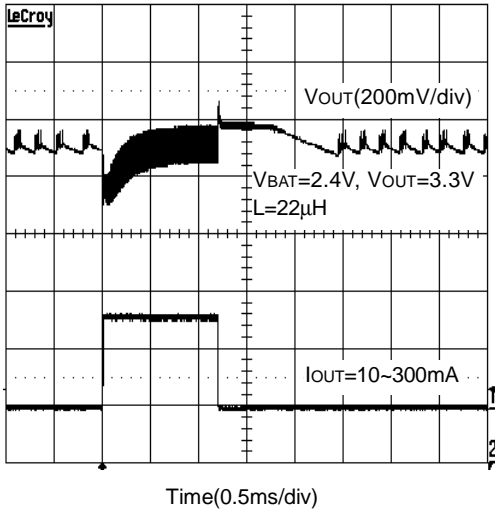


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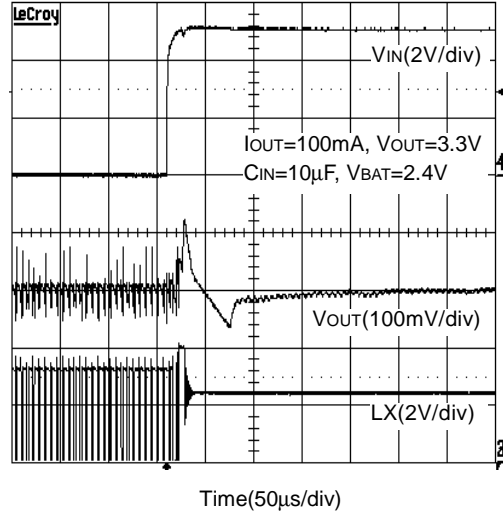


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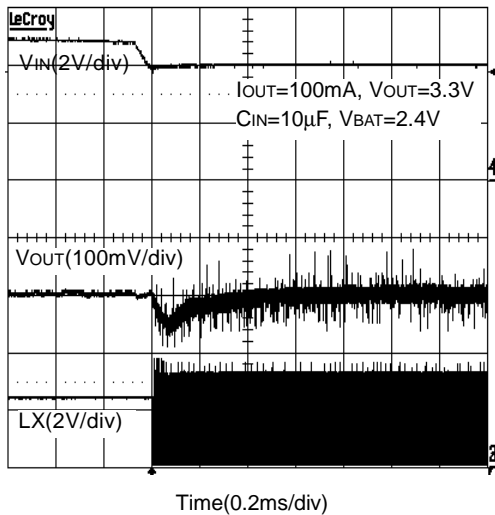
Load Transient Response



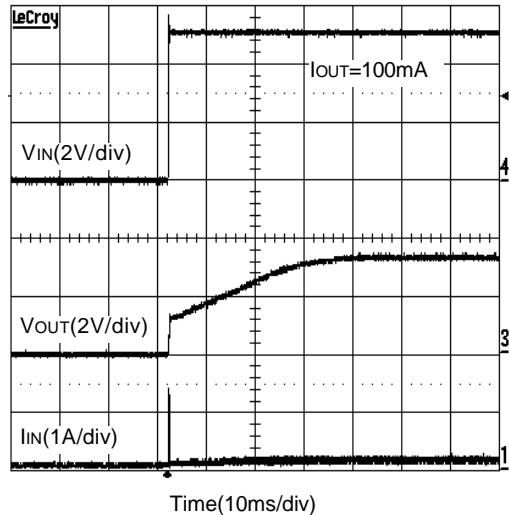
PWM to LDO



LDO to PWM

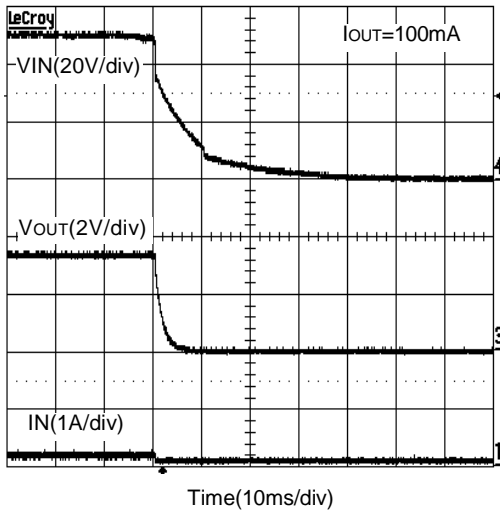


LDO Power Up

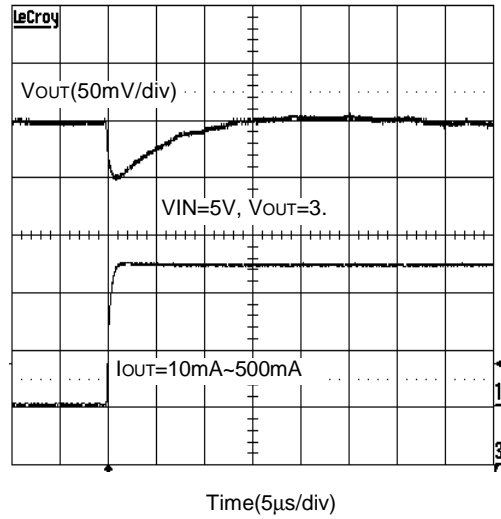


Typical Operating Characteristics (Cont.)

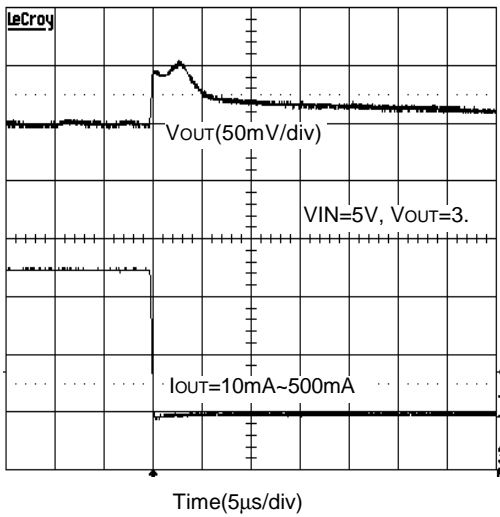
LDO Power Down



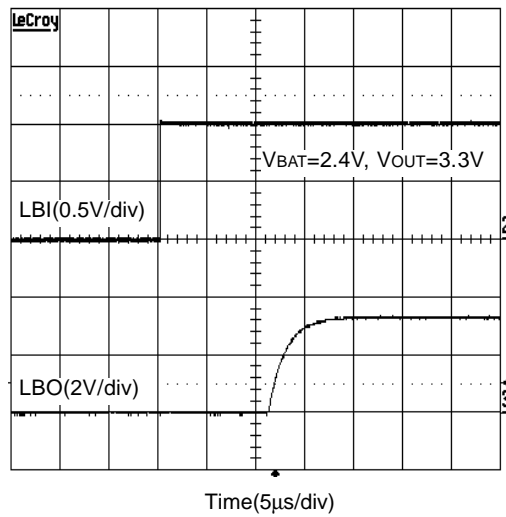
LDO Load Transient Response



LDO Load Transient Response

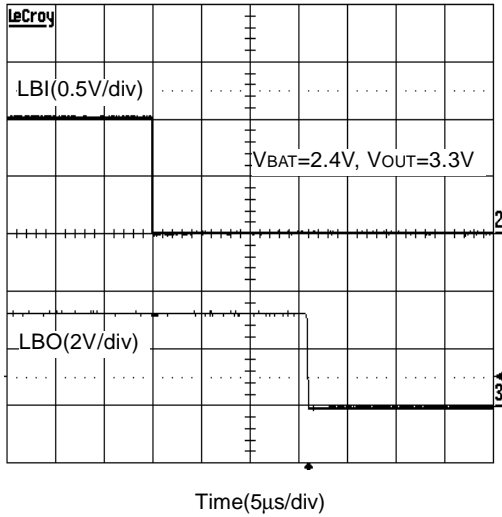


LBO Rising Delay Time

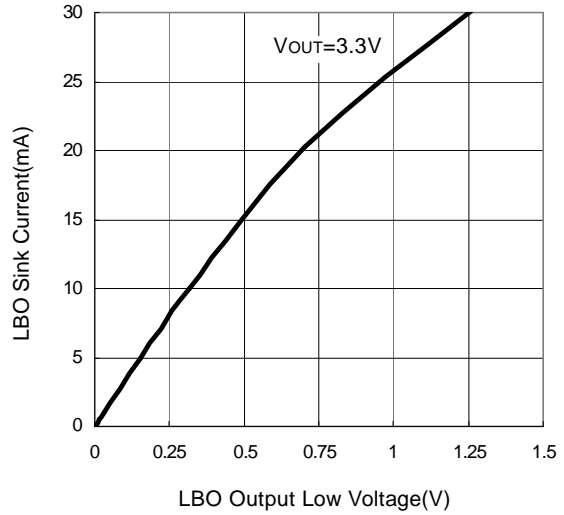


Typical Operating Characteristics (Cont.)

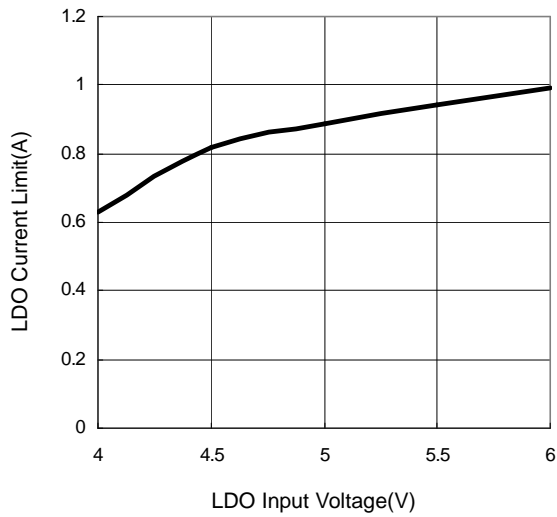
LBO Falling Delay Time



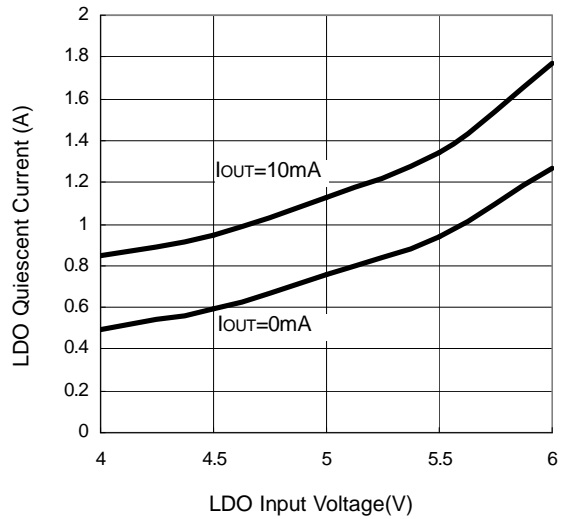
LBO Output Sink Current vs. LBO Low Voltage



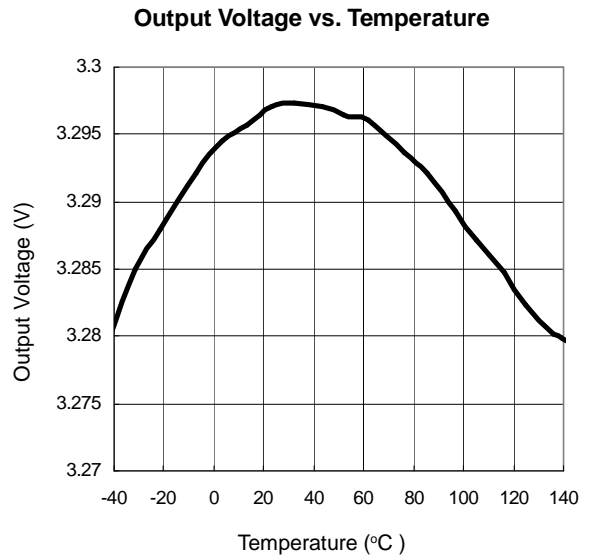
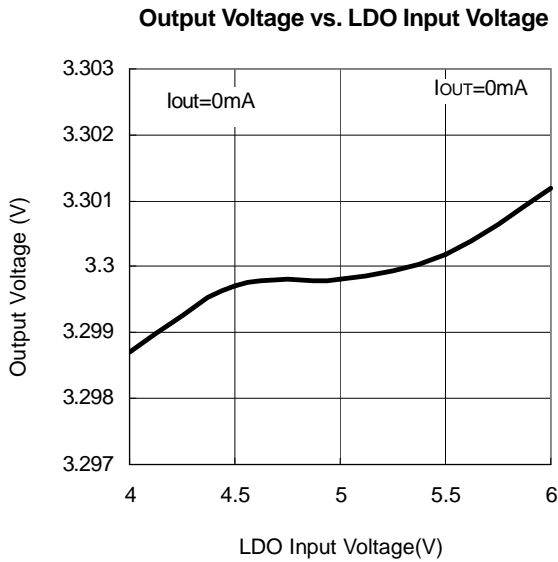
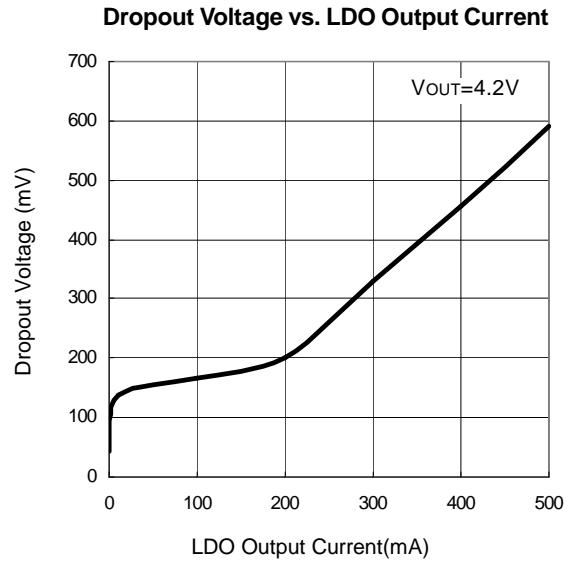
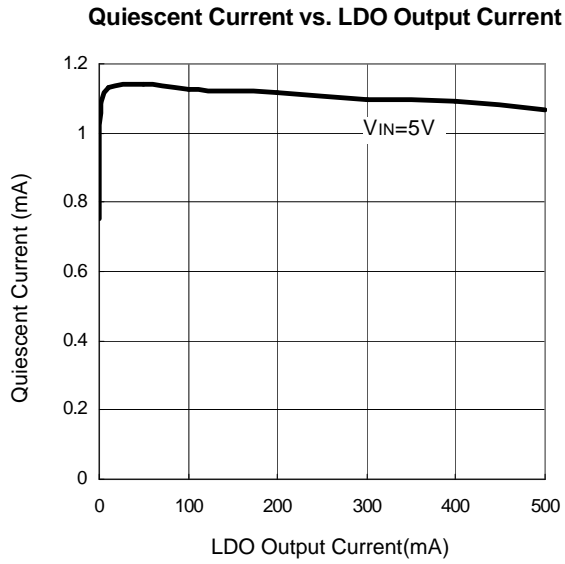
LDO Current Limit vs. LDO Input Voltage



LDO Quiescent Current vs. LDO Input Voltage



Typical Operating Characteristics (Cont.)



Function Description

PFM Control Scheme

The APW7075 features the PFM control scheme to improve the efficiency during light load. In PFM mode, the inductor stores the energy during internal N-channel MOSFET turns on, and the energy is transferred to output capacitors and load during internal P-channel MOSFET turns on. If the energy which is charged to output capacitors exceeds the requirement of load, the current will reverse from output capacitors to inductor and input capacitors. The PFM comparator compares the source (OUT) and drain (LX) of the internal P-channel MOSFET. When the current that flows through the internal P-channel MOSFET is backward (from OUT to LX), the internal P-channel MOSFET will be turned off, and the output capacitor supplies the load and maintains the output voltage. During PFM mode, the IC switches only as need to serve the load, reduce the switching frequency and associate losses in the internal switches and the external inductor. Some jitter are normal during transition from PFM to PWM mode; the transition of the PFM to PWM is dependent on the inductance values, VIN and VOUT. The output ripple is higher during PFM operation, a larger output capacitor can be used to minimize the output ripple.

Synchronous Rectification

The APW7075 has an internal N-channel and a P-channel MOSFET, it is no need for external components, the internal low RDS(ON) P-channel MOSFET replaces the discrete Schottky diode, and it reduces cost and board space. During the cycle off time, the P-channel MOSFET turns on, and the power dissipation on the P-channel MOSFET is lower than discrete Schottky diode, thus, the conversion efficiency can be improved.

Shutdown

The APW7075 has an active high enable function. Force SHDN high (>1.4V) to enable the step-up converter, SHDN low (<0.3V) to disable the step-up converter and the device enters shutdown mode. In shutdown mode, the converter stops switching and all internal control circuits are turned off, but the output is still applied by input voltage through the body diode of P-channel MOSFET, it is about Vin-0.6V. Note that when the output is applied from the VIN (LDO mode), the shutdown function is disabled.

Soft-Start

The APW7075 provides the soft-start function to get the controlled output voltage rise. When the battery voltage (<1.8V) is supplied to the device and exceeds the start-up voltage, the internal N-channel and P-channel MOSFETs start to switch and pump up the output voltage to 1.8V (if the battery voltage is over 1.8V, the output voltage will equal battery voltage during this time), which control circuitry can operate normally. The soft-start controls the rise of internal reference voltage. When the internal reference voltage exceeds the feedback voltage which is divided by the resistor from the output voltage, the soft-start circuit will control the output voltage until the output voltage is in regulation. The soft-start interval is approximately 30ms.

LDO

The output voltage has two operation modes. When VIN exceeds 3.9V, the output will become the LDO regulator and the step-up converter will be disabled. The LDO output is a P-channel low dropout regulator with 1A current limit. When the VIN is below 3.8V, the output will return to the step-up converter, and the LDO mode will be disabled. Note that when LDO mode is used, the output voltage should be under 3.8V.

Low Battery Detection

The low battery detection is used to monitor the battery voltage and to generate a signal. This function includes two pins, LBI is the inverting input of the comparator and LBO is an open drain output (See Block Diagram). When the LBI voltage drops below the threshold voltage 0.6V, the open drain device will turn on and LBO becomes low. The Low battery threshold voltage can be programmed with a resistive divider from battery to LBI pin to the ground. Since the LBO is an open drain output, it usually requires an external pull-up resistor.

Application Information

Output Voltage Selection

The output voltage of APW7075 can be adjusted by an external resistor divider, or connect FB pin to OUT for 3.3V and to the ground for 2.5V (see Application Schematic). The internal reference voltage is 1.2V and the allowed output voltage is from 2.5V to 5.5V. The following equation can be used to calculate the output voltage:

$$V_{OUT} = \left(1 + \frac{R1}{R2} \right) \times 1.2V$$

Programming Low Battery Threshold Voltage

The low battery threshold voltage can be programmed with a resistive divider from battery to LBI pin to the ground (see Application Schematic). The internal reference voltage is 0.6V, and the low battery threshold voltage must be below the battery voltage. The following equation can be used to calculate the low battery threshold voltage:

$$V_{BAT-TH} = \left(1 + \frac{R3}{R4} \right) \times 0.6V$$

Inductor Selection

The APW7075 works well with a 22μH inductor in most applications. The inductance values determine the inductor ripple current and affect the output current. Higher inductance values reduce ripple and improve efficiency. Lower inductance values have fast response but increase the ripple and reduce the efficiency. The maximum allowed LX current is 1A (the maximum output current shows in Typical Characteristics), therefore, the peak inductor current cannot exceed it. The following equations calculate the inductor current, and output current.

$$I_{OUT} = I_L \times (1-D)$$

$$\Delta I_L = (V_{OUT} - V_{IN}) \times \frac{(1-D)}{L \times f}$$

Where:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

The inductor's DC resistance affects the efficiency; larger resistance dissipates more power, it should be as small as possible. It is important to choose the inductor's saturation current rating greater than the peak current which the inductor will flow in the application.

Boost Converter Input Capacitor Selection

At least a 10μF input capacitor is recommended to stabilize the battery voltage and minimizes the peak current ripple from the battery.

LDO Input Capacitor Selection

The LDO input capacitor with larger values and lower ESRs provides better PSRR and line transient response. At least a 10μF capacitor is recommended.

Output Capacitor Selection

The output capacitor is used for supplying the output during internal N-channel MOSFET turns on time. Larger capacitance and lower ESR reduce the output voltage ripple. The output voltage supplies the power to the IC and so the output voltage ripple must be as small as possible to provide better PSRR. In general, a 100μF to 220μF low ESR Tantalum capacitor is recommended, a 1μF ceramic capacitor in parallel for bypassing the noise is also recommended. The following equation calculates the output ripple.

$$V_{ripple} = I_{OUT} \times \left(\frac{V_{OUT} - V_{BAT}}{C_{OUT} \times F_{SW} \times V_{OUT}} + ESR \right)$$

Layout Consideration

The correct PCB layout is important for all switching converters. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Figure 5 illustrates the layout guidelines, the bold lines indicate the high current paths; these traces must be short and wide. The input capacitors, output capacitors, and the inductor should be as close to the IC as possible. Use a common ground plane for power ground and a different one for control ground to minimize the effects of the ground noise. Connect these ground planes at a node close to the GND pin of IC. The feedback and LBI resistor dividers should be placed as close to the IC as possible.

Application Information (Cont.)

Layout Consideration (Cont.)

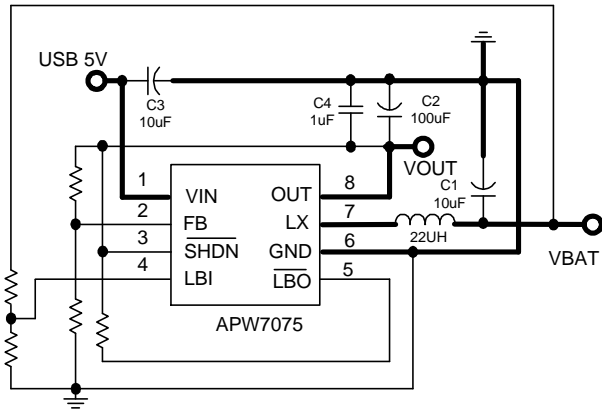
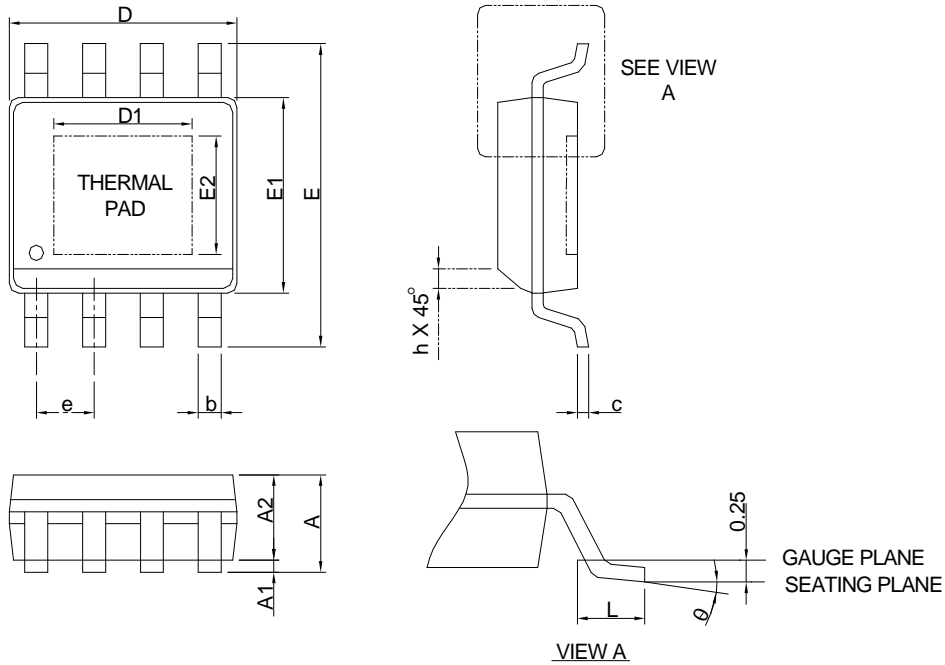


Figure 5. Recommended Layout Diagram

Package Information

SOP-8P

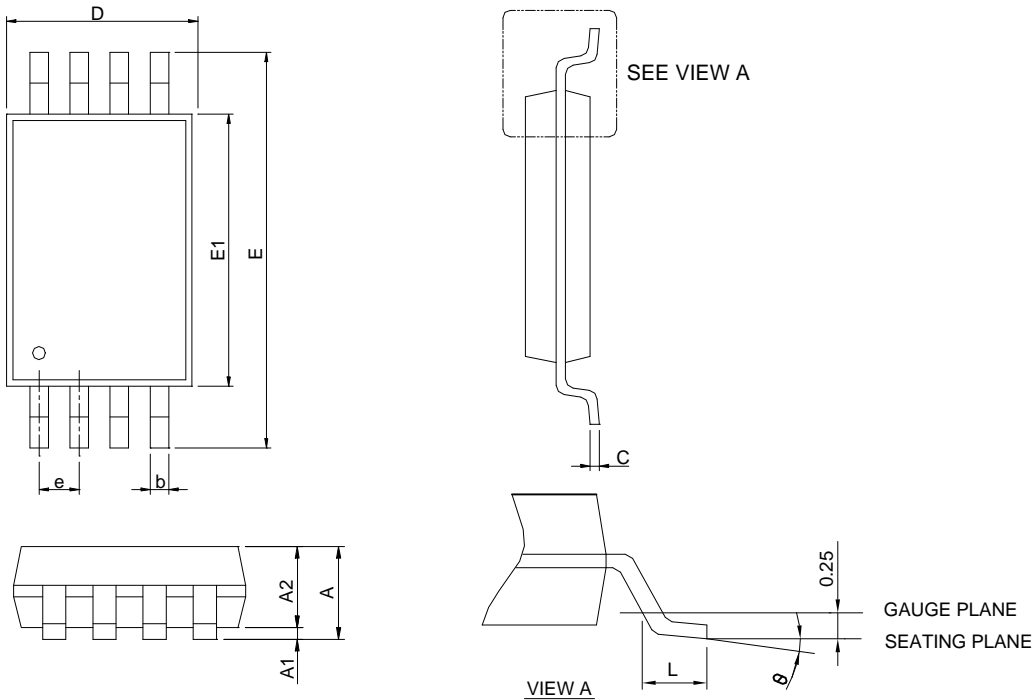


| SYMBOL | SOP-8P | | | |
|--------|-------------|------|-----------|-------|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.60 | 0.063 | |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| A2 | 1.25 | | 0.049 | |
| b | 0.31 | 0.51 | 0.012 | 0.020 |
| c | 0.17 | 0.25 | 0.007 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| D1 | 2.25 | 3.50 | 0.098 | 0.138 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| E2 | 2.00 | 3.00 | 0.079 | 0.118 |
| e | 1.27 BSC | | 0.050 BSC | |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

- Note : 1. Follow JEDEC MS-012 BA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

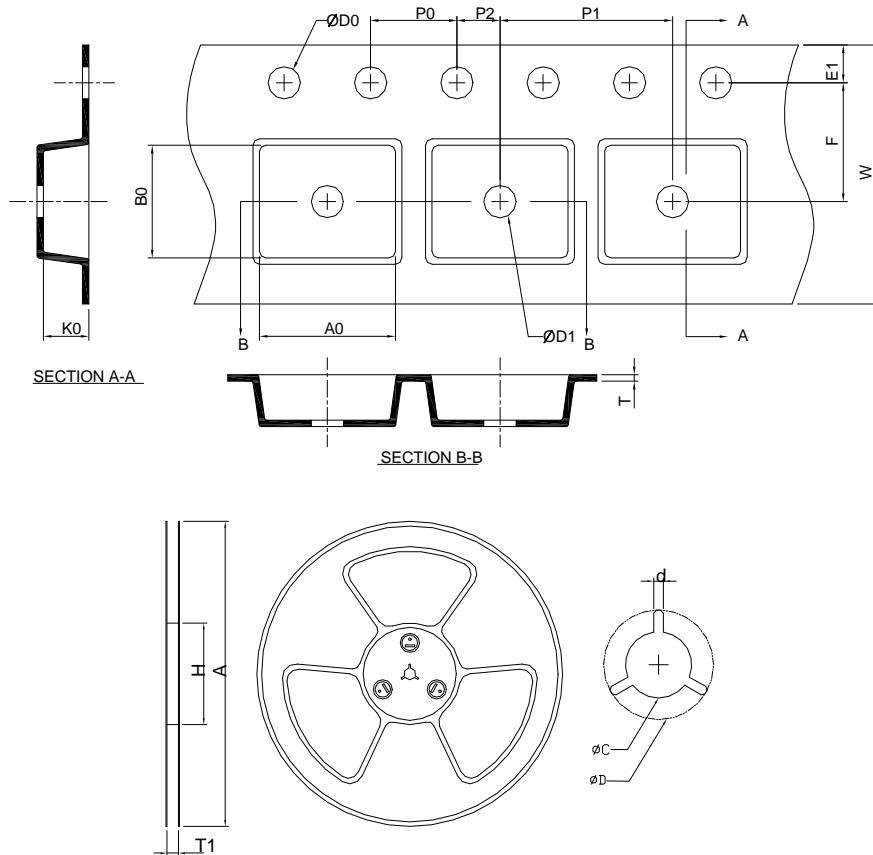
TSSOP-8



| SYMBOL | TSSOP-8 | | | |
|--------|-------------|------|-----------|-------|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.004 | 0.008 |
| D | 2.90 | 3.10 | 0.114 | 0.122 |
| E | 6.20 | 6.60 | 0.244 | 0.260 |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 BSC | | 0.026 BSC | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| θ | 0° | 8° | 0° | 8° |

- Note : 1. Follow JEDEC MO-153 AA
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



| Application | A | H | T1 | C | d | D | W | E1 | F |
|-------------|-------------|------------|--------------------|--------------------|-----------|-------------------|------------|------------|------------|
| SOP-8P | 330.0 ±0.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0 ±0.30 | 1.75 ±0.10 | 5.5 ±0.05 |
| | P0 | P1 | P2 | D0 | D1 | T | A0 | B0 | K0 |
| | 4.0 ±0.10 | 8.0 ±0.10 | 2.0 ±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.40 ±0.20 | 5.20 ±0.20 | 2.10 ±0.20 |
| Application | A | H | T1 | C | d | D | W | E1 | F |
| TSSOP-8 | 330.0 ±0.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0 ±0.30 | 1.75 ±0.10 | 5.5 ±0.10 |
| | P0 | P1 | P2 | D0 | D1 | T | A0 | B0 | K0 |
| | 4.00 ±0.10 | 8.00 ±0.10 | 2.00 ±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.90 ±0.20 | 3.40 ±0.20 | 1.60 ±0.20 |

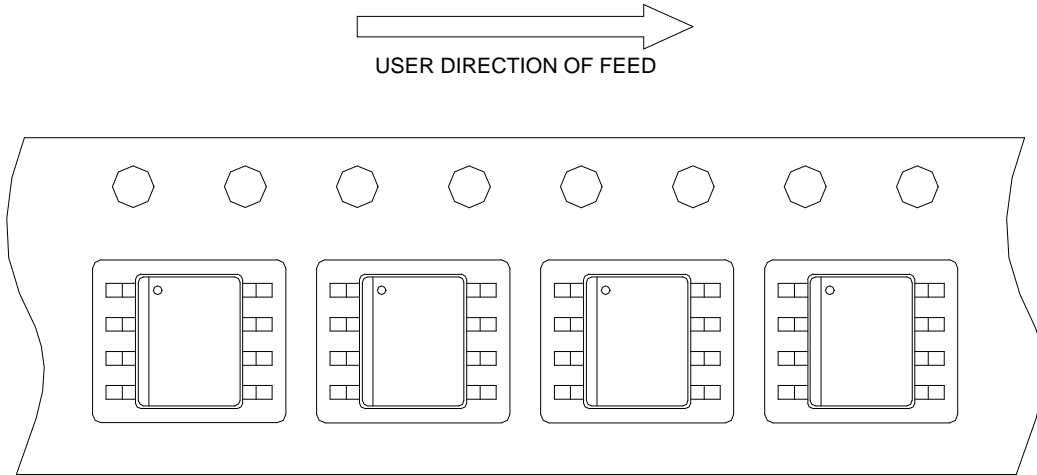
(mm)

Devices Per Unit

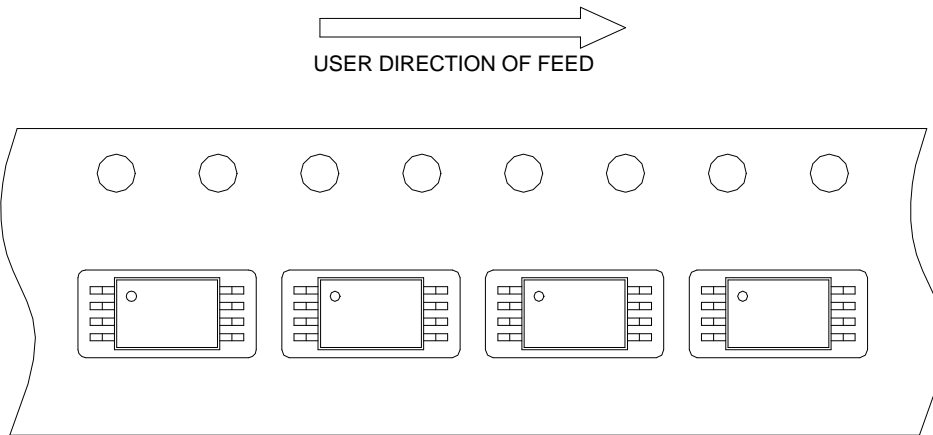
| Package Type | Unit | Quantity |
|--------------|-------------|----------|
| SOP-8P | Tape & Reel | 2500 |
| TSSOP-8 | Tape & Reel | 2500 |

Taping Direction Information

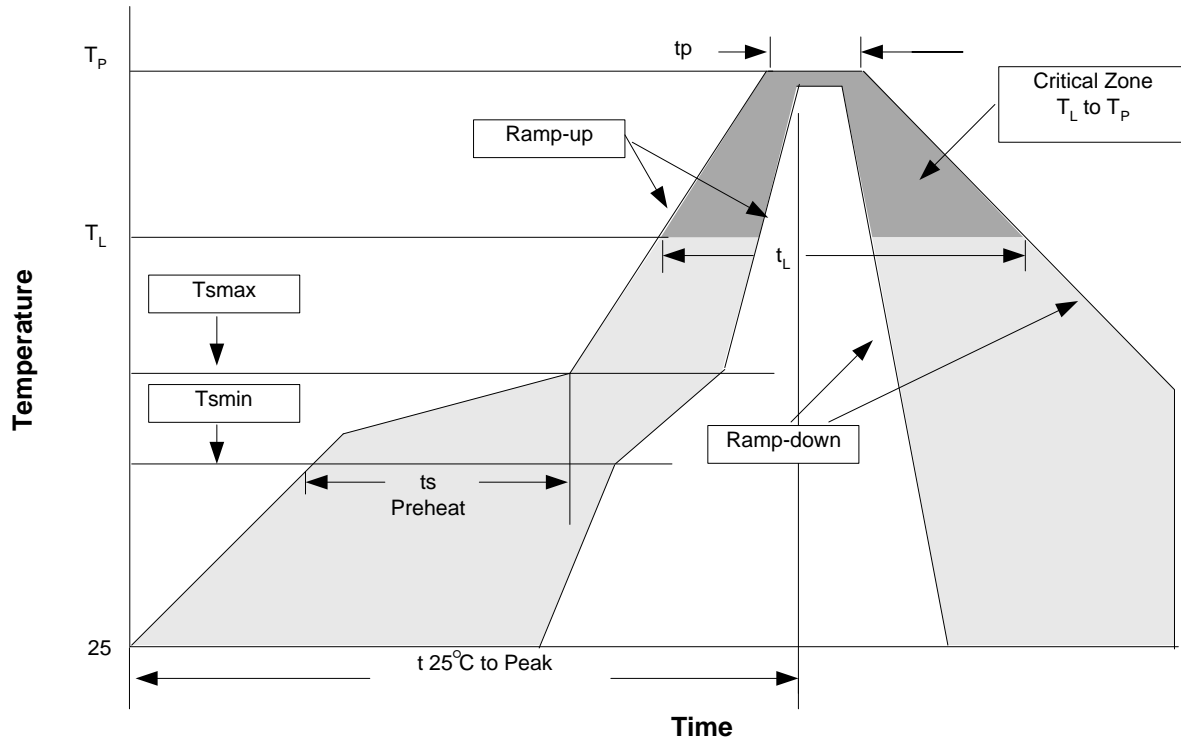
SOP-8P



TSSOP-8



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

| Test item | Method | Description |
|---------------|---------------------|-------------------------------|
| SOLDERABILITY | MIL-STD-883D-2003 | 245°C, 5 sec |
| HOLT | MIL-STD-883D-1005.7 | 1000 Hrs Bias @125°C |
| PCT | JESD-22-B, A102 | 168 Hrs, 100%RH, 121°C |
| TST | MIL-STD-883D-1011.9 | -65°C~150°C, 200 Cycles |
| ESD | MIL-STD-883D-3015.7 | VHBM > 2KV, VMM > 200V |
| Latch-Up | JESD 78 | 10ms, 1 _{tr} > 100mA |

Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|--|-------------------------|------------------|
| Average ramp-up rate (T _L to T _P) | 3°C/second max. | 3°C/second max. |
| Preheat | | |
| - Temperature Min (T _{min}) | 100°C | 150°C |
| - Temperature Max (T _{max}) | 150°C | 200°C |
| - Time (min to max) (ts) | 60-120 seconds | 60-180 seconds |
| Time maintained above: | | |
| - Temperature (T _L) | 183°C | 217°C |
| - Time (t _L) | 60-150 seconds | 60-150 seconds |
| Peak/Classification Temperature (T _P) | See table 1 | See table 2 |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds | 20-40 seconds |
| Ramp-down Rate | 6°C/second max. | 6°C/second max. |
| Time 25°C to Peak Temperature | 6 minutes max. | 8 minutes max. |

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

| Package Thickness | Volume mm ³ <350 | Volume mm ³ ≥350 |
|-------------------|--------------------------------|--------------------------------|
| <2.5 mm | 240 +0/-5°C | 225 +0/-5°C |
| ≥2.5 mm | 225 +0/-5°C | 225 +0/-5°C |

Table 2. Pb-free Process – Package Classification Reflow Temperatures

| Package Thickness | Volume mm ³ <350 | Volume mm ³ 350-2000 | Volume mm ³ >2000 |
|-------------------|--------------------------------|------------------------------------|---------------------------------|
| <1.6 mm | 260 +0°C* | 260 +0°C* | 260 +0°C* |
| 1.6 mm – 2.5 mm | 260 +0°C* | 250 +0°C* | 245 +0°C* |
| ≥2.5 mm | 250 +0°C* | 245 +0°C* | 245 +0°C* |

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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