Low Dropout 600mA Linear Regulator for DC Fan Control

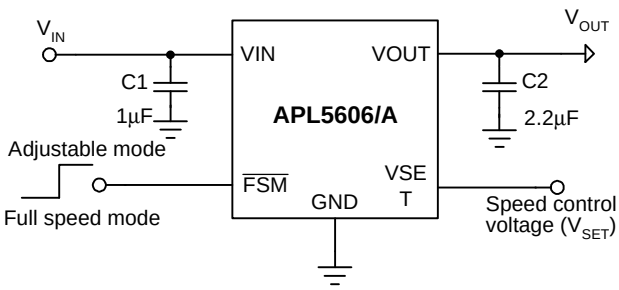
Features

- **Low Dropout Voltage: 220mV (typical) @ 600mA**
- **Low Quiescent Current: 140μA**
- **Selectable Adjustable/Full Speed Mode**
- **O/I Voltage Ratio in Adjustable Mode : 1.6 times**
- **Stable with Low ESR Ceramic Capacitors**
- **Over-Temperature Protection**
- **Current-Limit Protection with Foldback Current**
- **Internal Soft-Start**
- **SOP-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APL5606/A is a low quiescent current and low drop-out linear regulator which is designed with a P-channel pass MOSFET to power a DC fan and delivers output current up to 600mA. In adjustable mode, the output voltage follows the 1.6 times of the voltage on VSET pin to dynamically adjust the DC fan speed; in full speed mode, the internal P-channel MOSFET fully turns on to drive the DC fan with maximum supply voltage for full speed operation.The APL5606/A with low 140μA quiescent current is ideal for battery-powered system appliances. It is also stable with a low-ESR ceramic output capacitor (2.2μF typical) to reduce total cost and to minimize the PCB area required. The APL5606/A features current-limit (with foldback current) and over-temperature protections to protect the device against current over-loads and over-temperature. The APL5606/A is available in a SOP-8 package.

Simplified Application Circuit



Applications

- **Notebook Fan Driver**
- **Motherboards**
- **PC Peripherals**
- **Battery-Powered System**

Ordering and Marking Information

APL5606/A □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
K : SOP-8
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device
G : Halogen and Lead Free Device

APL5606/A K :

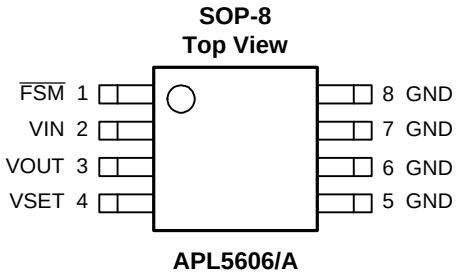
APL5606 XXXXX	APL5606A XXXXX

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND	-0.3 ~ 6.5	V
$V_{\overline{FSM}}$	$\overline{FSM}$ to GND	-0.3 ~ V_{IN}+0.3	V
V_{OUT}	VOUT to GND	-0.3 ~ V_{IN}+0.3	V
T_J	Maximum Junction Temperature	150	°C
P_D	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_L	Lead Temperature, 10 Seconds	260	°C

Note1: Stresses beyond the absolute maximum rating may damage the device and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance (Note 2) SOP-8	80	°C/W

Note 2 : q_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN to GND	4.5 ~ 6	V
$V_{\overline{FSM}}$	$\overline{FSM}$ to GND	0 ~ V_{IN}	V
V_{OUT}	VOUT to GND	0 ~ V_{IN}-V_{DROP}	V
V_{SET}	VSET to GND	0 ~ 3.3	V
I_{OUT}	Output Current	0 ~ 0.6	A
C_{IN}	Input Capacitor	0.82 ~ 470	µF
C_{OUT}	Output Capacitor	1 ~ 330	µF
T_J	Junction Temperature	-40 ~ 125	°C
T_A	Ambient Temperature	-40 ~ 85	°C

Electrical Characteristics

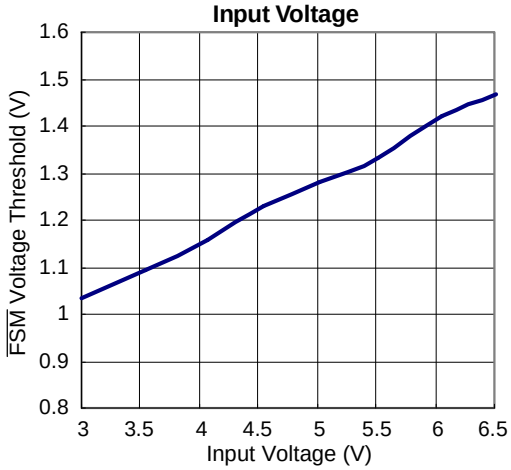
Refer to the typical application circuit. V_{IN} = 5V, $V_{\overline{FSM}}$ = V_{IN}, I_{OUT} = 1mA~600mA, T_J = -40 to 125 °C, T_A = -40 to 85°C, unless otherwise specified. Typical values are at T_A = 25 °C.

Symbol	Parameter	Test Conditions	APL5606/A			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_Q	Quiescent Current	$V_{\overline{FSM}}$ = 0V	-	-	1	μA
		$V_{\overline{FSM}}$ = 5V, I_{OUT} = 0A	-	140	200	μA
UNDER-VOLTAGE-LOCKOUT (UVLO)						
	VIN UVLO Threshold	V_{IN} rising	2.1	2.5	2.9	V
	VIN UVLO Hysteresis		-	0.15	-	V
OUTPUT VOLTAGE						
	VOUT Voltage / VSET Voltage	T_J = 25°C, V_{IN}=5.5V, I_{OUT}=1mA, V_{SET}=3.3V	1.552	1.6	1.648	V/V
	VOUT Voltage / VSET Voltage	T_J = 40 ~ 125°C, V_{IN}=5.5V, I_{OUT}=1mA, V_{SET}=1 ~ 3.3V	1.504	1.6	1.696	V/V
	Minimum VSET Voltage in Full Speed Mode	$V_{\overline{FSM}}$ = 0V	-	0.8	-	V
	VSET pin Current	V_{SET}=5V	-	0.05	1	μA
	Line Regulation	V_{IN} = V_{OUT} + 1V to 6V	-	0.03	0.1	%/V
	Load Regulation	I_{OUT} = 1mA to 600mA	-	60	100	mV
V_{DROP}	Dropout Voltage	I_{OUT} = 600mA, V_{OUT}=2.5V	-	250	400	mV
		I_{OUT} = 600mA, V_{OUT}=3.3V	-	220	350	mV
		I_{OUT} = 600mA, V_{OUT}=5V	-	200	320	mV
PROTECTION AND SOFT-START						
I_{LIM}	Output Current-Limit		700	-	-	mA
	Thermal Shutdown Temperature		-	150	-	°C
	Thermal Shutdown Hysteresis		-	40	-	°C
	Foldback Current-Limit	V_{OUT} < 0.6V	-	250	-	mA
T_{SS}	Soft-Start Time		-	130	300	μs
	VOUT Pull Low Resistance	$V_{\overline{FSM}}$ =0V, V_{OUT}=0.5V	-	60	-	Ω
LOGIC INPUT						
	$\overline{FSM}$ Logic Input-High Level		1.6	-	-	V
	$\overline{FSM}$ Logic Input-Low Level		-	-	0.4	V
	$\overline{FSM}$ Pull-Low Resistance	APL5606, $V_{\overline{FSM}}$ <3V	-	2	-	MΩ
	$\overline{FSM}$ Pull-High Resistance	APL5606A	-	390	-	kΩ

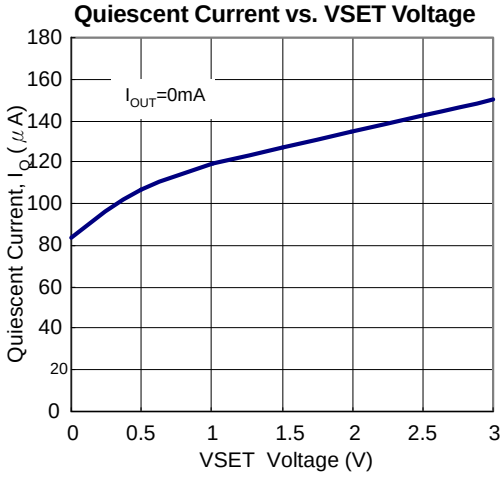
Typical Operating Characteristics

V_{IN}=5V, V_{SET}=2V, V_{OUT}=3.2V, C_{IN}=1µF, C_{OUT}=2.2µF, unless otherwise specified.

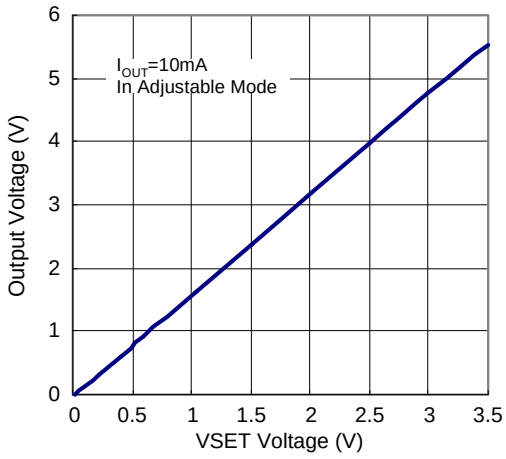
$\overline{FSM}$ Voltage Threshold vs. Input Voltage



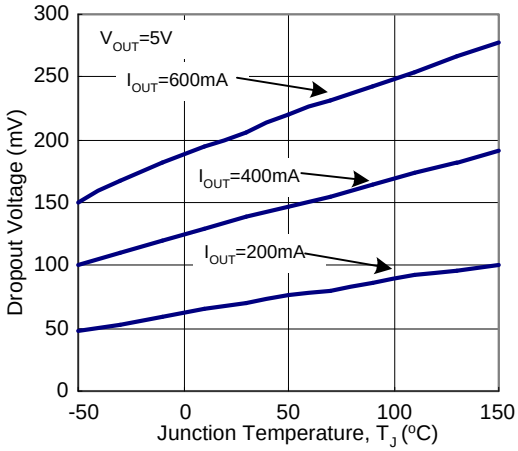
Quiescent Current vs. VSET Voltage



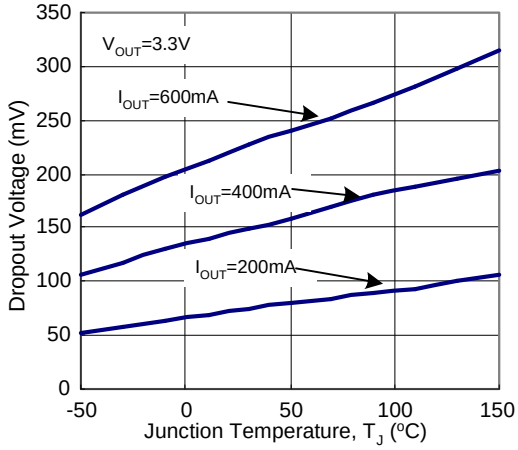
VSET Voltage vs. Output Voltage



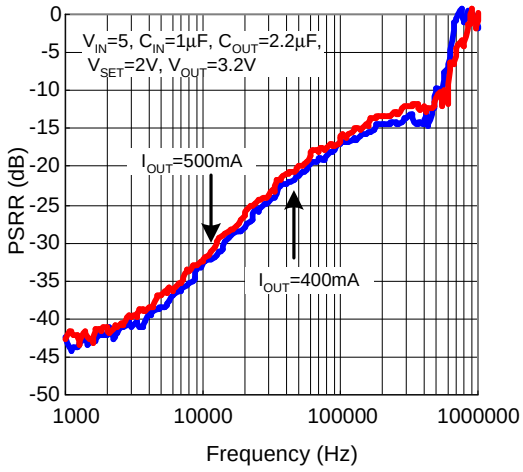
Dropout vs. Junction Temperature



Dropout vs. Junction Temperature



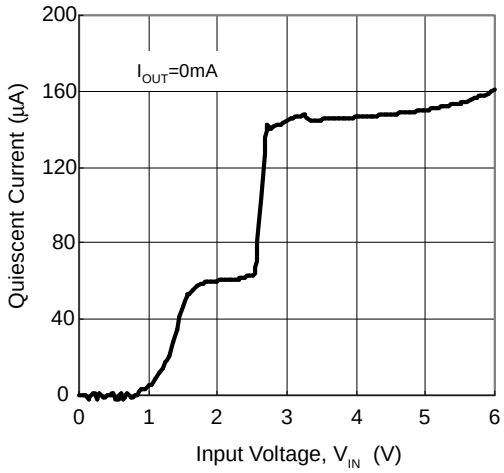
Power Supply Rejection Ratio (PSRR)



Typical Operating Characteristics (Cont.)

V_{IN}=5V, V_{SET}=2V, V_{OUT}=3.2V, C_{IN}=1µF, C_{OUT}=2.2µF, unless otherwise specified.

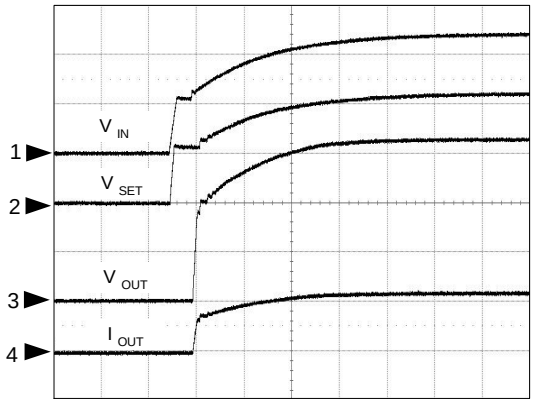
Quiescent Current vs. Input Voltage



Operating Waveforms

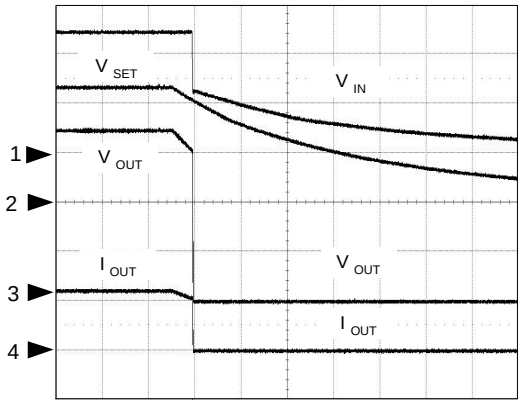
V_{IN}=5V, V_{SET}=2V, V_{OUT}=3.2V, C_{IN}=1µF, C_{OUT}=2.2µF, unless otherwise specified.

Power On



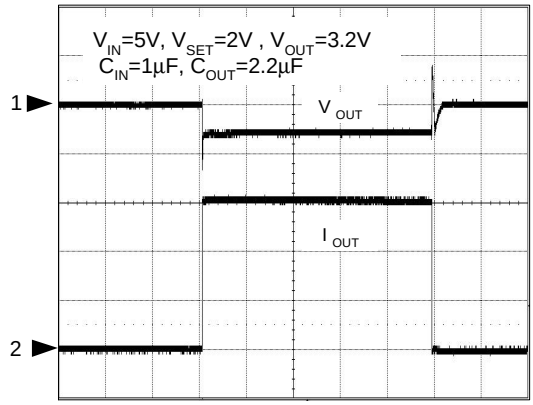
CH1 : V_{IN} , 2V/div
CH2 : V_{SET} , 1V/div
CH3 : V_{OUT} , 1V/div
CH4 : I_{OUT} , 500mA/div
Time : 1ms/div

Power Off



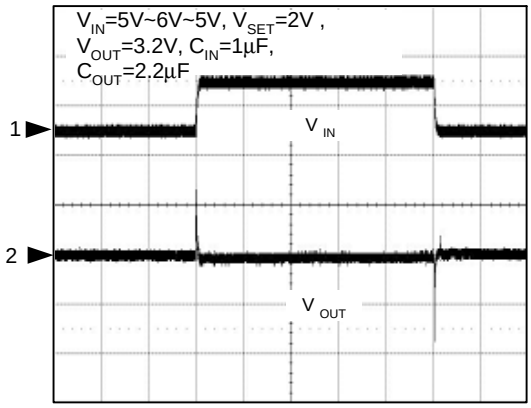
CH1 : V_{IN} , 2V/div
CH2 : V_{SET} , 1V/div
CH3 : V_{OUT} , 1V/div
CH4 : I_{OUT} , 500mA/div
Time : 200ms/div

Load Transient



CH1 : V_{OUT} , 100mV/div
CH2 : I_{OUT} , 200mV/div
Time : 200µs/div

Line Transient

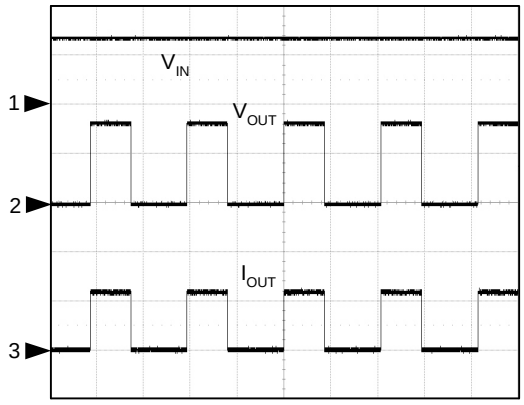


CH1 : V_{IN} , 1V/div
CH2 : V_{OUT} , 100mV/div
Time : 1ms/div

Operating Waveforms (Cont.)

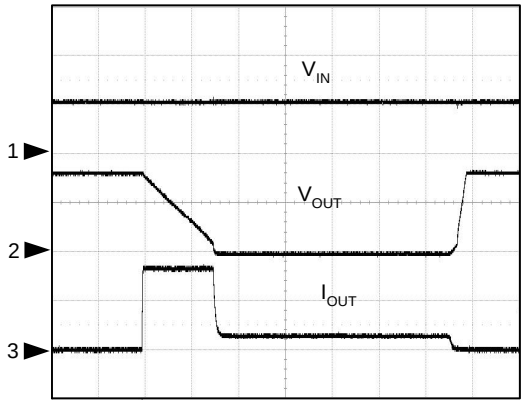
V_{IN}=5V, V_{SET}=2V, V_{OUT}=3.2V, C_{IN}=1µF, C_{OUT}=2.2µF, unless otherwise specified.

Thermal Shutdown



CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{OUT} , 500mA/div
Time : 500ms/div

Current-Limit and Short-Circuit Current-Limit



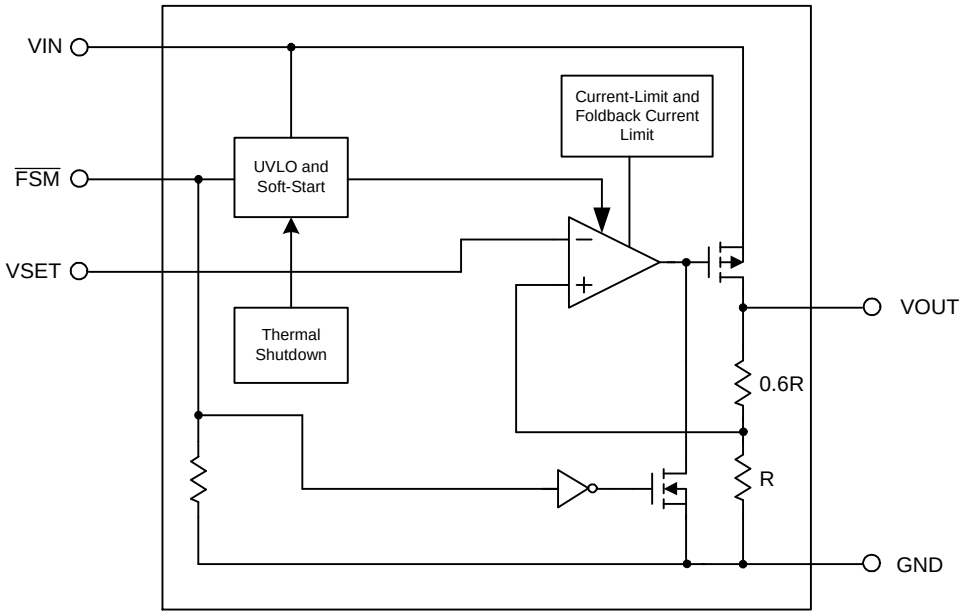
CH1 : V_{IN} , 5V/div
CH2 : V_{OUT} , 2V/div
CH3 : I_{OUT} , 1A/div
Time : 2ms/div

Pin Description

PIN		FUNCTION
NO.	NAME	
1	$\overline{FSM}$	Adjustable/Full Speed Mode Selection Input Pin. Output voltage follows 1.6 times of the voltage on VSET pin. If the $\overline{FSM}$ is at low level, the IC operates in full speed mode with the P-channel MOSFET fully turned on. The $\overline{FSM}$ pin is internally pulled low in the APL5606 and is pulled high in the APL5606A.
2	VIN	Supply Voltage Input Pin. Supply voltage can range from 4.5V to 6V. Bypass with a 1μF (typical) capacitor to GND
3	VOUT	Regulator Output. Sources up to 600mA. A small capacitor is needed and connected from this pin to ground to assure stability.
4	VSET	Output Voltage-Set Input. The output voltage follows the 1.6 times of the VSET voltage.
5,6,7,8	GND	Ground. These pins are internally connected with the internal leadframe. Connect these pins to a wide ground plane for good heat dissipation.

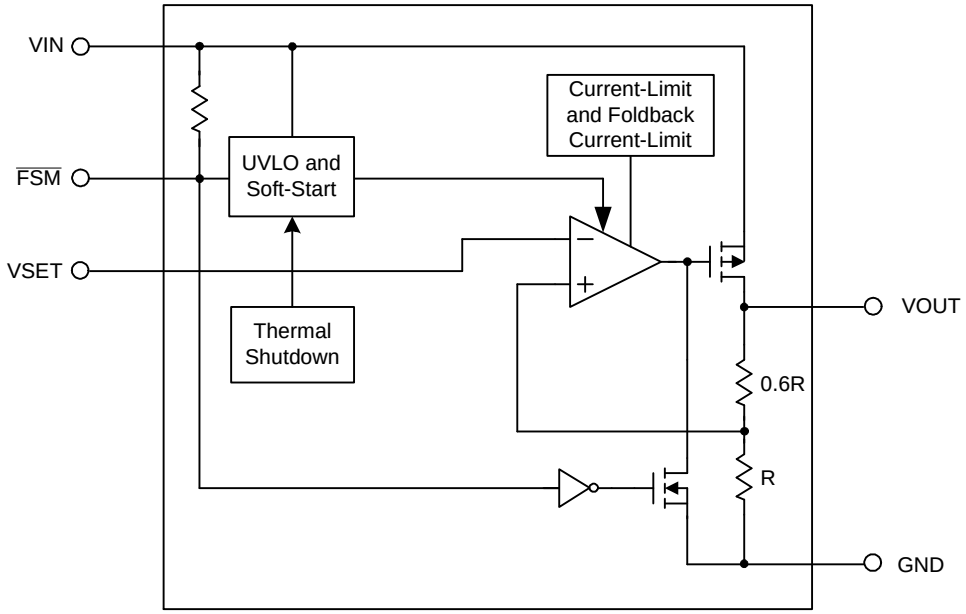
Block Diagram

APL5606

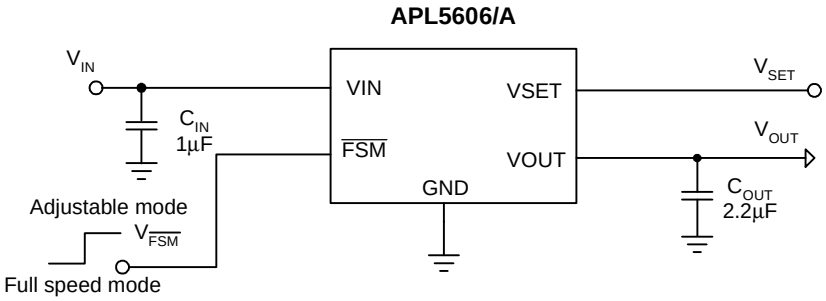


Block Diagram (Cont.)

APL5606A



Typical Application Circuit



Function Description

Under-Voltage Lock-Out (UVLO)

The APL5606/A has a built-in under-voltage lock-out circuit to keep the output off until the internal circuitry is operating properly. The UVLO function initiates a soft-start process after input voltage exceeds its rising UVLO threshold during power on. Typical UVLO threshold is 2.5V with 0.15V hysteresis.

Soft-Start

The APL5606/A provides an internal soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. Approximate 20μs delay time after the V_{IN} is over the UVLO threshold, the IC starts a soft-start. The typical soft-start interval is about 130μs.

Adjustable/Full Speed Mode Selection

The APL5606/A features an input pin to select one of the operation modes for DC fan speed control. In adjustable mode, the output voltage follows the 1.6 times of the voltage on VSET pin to dynamically adjust the DC fan speed; in full speed mode, the internal P-channel MOSFET fully turns on to drive the DC fan with maximum supply voltage (V_{IN}-V_{DROP}) for full speed operation. Driving the $\overline{FSM}$ voltage at high level($V_{\overline{FSM}}$>1.6V) sets the IC to operate in adjustable mode; driving the $\overline{FSM}$ at low level($V_{\overline{FSM}}$<0.4V) sets the IC to operate in full speed mode. The $\overline{FSM}$ pin is internally pulled low in the APL5606 and is pulled high in the APL5605A.

Current-Limit

The APL5606/A provides a current-limit circuitry, which monitors the output current and controls P-MOS's gate voltage to limit the output current at 700mA (min.).

Foldback Current-Limit

When the output voltage drops below 0.6V (typical), which is caused by overload or short-circuit, the foldback current-limit circuitry limits the output current to 250mA. The foldback circuit current-limit is used to reduce the power dissipation during short-circuit condition. The foldback current-limit is disabled for 0.6ms (typical) after the UVLO threshold is reached, therefore, the IC has normal 700mA (min.) current-limit level during start-up.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5606/A. When the junction temperature exceeds +150°C, the thermal shutdown circuitry disables the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal protection is designed to protect the IC in the event of over-temperature conditions. For reliable operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

The APL5606/A requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, place the Input capacitors near VIN as close as possible. The input capacitors should be larger than 0.82µF.

Output Capacitor

The APL5606/A needs a proper output capacitor to maintain circuit stability and to improve transient response over-temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1µF. With X5R and X7R dielectrics, 2.2µF is sufficient at all operating temperatures.

Operation Region and Power Dissipation

The APL5606/A maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = \frac{(T_J - T_A)}{\theta_{JA}}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(150-25)/80$$
$$= 1.56\ (W)$$

For normal operation, do not exceed the maximum junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

$$P_D=(125-25)/80$$
$$= 1.25\ (W)$$

PCB Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN
2. Ceramic capacitors for load must be placed near the load as close as possible
3. To place APL5606/A and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 1, must have wide tracks.

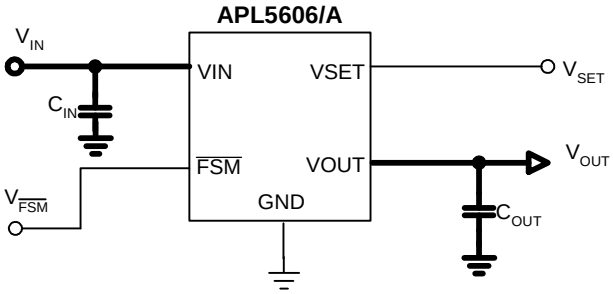


Figure 1

Optimum performance can only be achieved when the device is mounted on a PC board according to the SOP-8 Board Layout diagram.

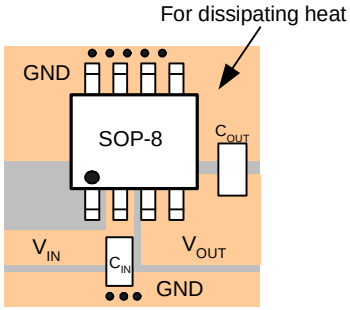
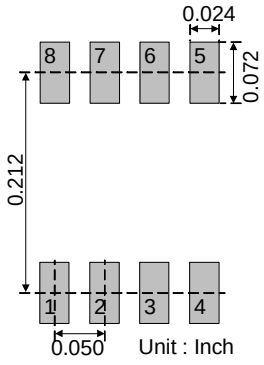


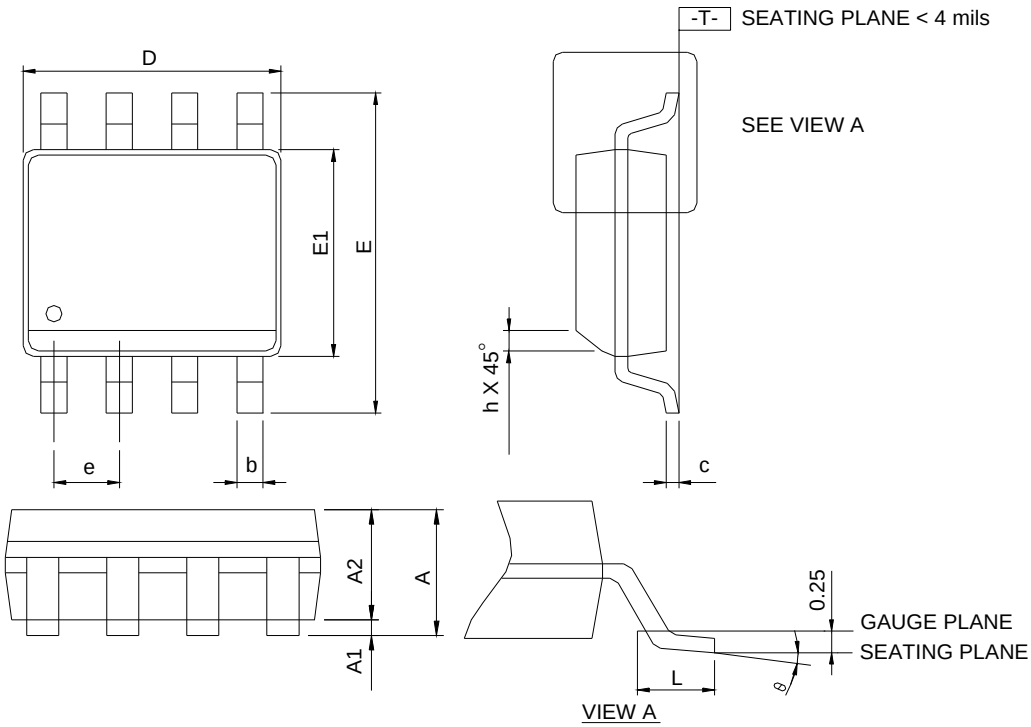
Figure 2

Recommanded Minimum Footprint



Package Information

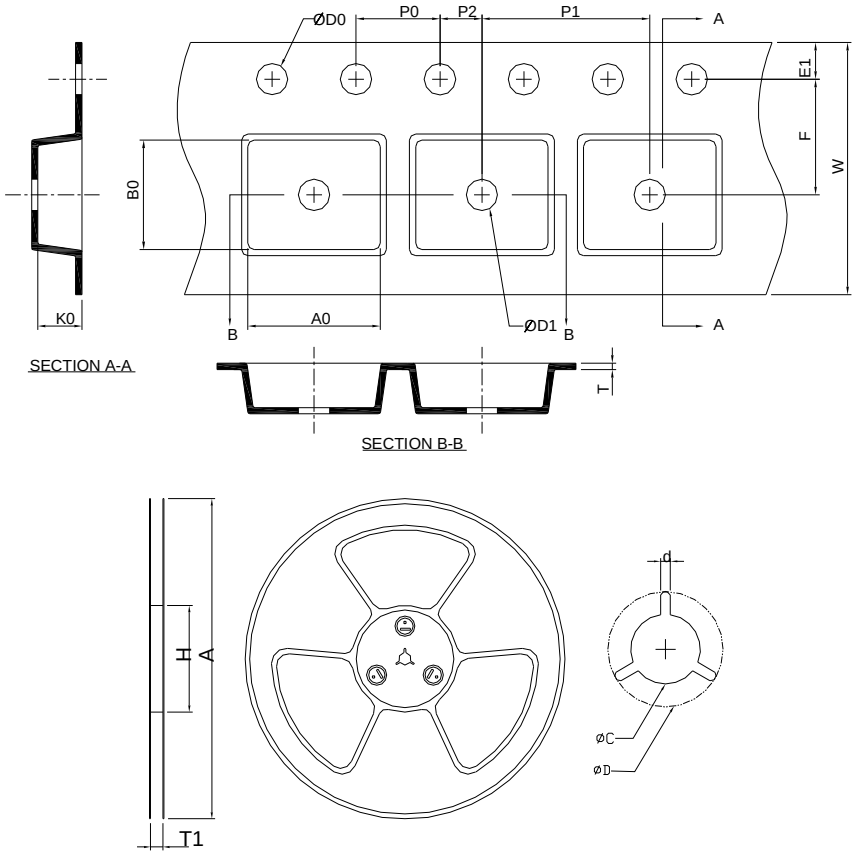
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

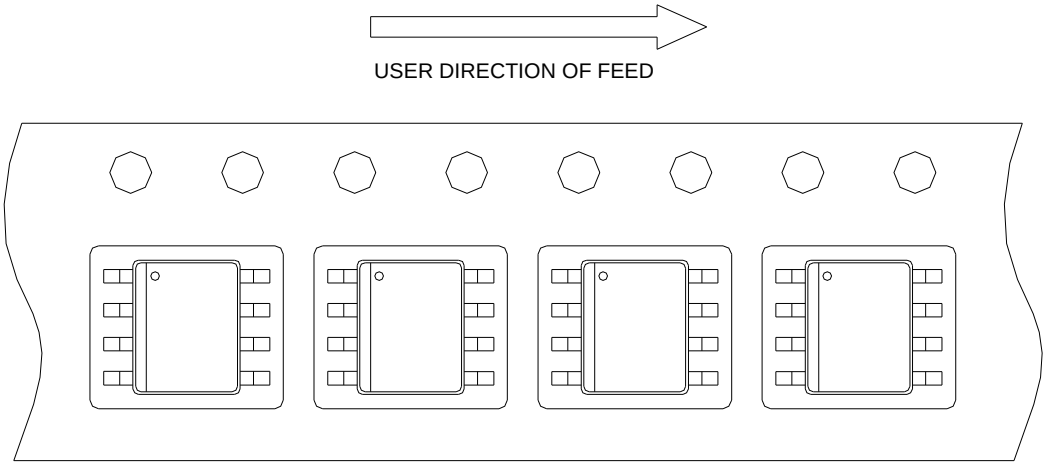
(mm)

Devices Per Unit

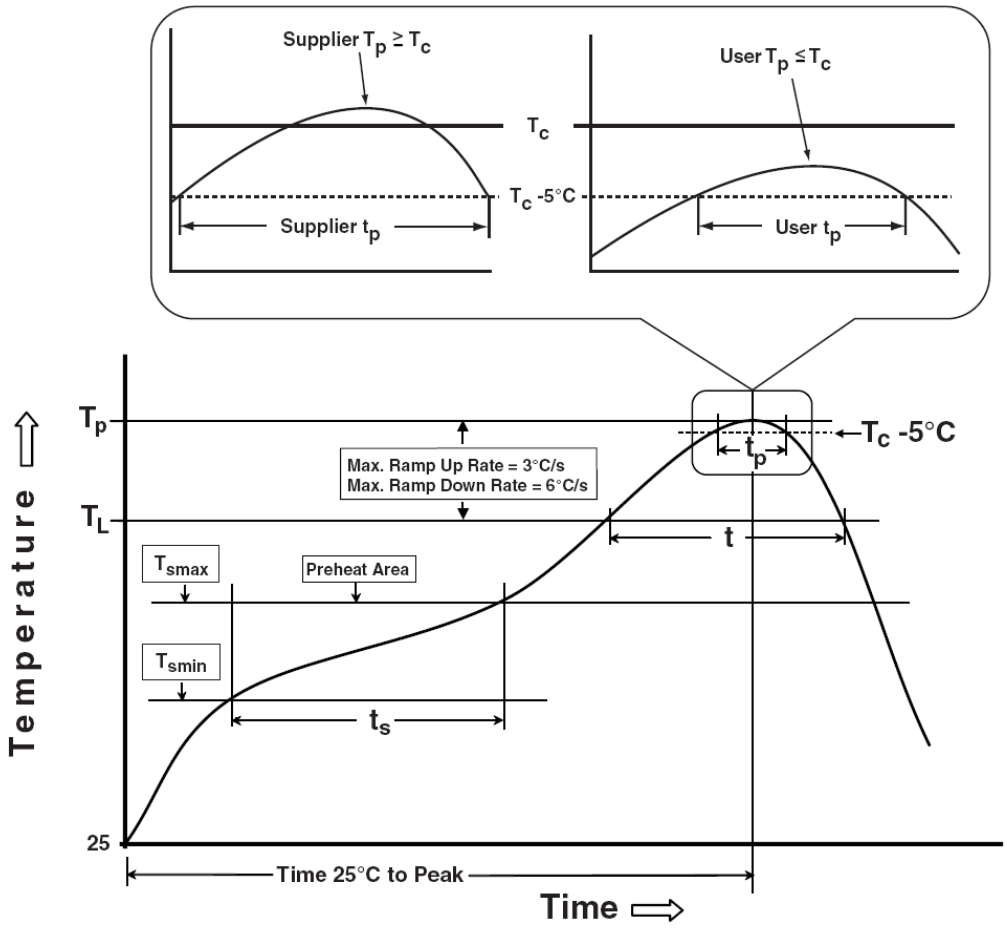
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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