

## Synchronous single PWM Controller with Multiform supply Voltage

### Features

- Adjustable Output Voltage from +0.8V to +5.0V
- 0.8V Reference Voltage
- $\pm 0.6\%$  Accuracy
- Operates from An Input Battery Voltage Range of +4V to +25V
- Multiform Purpose Input Voltage Collocation
- $V_{CC}=5V / V_{IN}=8\sim 19V$  For NB application
- $V_{CC}=5\sim 12V / V_{IN}=5\sim 12V$  For table PC application
- Power-On-Reset Monitoring on  $V_{CC}$  pin
- Excellent line and load transient responses
- Ultrasonic Operation Eliminated Audio Noise
- PFM mode for increased light load efficiency
- 300kHz Constant PWM Switching Frequency
- Integrated MOSFET Drivers
- Integrated Bootstrap Forward P-CH MOSFET
- Integrated Soft-Start Function
- Power Good Monitoring
- 70% Under-Voltage Protection
- 125% Over-Voltage Protection
- Adjustable Current-limit protection
- Using Sense Low-Side MOSFET's  $R_{DS(ON)}$
- Over-Temperature Protection
- TDFN3x3-10 package
- Lead Free and Green Devices Available (RoHS Compliant)

### Applications

- Notebook
- Table PC
- Hand-Held Portable
- AIO PC
- Wide input DC/DC Regulators

### General Description

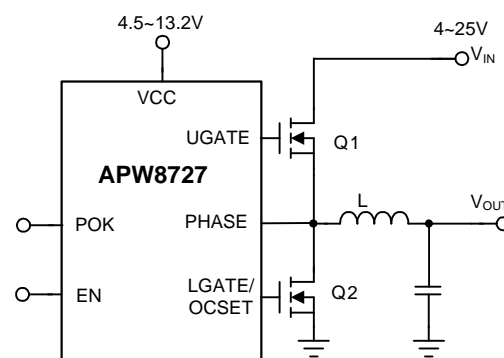
The APW8727 is a single-phase, constant on-time, synchronous PWM controller, which drives N-channel MOSFETs. The APW8727 steps down high voltage to generate low-voltage chipset, RAM supplies in notebook computers or motherboard applications.

The APW8727 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8727 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements. The unique ultrasonic mode maintains the switching frequency above 37kHz, which eliminates noise in audio application.

The APW8727 is equipped with accurate positive current limit, output under-voltage, and output over-voltage protections, perfect for multiform applications. The Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The APW8727 has an internal 2ms digital soft start that ramps up the output voltage with programmable slew rate to reduce the start-up current. The enable function can let user easy to apply APW8727.

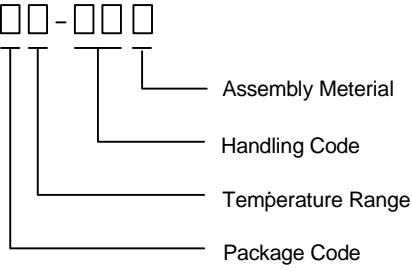
The APW8727 is available in 10pin TDFN 3x3 package respectively.

### Simplified Application Circuit



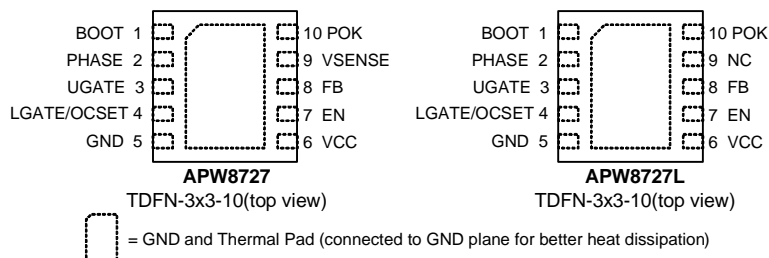
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

<p>APW8727/L <span style="border: 1px solid black; padding: 2px;">  </span> - <span style="border: 1px solid black; padding: 2px;">  </span> <span style="border: 1px solid black; padding: 2px;">  </span> <span style="border: 1px solid black; padding: 2px;">  </span></p>  <p>Assembly Material Handling Code Temperature Range Package Code</p>	<p>Package Code QB : TDFN3x3-10 Temperature Range I : -40 to 85 °C Handling Code TR : Tape &amp; Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APW8727 QB : <span style="border: 1px solid black; padding: 2px;">APW 8727 XXXXX</span></p>	<p>XXXXX - Date Code</p>
<p>APW8727L QB : <span style="border: 1px solid black; padding: 2px;">APW 8727L XXXXX</span></p>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration



## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{CC}$	VCC Supply Voltage (VCC to GND)	-0.3 ~ 16	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 44	V
$V_{BOOT}$	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 16	V
$V_{POK}$	POK Supply Voltage (POK to GND)	-0.3 ~ 16	V
	All Other Pins (EN, VSENSE and FB to GND)	-0.3~7	V

**Absolute Maximum Ratings (Cont.)** (Note 1)

Symbol	Parameter	Rating	Unit
	UGATE Voltage (UGATE to PHASE) <100ns pulse width >100ns pulse width	-3 ~ $V_{BOOT}+3$ -0.3 ~ $V_{BOOT}+0.3$	V
	LGATE Voltage (LGATE to GND) <100ns pulse width >100ns pulse width	-5 ~ $V_{CC}+5$ -0.3 ~ $V_{CC}+0.3$	V
$V_{PHASE}$	PHASE Voltage (PHASE to GND) <100ns pulse width >100ns pulse width	-5 ~ 35 -0.3 ~ 28	V
$T_J$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature	-65 ~ 150	°C
$T_{SDR}$	Maximum Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Thermal Characteristics**

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Thermal Resistance -Junction to Ambient (Note 2) TDFN3x3-10	55	°C/W

Note 2:  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

**Recommended Operating Conditions (Note 3)**

Symbol	Parameter	Range	Unit
$V_{IN}$	Converter Input Voltage	4 ~ 25	V
$V_{CC}$	VCC Supply Voltage	4.5 ~ 13.2	V
$V_{OUT}$	Converter Output Voltage	0.8~5	V
$I_{OUT}$	Converter Output Current	0 ~ 20	A
$T_A$	Ambient Temperature	-40 ~ 85	°C
$T_J$	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit for further information.

### Electrical Characteristics

These specifications apply for  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise stated. All typical specifications  $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V}$

Symbol	Parameter	Test Condition	APW8727			
			Min.	Typ.	Max.	Unit
<b>Reference VOLTAGE</b>						
$V_{REF}$	Reference Voltage		-	0.8	-	V
	Regulation Accuracy	$T_A = 25^{\circ}\text{C}$	-0.6	-	+0.6	%
$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ , Line / Load Transient		-1.0	-	+1.0	%	
$I_{FB}$	FB Input Bias Current	FB=0.8V	-	-	1	$\mu\text{A}$
<b>SUPPLY CURRENT</b>						
$I_{VCC}$	VCC Input Bias Current	VCC Current, EN=5V, $V_{FB}=0.9\text{V}$ , PHASE=0.5V	-	2	3	mA
$I_{VCC\_SHDN}$	VCC Shutdown Current	EN=GND, VCC=5V	-	15.3	20	$\mu\text{A}$
<b>SWITCHING FREQUENCY AND DUTY</b>						
$T_{ON}$	PWM On Time	$V_{IN}=12\text{V}$ , $V_{OUT}=1\text{V}$	222	278	333	ns
$T_{OFF(MIN)}$	Minimum off time	$V_{FB}=0.75\text{V}$ , $V_{PHASE}=-0.1\text{V}$	300	400	500	ns
	Minimum Ultrasonic Skip Operating Frequency		25	37	-	kHz
<b>Power On Timing</b>						
	OCP Threshold Setting Time	When set the max. value	-	950	-	$\mu\text{s}$
$T_{SS}$	Internal Soft Start Time	$V_{OUT}=0\%$ to $V_{OUT}$ Regulation (95%)	-	2	-	ms
<b>GATE DRIVER</b>						
	5V UG Source current	VCC=5V, BOOT-UG=5V	-	1.5	-	A
	5V UG Sink Resistance	VCC=5V, UG-PHASE=1V	-	1.4	-	$\Omega$
	5V LG Source current	VCC=5V, VCC-LG=5V	-	1.5	-	A
	5V LG Sink Resistance	VCC=5V, LG-GND=1V	-	1.0	-	$\Omega$
	UG to LG Dead time	UG falling to LG rising at VCC=5V	-	40	-	ns
		UG falling to LG rising at VCC=12V	-	20	-	ns
	LG to UG Dead time	LG falling to UG rising at VCC=5V	-	40	-	ns
		LG falling to UG rising at VCC=12V	-	20	-	ns
<b>BOOTSTRAP SWITCH</b>						
$V_F$	Bootstrap Forward Voltage	$V_{VCC} - V_{BOOT-GND}$ , $I_F = 10\text{mA}$	-	0.2	0.4	V
$I_R$	Reverse Leakage	$V_{BOOT-GND} = 30\text{V}$ , $V_{PHASE} = 25\text{V}$ , $V_{VCC} = 5\text{V}$	-	-	0.5	$\mu\text{A}$

**Electrical Characteristics (Cont.)**

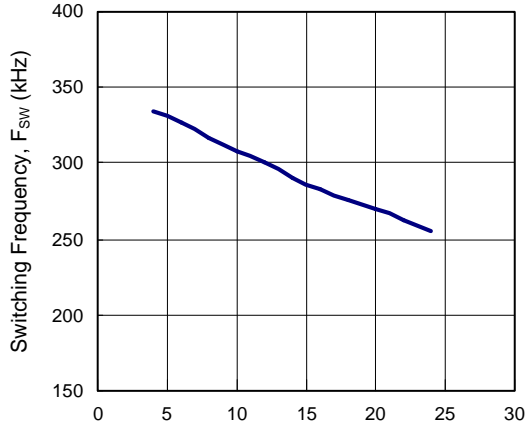
These specifications apply for  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise stated. All typical specifications  $T_A = +25^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V}$

Symbol	Parameter	Test Condition	APW8727			
			Min.	Typ.	Max.	Unit
<b>VCC POR THRESHOLD</b>						
$V_{VCC\_THR}$	Rising VCC POR Threshold Voltage		4.25	4.35	4.45	V
	VCC POR Hysteresis		-	300	-	mV
<b>CONTROL INPUTS</b>						
	EN Threshold	Shutdown	-	-	0.85	V
		Enable	1.3	-	-	
	EN Leakage	EN=5V	-	0.1	1.0	$\mu\text{A}$
<b>POWER-OK INDICATOR</b>						
$V_{POK}$	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK out from normal falling (POK Goes Low)	65	70	75	%
		POK out from normal rising (POK Goes Low)	120	125	130	%
$I_{POK}$	POK Leakage Current	$V_{POK}=5\text{V}$	-	0.1	1	$\mu\text{A}$
	POK Sink Current	$V_{POK}=0.5\text{V}$	5	15	-	mA
	POK Enable Delay Time	$V_{OUT}$ from 0% to POK High	-	2.5	-	ms
<b>CURRENT SENSE</b>						
$I_{OCSET}$	$I_{OCSET}$ OCP Threshold	$I_{OCSET}$ Sourcing	9.5	10	10.5	$\mu\text{A}$
$T_{CIOSET}$	$I_{OCSET}$ Temperature Coefficient	On The Basis of $25^{\circ}\text{C}$		2780		ppm/ $^{\circ}\text{C}$
$V_{ROCSET}$	Maximum Current Limit Threshold	$R_{OCSET}$ open	-	640	-	mV
	Zero Crossing Comparator Offset	$V_{GND-PHASE}$ Voltage	-3	0	3	mV
<b>PROTECTION</b>						
$V_{UV}$	UVP Threshold		65	70	75	%
	UVP Debounce Time		-	30	-	$\mu\text{s}$
	UVP Enable Delay	$V_{OUT}$ from 0% to UVP enable	-	2.5	-	ms
$V_{OVR}$	OVP Rising Threshold	$V_{FB}$ rising, LG fully turn on	120	125	130	%
	OVP Propagation Delay	$V_{FB}$ Rising	-	2	-	$\mu\text{s}$
$T_{OTR}$	OTP Rising Threshold (Note 4)		-	150	-	$^{\circ}\text{C}$
	OTP Hysteresis (Note 4)		-	25	-	$^{\circ}\text{C}$

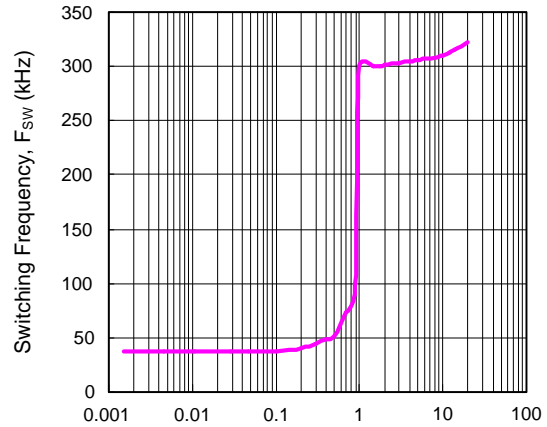
Note 4: Guaranteed by design.

Typical Operating Characteristics

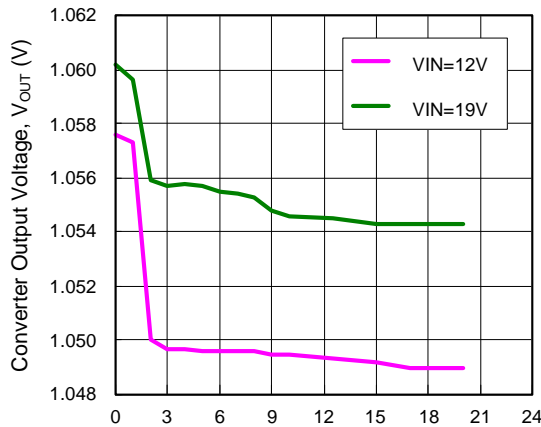
Switching Frequency vs. Converter Input Voltage



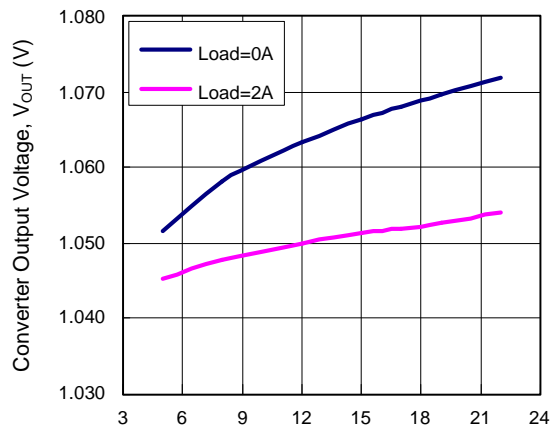
Switching Frequency vs. Converter Output Current



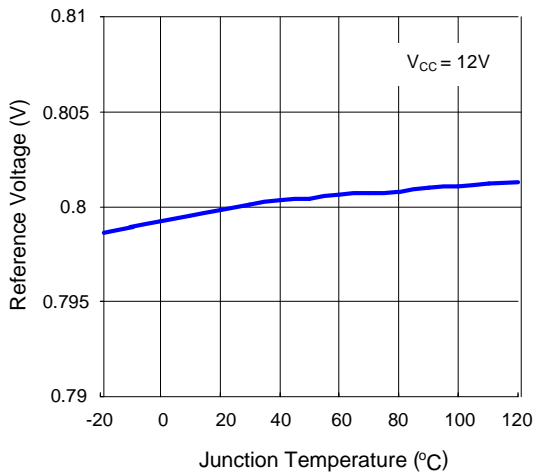
Converter Output Voltage vs. Converter Output Current



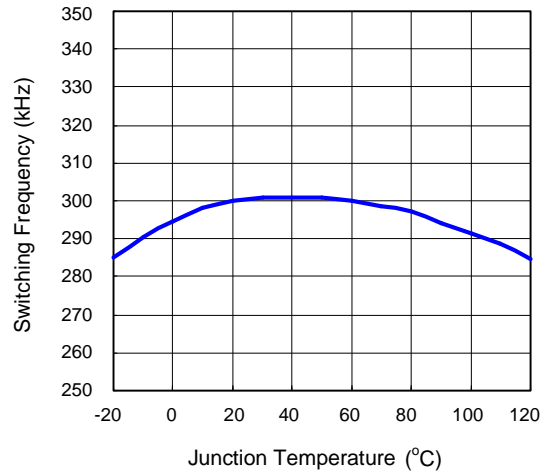
Converter Output Voltage vs. Converter Input Voltage



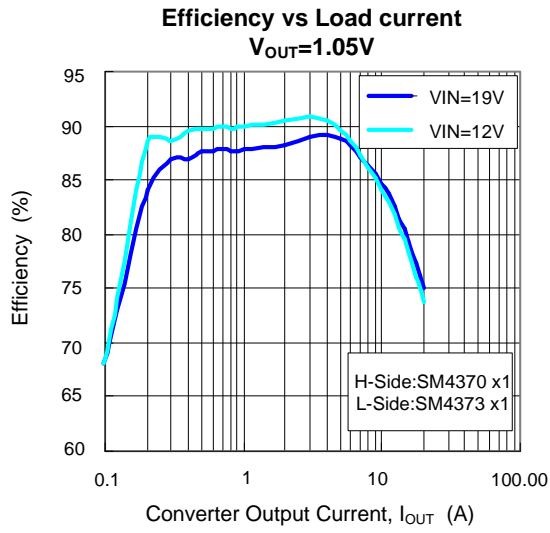
Reference Voltage vs. Junction Temperature



Switching Frequency vs. Junction Temperature

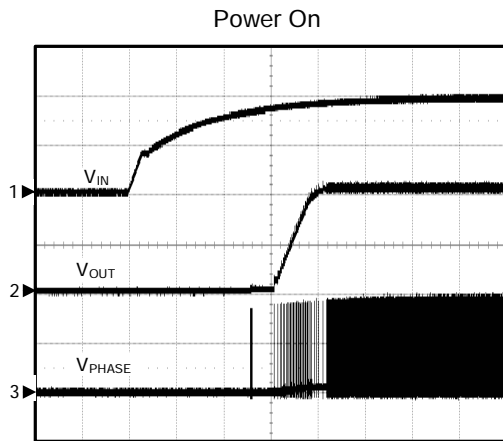


### Typical Operating Characteristics

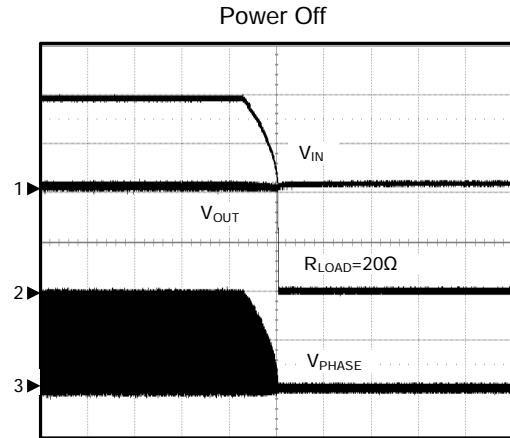


## Operating Waveforms

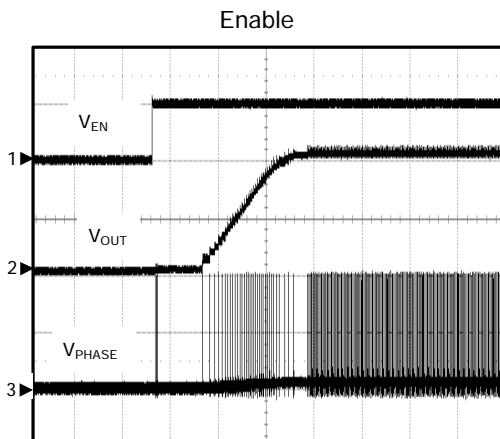
Refer to the typical application circuit. The test condition is  $V_{IN}=19V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.



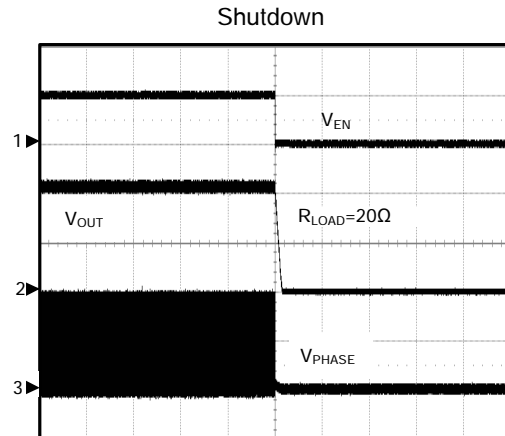
CH1:  $V_{IN}$ , 10V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 2ms/Div



CH1:  $V_{IN}$ , 10V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 20ms/Div



CH1:  $V_{EN}$ , 5V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 1ms/Div



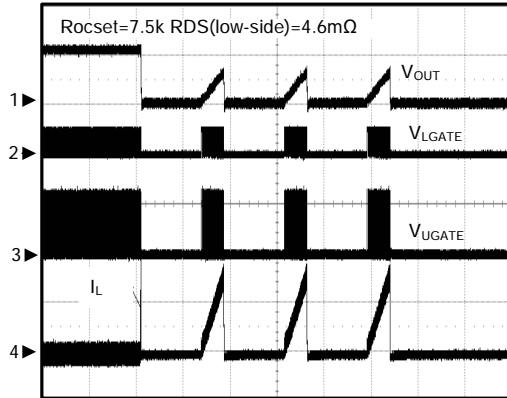
CH1:  $V_{EN}$ , 50V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 1ms/Div



## Operating Waveforms

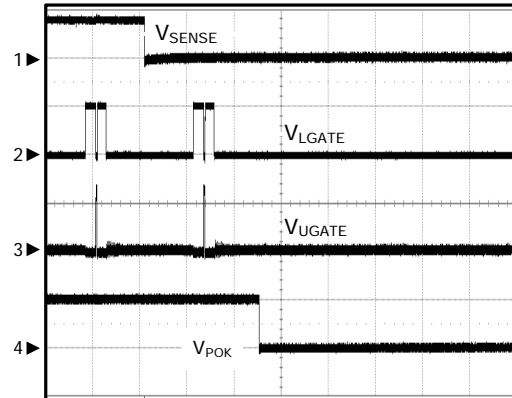
Refer to the typical application circuit. The test condition is  $V_{IN}=19V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

Over-Current Protection



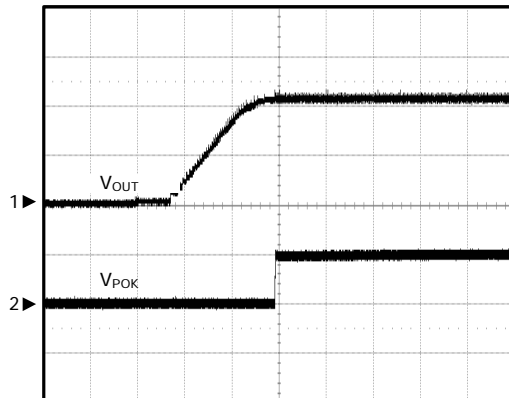
CH1:  $V_{OUT}$ , 10V/Div  
 CH3:  $V_{LGATE}$  10V/Div  
 CH3:  $V_{UGATE}$  20V/Div  
 CH3:  $I_L$ , 10A/Div  
 TIME: 2ms/Div

Under-Voltage Protection



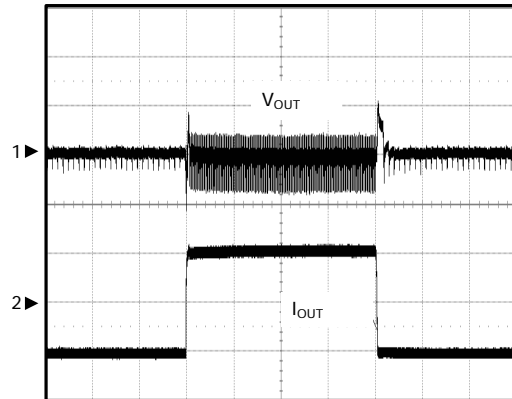
CH1:  $V_{sense}$ , 500mV/Div  
 CH3:  $V_{LGATE}$  5V/Div  
 CH3:  $V_{UGATE}$  20V/Div  
 CH3:  $V_{POK}$ , 5V/Div  
 TIME: 10us/Div

POWER OK



CH1:  $V_{OUT}$ , 500mV/Div  
 CH2:  $V_{POK}$ , 5V/Div  
 TIME: 20ms/Div

Load Transient

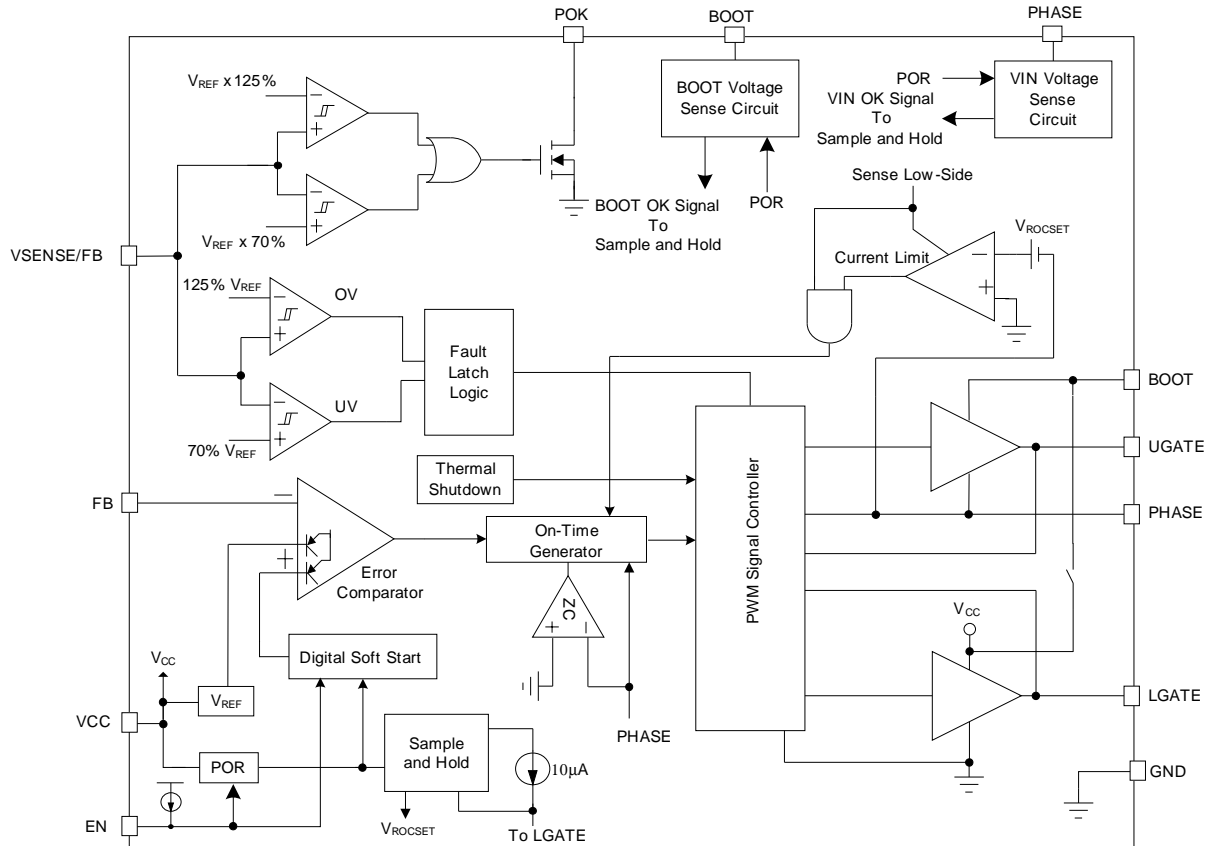


CH1:  $V_{OUT}$ , 50mV/Div  
 CH2:  $I_{OUT}$ , 5A/Div  
 TIME: 200us/Div

## Pin Description

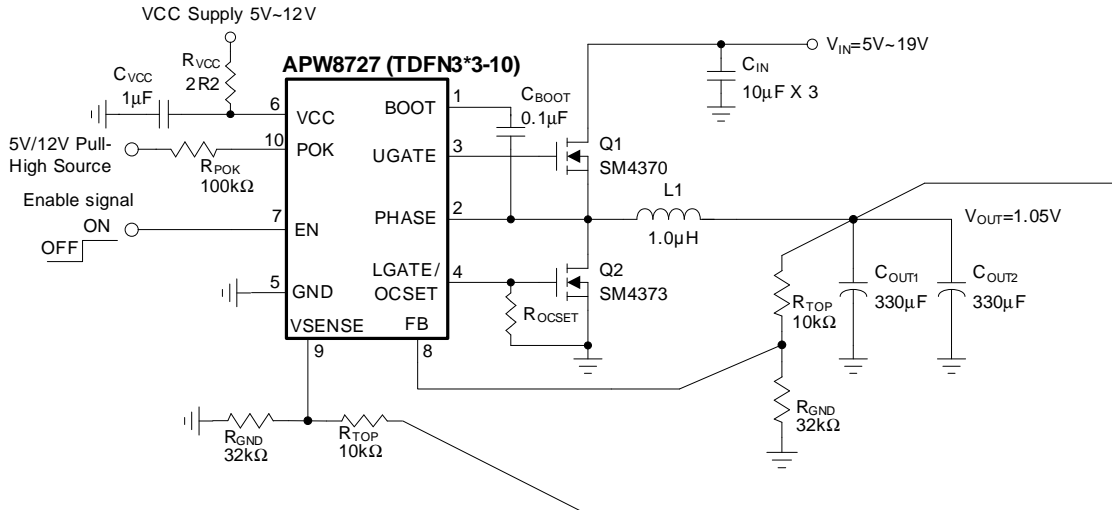
PIN		Name	FUNCTION
No.			
APW8727	APW8727L		
1	1	BOOT	Supply Input for The UGATE Driver and An Internal Level-shift Circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
2	2	PHASE	Junction Point of The High-side MOSFET Source, Output Filter Inductor and The Low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UG high-side gate driver.
3	3	UGATE	Output of The High-side MOSFET Driver. Connect this pin to Gate of the high-side MOSFET.
4	4	LGATE/OCSET	Output of The Low-side MOSFET Driver And Current-Limit Setting Input. Connect this pin to Gate of the low-side MOSFET. There is an internal source current 10 $\mu$ A through a resistor from LGATE/OCSET pin to GND before power on. This action is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current limit.
5	5	GND	Signal Ground for The IC
6	6	VCC	Supply Voltage Input Pin for Control Circuitry. Connect +5V~+12V from the VCC pin to the GND. Decoupling at least 1 $\mu$ F of a MLCC capacitor from the VCC pin to the GND.
7	7	EN	Enable/Shutdown Pin. When EN=1, enable the PWM controller, EN=0, shutdown the PWM controller. When the EN is floating, it will pull up to high logic automatically.
8	8	FB	Output Voltage Feedback Pin. This pin is connected to the resistive divider in remote side that set the desired output voltage. In APW8727L, The POK, UVP, and OVP circuits detect this signal to report output voltage status.
9	-	VSENSE	Output Voltage Sense Pin. It is used to sense the output voltage. The VSENSE pin is the input of over-voltage, under-voltage and POK detecting comparator. Connect a resistor diver from output to GND to set the OVP and UVP thresholds. VSENSE should not be left floating.
-	9	NC	No Connect
10	10	POK	Power Good Output. POK is an open drain output used to indicate the status of the output voltage. Connect the POK in to +5V~+12V through a pull-high resistor.
Exposed pad	Exposed pad	GND	Signal Ground for The IC

Block Diagram

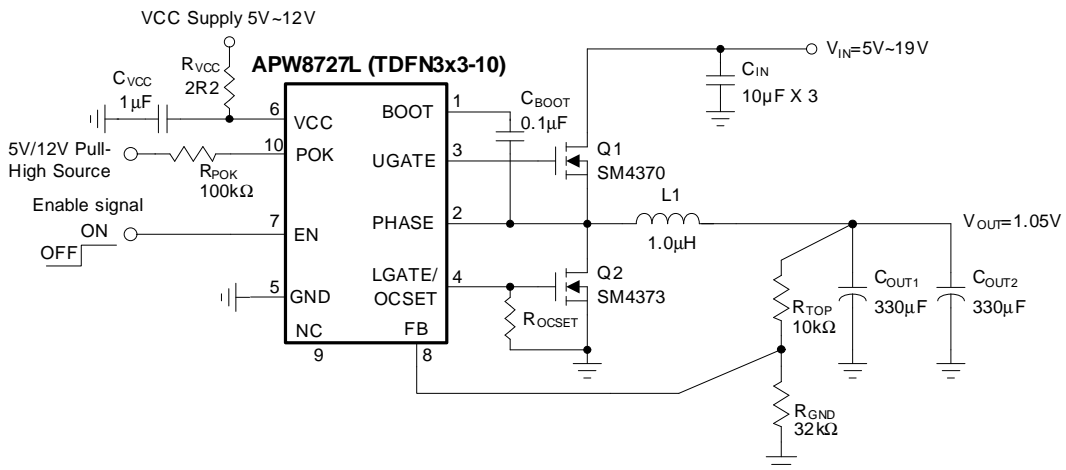


## Typical Application Circuit

Circuit 1



Circuit 2



## Function Description

### Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudofixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a oneshot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (400ns, typical). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time oneshot has timed out.

### Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{\text{ON-PFM}} = \frac{1}{F_{\text{SW}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Where  $F_{\text{SW}}$  is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$\begin{aligned} I_{\text{LOAD(PFM to PWM)}} &= \frac{1}{2} \times \frac{V_{\text{IN}} - V_{\text{OUT}}}{L} \times T_{\text{ON-PFM}} \\ &= \frac{V_{\text{IN}} - V_{\text{OUT}}}{2L} \times \frac{1}{F_{\text{SW}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} \end{aligned}$$

### Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising VCC POR Threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. There is a hysteresis to POR voltage threshold (about 300mV typical). When VCC voltage drops lower than 4.05V (typical), the POR disables the chip.

### EN Pin Control

When  $V_{\text{EN}}$  is above the EN high threshold (1.3V, minimum), the converter is enabled. When  $V_{\text{EN}}$  is below the EN low threshold (0.85V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC. When EN pin is in float state, it will pull up high logic automatically.

### Digital Soft-Start

The APW8727 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 2ms (typical) and independent of the UGATE switching frequency.

## Function Description (Cont.)

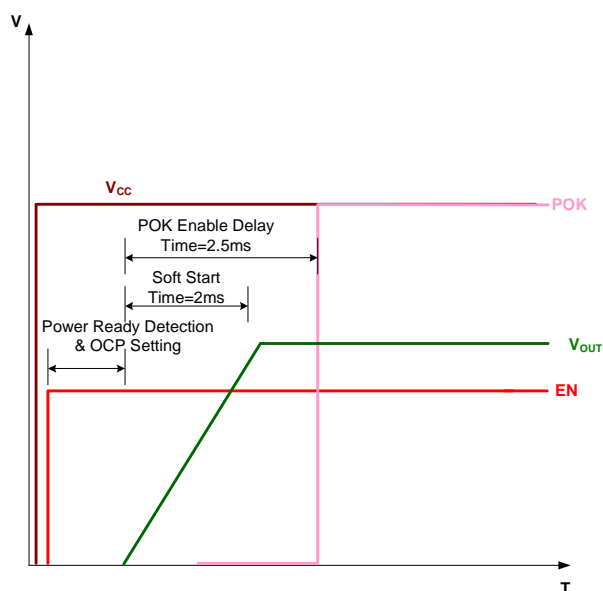


Figure 1. Soft-Start Sequence

During soft-start stage before the PGOOD pin is ready, the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage equals to the  $V_{FB}$  voltage. This will ensure that the output voltage starts from its existing voltage level.

### Power OK Indicator

The APW8727 features an open-drain POK pin to indicate output regulation status. In normal operation, when the output voltage rises 90% of its target value, the POK goes high. When the output voltage outruns 70% or 125% of the target voltage, POK signal will be pulled low immediately.

In APW8727L, since the FB pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the FB pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false POK from dropping, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

### Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the VSENSE voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the under-voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After  $30\mu\text{s}$  debounce time, the device turns off both high-side and low-side MOSFET with latched. Toggling enable pin to low or recycling VCC, will clear the latch and bring the chip back to operation. In APW8727L, the FB pin is also used for monitoring this function.

### Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by VSENSE pin. When the VSENSE voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator designed with a  $2\mu\text{s}$  noise filter will force the low-side MOSFET gate driver fully turn on and latch high. This action actively pulls down the output voltage.

This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN, VCC power-on-reset signal. In APW8727L, the FB pin is also used for monitoring this function.

## Function Description (Cont.)

### Over-Current Protection of the PWM Converter

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during it's on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor ( $R_{OCSET}$ ), connected from the LGATE/OCSET to GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source,  $I_{OCSET}$  (10 $\mu$ A typical), flowing through the  $R_{OCSET}$  develops a voltage ( $V_{ROCSET}$ ) across the  $R_{OCSET}$ . The device holds  $V_{ROCSET}$  and stops the current source  $I_{OCSET}$  during normal operation. When the voltage across the low-side MOSFET exceeds the  $V_{ROCSET}$ , the APW8750 shuts off the converter and then initiates a new soft-start process. The device turns off both high-side and low-side MOSFETs and the converter's output is latched to be floating.

The APW8750 has an internal OCP voltage,  $V_{OCP\_MAX}$ , and the value is 0.7V (typical). When the  $R_{OCSET} \times I_{OCSET}$  exceed 0.64V or the  $R_{OCSET}$  is floating or not connected, the  $V_{ROCSET}$  will be the default value 0.7V. The over current threshold would be 0.7V across low-side MOSFET. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low - side)}$$

For the over-current is never occurred in the normal operating load range, the variation of all parameters in the above equation should be considered:

- The  $R_{DS(ON)}$  of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum  $R_{DS(ON)}$  by using the manufacturer's datasheet.
- The minimum  $I_{OCSET}$  (9.5 $\mu$ A) and minimum  $R_{OCSET}$  should be used in the above equation.
- Note that the  $I_{LIMIT}$  is the current flow through the low-side MOSFET;  $I_{LIMIT}$  must be greater than peak inductor current which is output current add the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} + \frac{\Delta I}{2}$$

Where  $\Delta I$  = output inductor ripple current

- The overshoot and transient peak current also should be considered.

### Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature  $T_{OTR}$ , the IC will enter the over-temperature protection state that suspends the PWM, which forces the UGATE and LGATE gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 25°C. The OTP is designed with a 25°C hysteresis to lower the average  $T_J$  during continuous thermal overload conditions, which increases lifetime of the APW8750.

### The On-Time Control and PWM Switching Frequency

The APW8750 does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage  $V_{OUT}$  and inverses proportional to input voltage  $V_{IN}$ . When  $V_{IN}$  is 12V,  $V_{OUT}$  is 1V, the switching frequency is 300kHz at PWM operation.

APW8750 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring  $V_{PHASE}$  voltage as input voltage to calculate on-time when the high-side MOSFET is turned on.

### Droop

As shown in figure 2, connect the DROOP pin a resistor to REFOUT. It can adjust reference voltage As shown in the following equation:

$$I_{SENSE} = \Delta PHASE \times gm$$

$$V_{DROOP} = I_{SENSE} \times R_{DROOP}$$

## Application Information

### Output Voltage Setting

The output voltage is adjustable from 0.8V to 5V with a resistor-divider connected with FB, GND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.8 \times \left( 1 + \frac{R_{TOP}}{R_{GND}} \right)$$

Where 0.8 is the reference voltage,  $R_{TOP}$  is the resistor connected from converter's output to FB, and  $R_{GND}$  is the resistor connected from FB to GND. Suggested  $R_{GND}$  is in the range from 1k to 20k $\Omega$ . To prevent stray pickup, locate resistors  $R_{TOP}$  and  $R_{GND}$  close to APW8727.

### Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current,  $I_{RIPPLE}$ , and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where  $F_{SW}$  is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency ( $F_{SW}$ ) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into

saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

### Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop  $\Delta V_{COUT}$  and ESR voltage drop  $\Delta V_{ESR}$  caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8C_{OUT}F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1 $\mu$ F) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

### Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times



## Application Information (Cont.)

### Input Capacitor Selection (Cont.)

higher than the maximum input voltage. The maximum RMS current rating requirement is approximately  $I_{OUT}/2$ , where  $I_{OUT}$  is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

### MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the  $R_{DS(ON)}$  of the MOSFET:

For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.

In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high  $dv/dt$  of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller  $R_{DS(ON)}$  of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually the secondary consideration. The high-side MOSFET does not have this zero voltage switching condition; in addition, because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the  $R_{DS(ON)}$ , reversing transfer capacitance ( $C_{RSS}$ ) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{\text{high-side}} = I_{OUT}^2 (1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{\text{low-side}} = I_{OUT}^2 (1+TC)(R_{DS(ON)})(1-D)$$

Where

$I_{OUT}$  is the load current

TC is the temperature dependency of  $R_{DS(ON)}$

$F_{SW}$  is the switching frequency

$t_{SW}$  is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval,  $t_{SW}$ , is the function of the reverse transfer capacitance  $C_{RSS}$ . The (1+TC) term is a factor in the temperature dependency of the  $R_{DS(ON)}$  and can be extracted from the " $R_{DS(ON)}$  vs. Temperature" curve of the power MOSFET.

### Layout Consideration

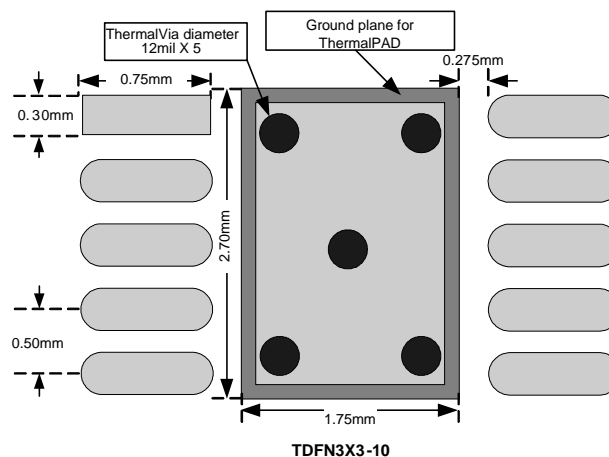
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, BOOT, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with these traces on any layer.

## Application Information (Cont.)

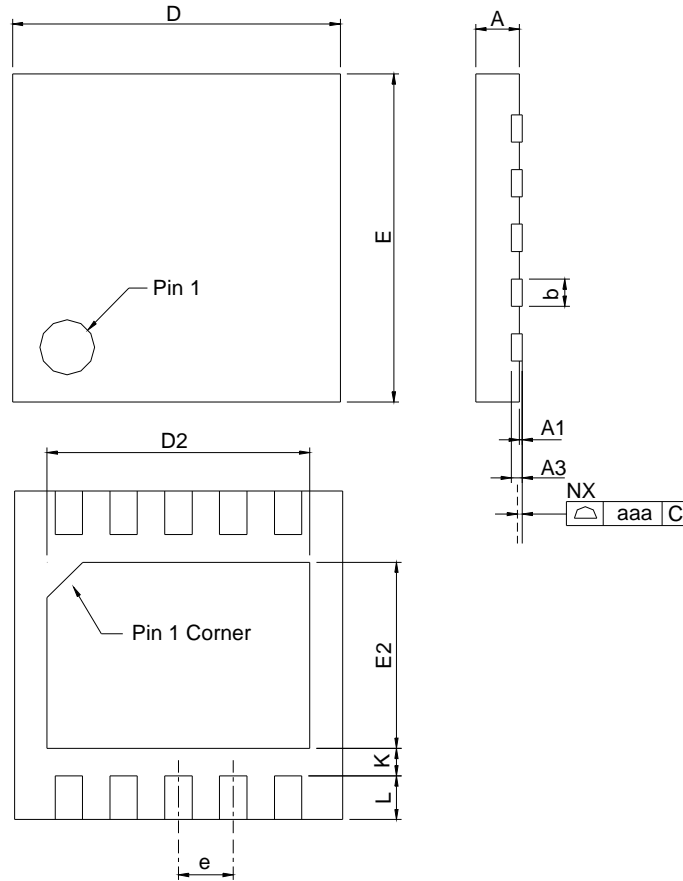
### Layout Consideration (Cont.)

- The signals going through these traces have both high  $dv/dt$  and high  $di/dt$  with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs ( $V_{IN}$  and PHASE nodes) can get better heat sinking.
- The GND is the current sensing circuit reference ground and also the power ground of the LGATE low-side MOSFET. On the other hand, the GND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UGATE, LGATE, BOOT, and PHASE).



Package Information

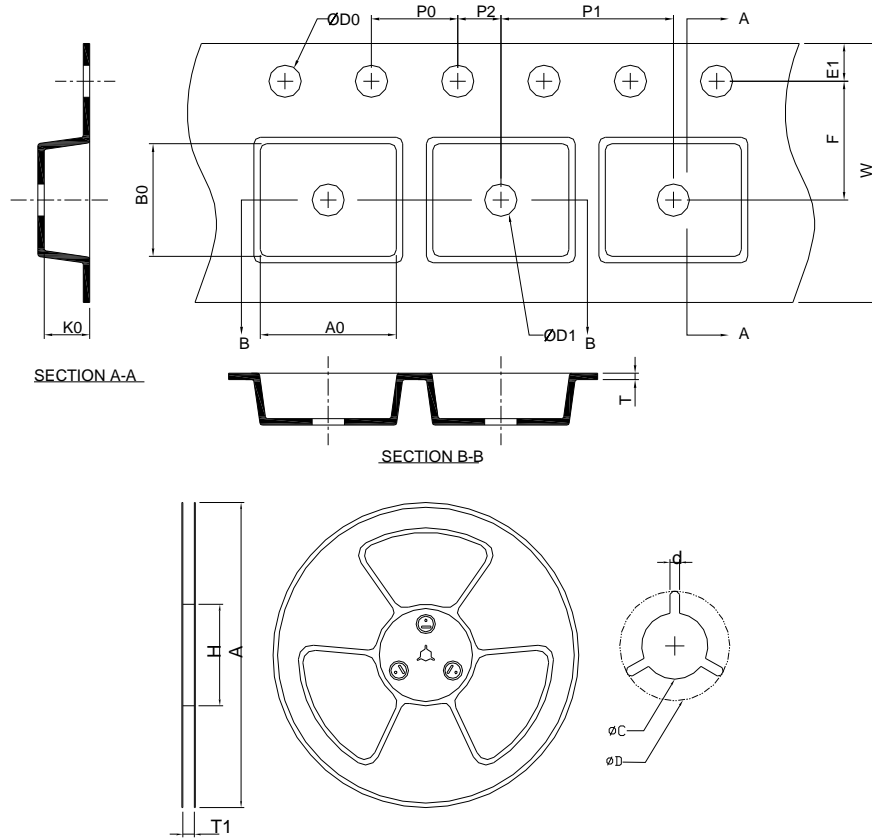
TDFN3x3-10



DIMENSIONS	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

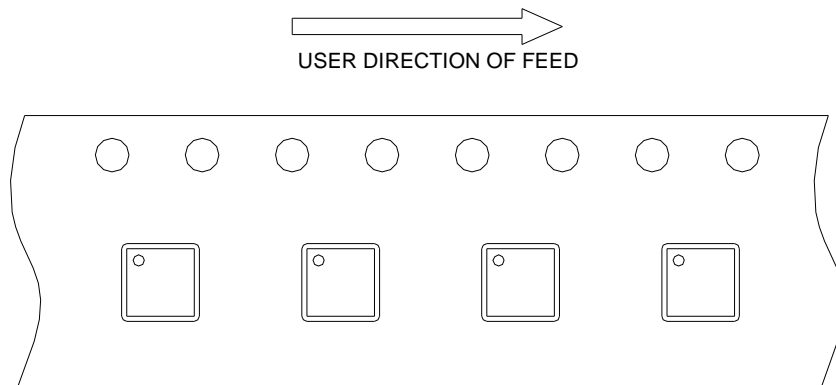
(mm)

Devices Per Unit

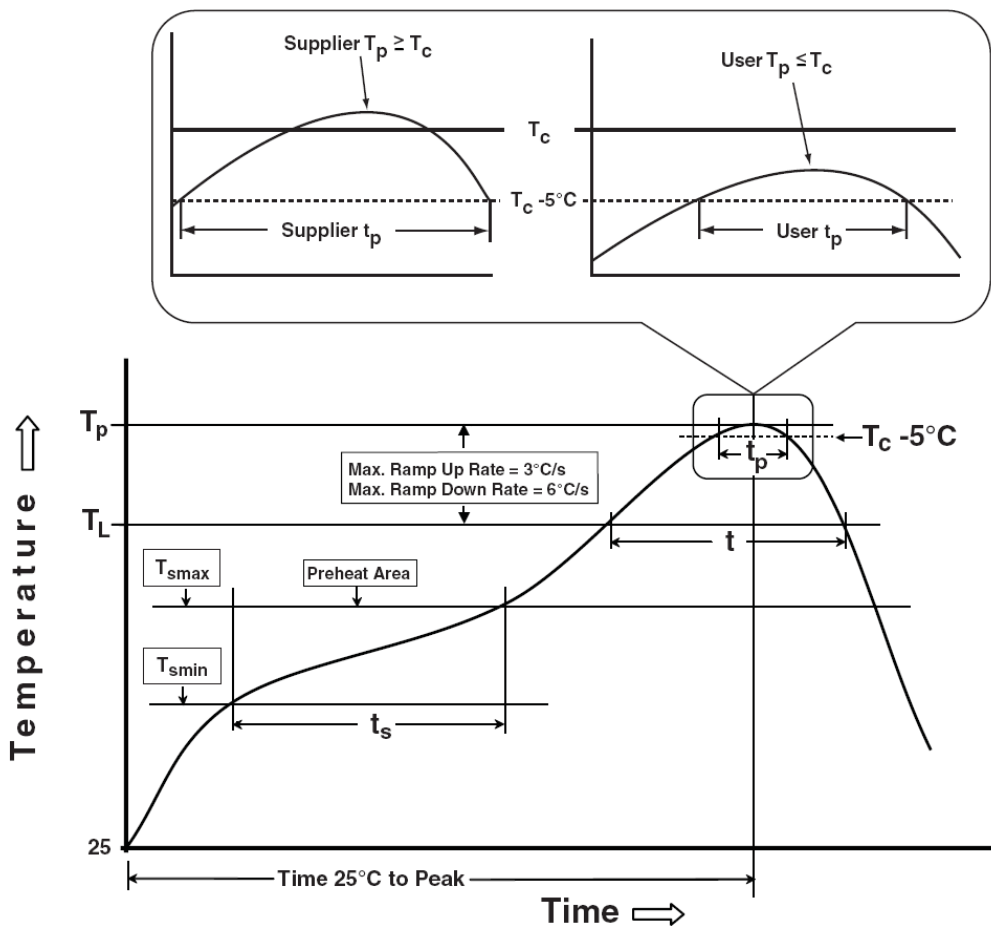
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

### Taping Direction Information

TDFN3x3-10



### Classification Profile



**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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