Source and Sink, 2A, Fast Transient Response Linear Regulator

Features

- Provide Bi-direction Currents
  - Sourcing or Sinking Current Up to 2A
- Built-in Soft-Start
- Power-On-Reset Monitoring on VCNTL Pins
- Fast Transient Resoponse
- Stable with Ceramic Output Capacitors
- ±10mV High System Output Accuracy Over Load and Temperature Ranges
- Adjustable Output Voltage by External Resistors
- Current-Limit Protection
- On-Chip Thermal Shutdown
- Shutdown for Standby or Suspend Mode
- Compact TDFN3x3-10 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- DDRII/III/IV SDRAM Termination Voltage
- Motherboard and VGA Card Power Supplies
- Setop Box
- Low Power DDRIII/IV

General Description

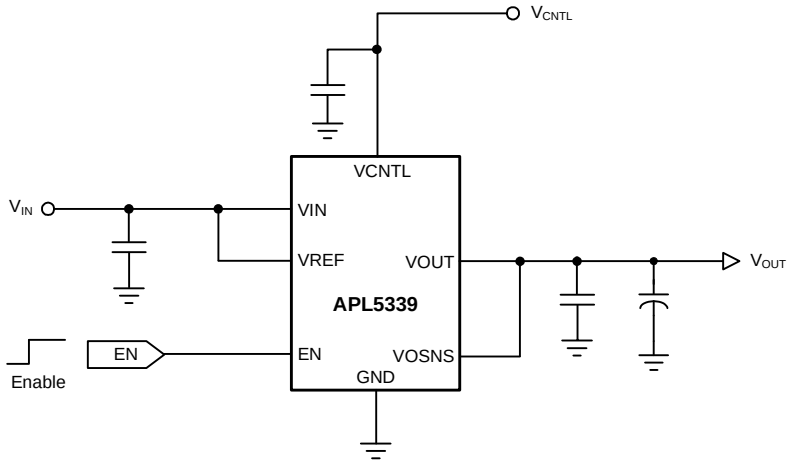
The APL5339 linear regulator is designed to provide a regulated voltage with bi-direction output current for DDR-SDRAM termination voltage. The APL5339 integrates two power transistors to source or sink load current up to 2A. It also features internal soft-start, current-limit, thermal shutdown and enable control functions into a single chip. The internal soft-start controls the rising rate of the output voltage to prevent inrush current during start-up. The current-limit circuit detects the output current and limits the current during short-circuit or current overload conditions. The on-chip thermal shutdown provides thermal protection against any combination of overload that would create excessive junction temperatures.

The output voltage of APL5339 is regulated to track the voltage on half voltage of VREF. An internal resistor divider is used to provide a half voltage of VREF for VOUT Voltage. The VOUT output voltage is only requiring 10µF of ceramic output capacitance for stability and fast transient response.

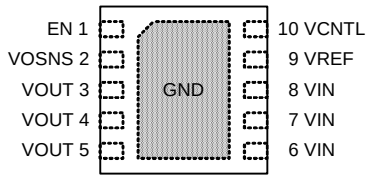
Pulling and holding the voltage on voltage of EN below the enable voltage threshold shuts off the output.

The APL5339 is available in TDFN3x3-10 package.

Simplified Application Circuit



Pin Configuration



TDFN3X3-10
(Top View)

= Exposed Pad
(connected to ground plane for better heat dissipation)

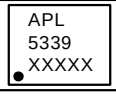
Ordering and Marking Information

APL5339 □□ – □□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB : TDFN3x3-10
Operating Junction Temperature
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL5339 QB:



X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 7	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 4	V
V_{REF}	VREF Input Voltage (VREF to GND)	-0.3 ~ 7	V
V_{OSNS}	VOSNS Input Voltage (VOSNS to GND)	-0.3 ~ 7	V
V_{OUT}	VOUT Output Voltage (VOUT to GND)	-0.3 ~ V_{IN}+0.3	V
V_{EN}	EN to GND Voltage	-0.3 ~ V_{CNTL}+0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TDFN3x3-10	60	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage (Note 4)	3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage	1.0 ~ 3.6	V
V_{REF}	VREF Input Voltage (Note 5)	0 ~ V_{IN}	V
V_{OUT}	VOUT Output Voltage (V_{CNTL} - V_{OUT} > 2.3V for I_{OUT} = 2A, T_J=25°C)	0.5xV_{REF} ~ V_{IN} – V_{DROP}	V
I_{OUT}	VOUT Output Current (Note 6)	-2 ~ +2	A
C_{IN}	Capacitance of Input Capacitor	10 ~ 100	µF
	Equivalent Series Resistor (ESR) of Input Capacitor	0 ~ 200	mΩ
C_{OUT}	Capacitance of Output Multi-layer Ceramic Capacitor (MLCC)	8 ~ 47	µF
	Total Output Capacitance (Note 7)	10 ~ 820	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Note 4: The voltage of VCNTL must be higher than the voltage of VOUT pin.

Note 5: The voltage of VREF should not be higher than the voltage of VIN when the regulator be enabled.

Note 6: The symbol "+" means the VOUT sources current to load; the symbol "-" means the VOUT sinks current from load to GND.

Note 7: It is necessary to use a multi-layer ceramic capacitor 8µF at least as an output capacitor. Please place the ceramic capacitor near VOUT pin as close as possible. Besides, the other kinds of capacitors (like Electrolytic, PoSCap, tantalum capacitors) can be used as the output capacitors in parallel.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CNTL}=5V, V_{IN}=1.8V, 1.5V or 1.35V, V_{REF}=V_{IN}, C_{IN}=10µF, C_{OUT}=10µF (MLCC) and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL5339			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{CNTL}	VCNTL Supply Current	V_{EN}=V_{CNTL}, I_{OUT}=0A	-	0.5	1	mA
I_{SD}	VCNTL Supply Current at Shutdown	V_{EN}=GND	-	15	30	µA
I_{VIN}	VIN Supply Current at Shutdown	V_{EN}=GND	-	-	1	µA
POWER-ON-RESET (POR)						
	Rising VCNTL POR Threshold	VCNTL Rising	2.3	2.6	2.9	V
	VCNTL POR Hysteresis		-	0.35	-	V
	Rising VIN POR Threshold	VIN Rising	0.4	0.6	0.8	V
	VIN POR Hysteresis		-	0.2	-	V

Electrical Characteristics(Cont.)

Unless otherwise specified, these specifications apply over V_{CNTL}=5V, V_{IN}=1.8V, 1.5V or 1.35V, V_{REF}=V_{IN}, C_{IN}=10µF, C_{OUT}=10µF (MLCC) and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

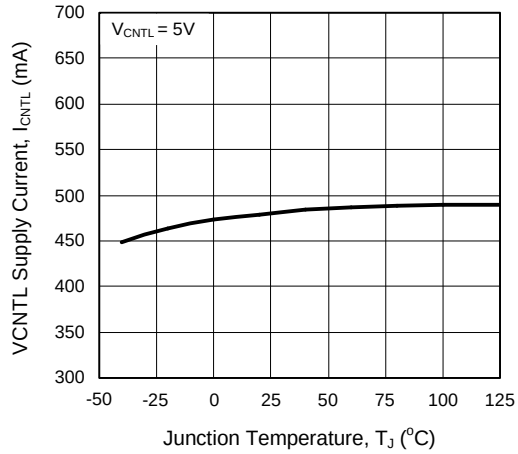
Symbol	Parameter	Test Conditions		APL5339			Unit
				Min	Typ	Max	
OUTPUT VOLTAGE							
V_{OUT}	VOUT Output Voltage			-	0.5	-	V_{REF}
	System Accuracy	Over Load, Offset and Temperature		-10	-	10	mV
	VOUT Discharge Current	V_{CNTL}=5V, V_{EN}=0V, V_{OUT}=0.1V		-	22	-	µA
	VOSNS Input Current	V_{OSNS}=V_{CNTL}		-100	-	+100	nA
	VREF Input Current	V_{REF}=5V		-	12.5	-	µA
ENABLE and INTERNAL SOFT-START							
V_{EN}	EN Logic Input Threshold	V_{CNTL}=3V~5.5V		0.5	0.8	1.1	V
	EN Hysteresis			-	0.1	-	V
I_{EN}	EN Pull-High Current	V_{EN}=GND		-	3.5	-	µA
t_{SS}	Internal Soft-Start Interval	V_{REF}=1.8V, V_{OUT}=10% to 90%, T_J=25 °C		0.1	0.25	0.4	ms
DROPOUT VOLTAGES							
V_{DROP}	VIN-to-VOUT Dropout Voltage	V_{CNTL}=5.0V, I_{OUT}=2 A, V_{OUT}=1.2V	T_J=25°C	-	0.34	0.41	V
			T_J=-40 °C ~125°C	-	-	0.55	V
PROTECTIONS							
I_{LIM}	Current Limit Level	Sourcing Current	T_J=25°C	2.6	3.4	4.2	A
			T_J=-40°C~125°C	2.2	-	-	A
		Sinking Current	T_J=25°C	-2.6	-3.4	-4.2	A
			T_J=-40°C ~ 125°C	-2.2	-	-	A
T_{SD}	Thermal Shutdown Temperature	T_J rising		-	170	-	°C
	Thermal Shutdown Hysteresis			-	50	-	°C

Pin Description

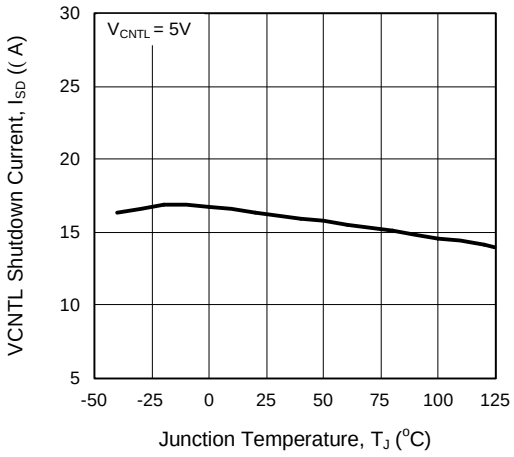
PIN		FUNCTION
NO.	NAME	
1	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When leave this pin open, an internal pull-up current (3μA typical) pulls the EN voltage and enables the regulator.
2	VOSNS	Output voltage feedback pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
3, 4, 5	VOUT	Output pin of the regulator. Connect this pin to load and output capacitors (8μF at least) required for stability and improving transient response. The output voltage is regulated to track the reference voltage and capable of sourcing or sinking current up to 2A. During shutdown, the output voltage is discharged by an internal pull-low MOSFET.
6, 7, 8	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The APL5339 sources current to VOUT pin by controlling the upper pass MOSFET, providing a current path from VIN pin.
9	VREF	Reference voltage input for VOUT regulator.
10	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
Exposed Pad	GND	Ground pin of the circuitry. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air. The APL5339 sinks current from VOUT pin by controlling the lower pass MOSFET, providing a current path to GND pin.

Typical Operating Characteristics

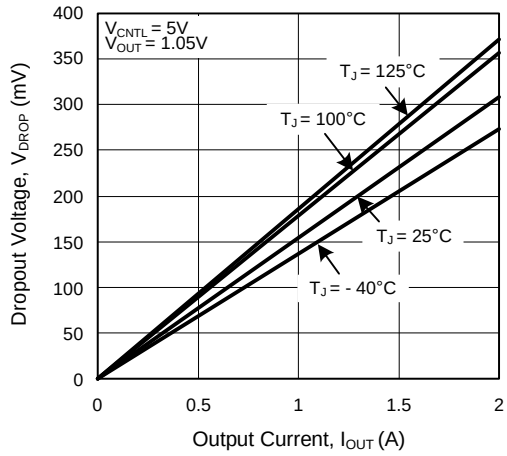
VCNTL Supply Current vs. Junction Temperature



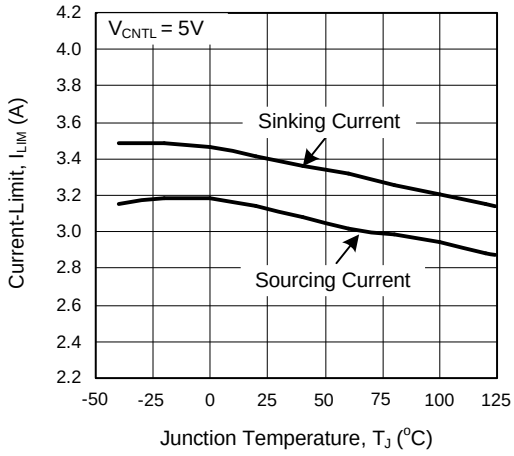
VCNTL Shutdown Current vs. Junction Temperature



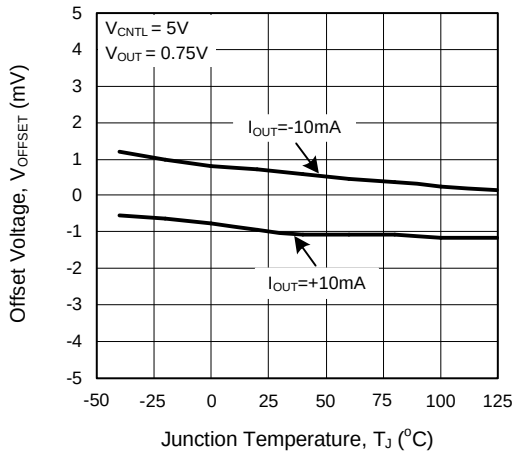
Dropout Voltage vs. Output Current



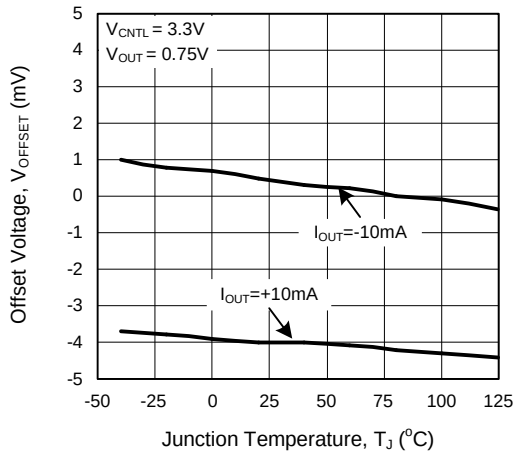
Current-Limit vs. Junction Temperature



Offset Voltage vs. Junction Temperature

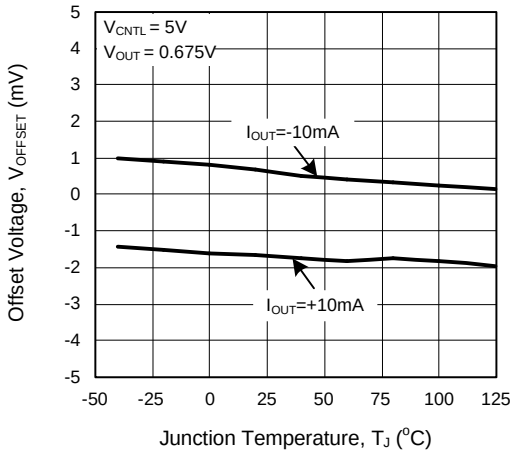


Offset Voltage vs. Junction Temperature

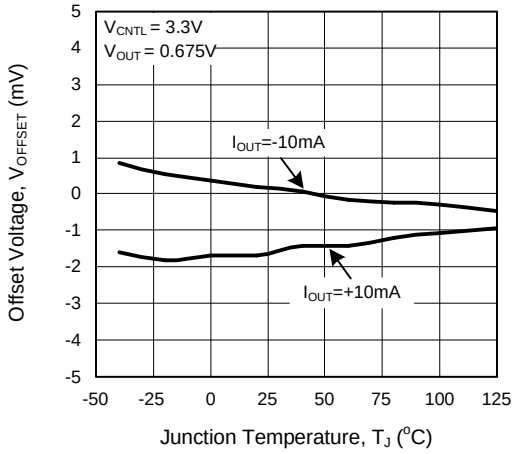


Typical Operating Characteristics (Cont.)

Offset Voltage vs. Junction Temperature



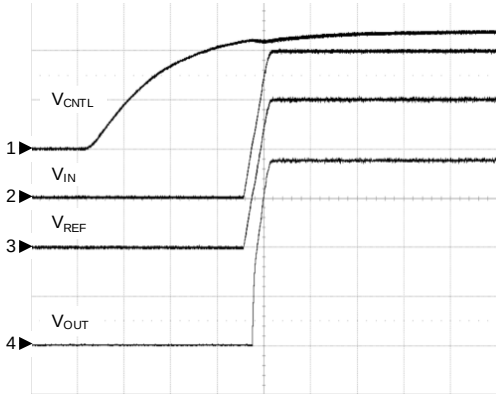
Offset Voltage vs. Junction Temperature



Operating Waveforms

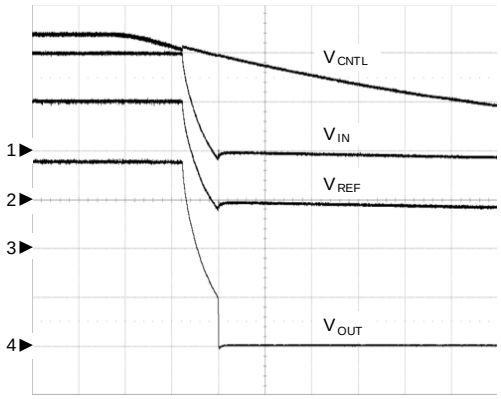
Refer to the typical application circuit. The test condition is V_{CNTL}=5V, T_A= 25°C unless otherwise specified.

Power On



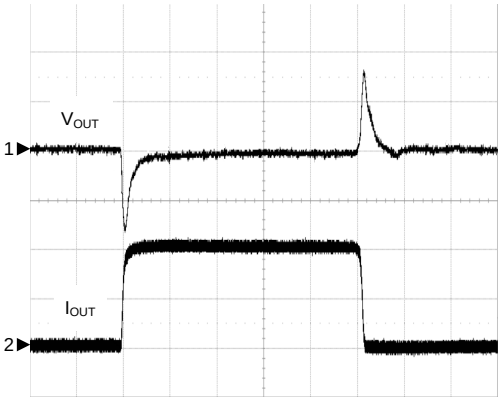
V_{CNTL}=5V, V_{IN}=1.5V, I_{OUT}=2A
CH1: V_{CNTL}, 2V/Div, DC
CH2: V_{IN}, 0.5V/Div, DC
CH3: V_{REF}, 0.5V/Div, DC
CH4: V_{OUT}, 0.2V/Div, DC
TIME: 2ms/Div

Power Off



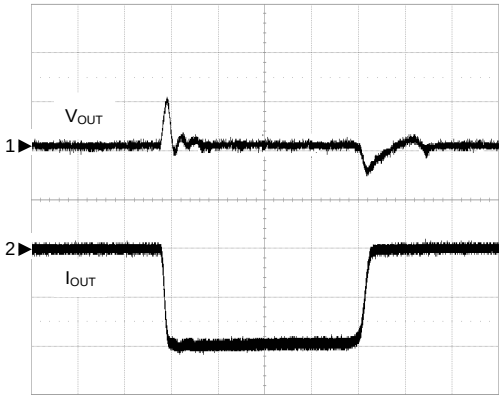
V_{CNTL}=5V, V_{IN}=1.5V, I_{OUT}=2A
CH1: V_{CNTL}, 2V/Div, DC
CH2: V_{IN}, 0.5V/Div, DC
CH3: V_{REF}, 0.5V/Div, DC
CH4: V_{OUT}, 0.2V/Div, DC
TIME: 500µs/Div

Load Transient Response



I_{OUT}=14mA to 2A to 14mA (rise / fall time = 1µs)
V_{CNTL}=5V, V_{IN}=1.35V, V_{OUT}=0.675V
CH1: V_{OUT}, 20mV/Div, DC offset 0.675V
CH2: I_{OUT}, 1A/Div, DC
TIME: 10µs/Div

Load Transient Response

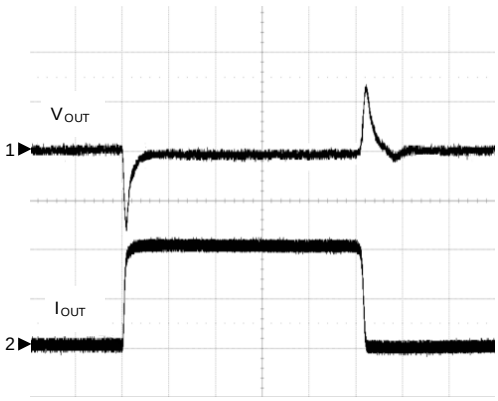


I_{OUT}= -14mA to -2A to -14mA (rise / fall time = 1µs)
V_{CNTL}=5V, V_{IN}=1.35V, V_{OUT}=0.675V
CH1: V_{OUT}, 20mV/Div, DC offset 0.675V
CH2: I_{OUT}, 1A/Div, DC
TIME: 5µs/Div

Operating Waveforms(Cont.)

Refer to the typical application circuit. The test condition is V_{CNTL}=5V, T_A= 25°C unless otherwise specified.

Load Transient Response

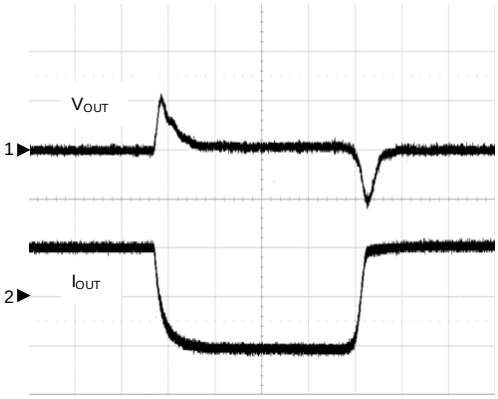


I_{OUT}=14mA to 2A to 14mA (rise / fall time = 1µs)
V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=0.75V
CH1: V_{OUT}, 20mV/Div, DC offset 0.75V
CH2: I_{OUT}, 1A/Div, DC
TIME: 10µs/Div

Load Transient Response

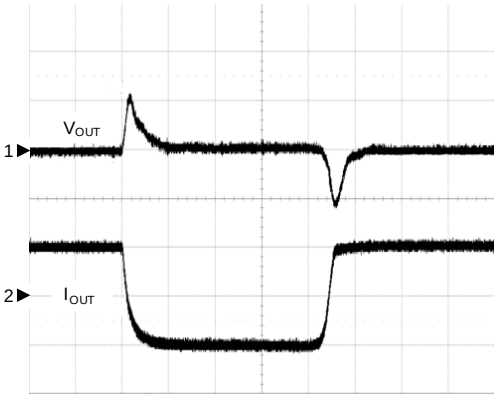
V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=0.75V
CH1: V_{OUT}, 20mV/Div, DC offset 0.75V
CH2: I_{OUT}, 1A/Div, DC
TIME: 5µs/Div

Load Transient Response



I_{OUT}= 2A to -2A to 2A
V_{CNTL}=5V, V_{IN}=1.35V, V_{OUT}=0.675V
CH1: V_{OUT}, 50mV/Div, DC offset 0.675V
CH2: I_{OUT}, 2A/Div, DC
TIME: 5µs/Div

Load Transient Response

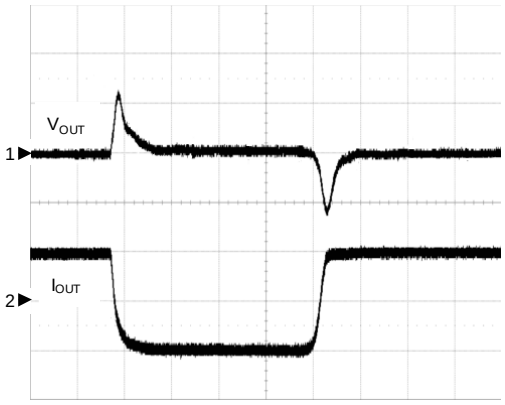


I_{OUT}= 2A to -2A to 2A
V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=0.75V
CH1: V_{OUT}, 50mV/Div, DC offset 0.75V
CH2: I_{OUT}, 2A/Div, DC
TIME: 5µs/Div

Operating Waveforms(Cont.)

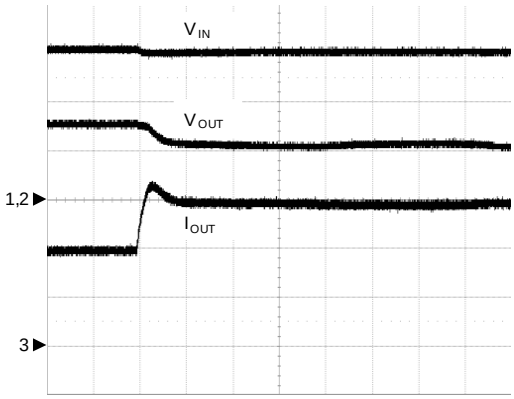
Refer to the typical application circuit. The test condition is V_{CNTL}=5V, T_A= 25°C unless otherwise specified.

Load Transient Response



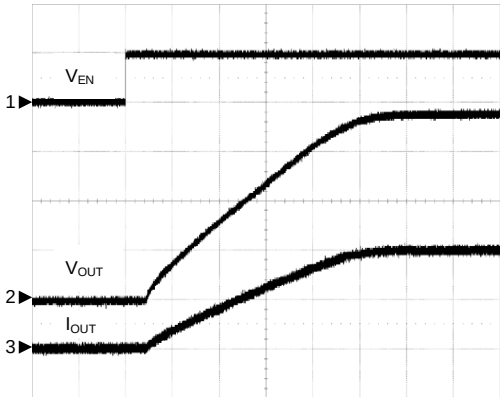
I_{OUT}= 2A to -2A to 2A
V_{CNTL}=5V, V_{IN}=1.8V, V_{OUT}=0.9V
CH1: V_{OUT}, 50mV/Div, DC offset 0.9V
CH2: I_{OUT}, 2A/Div, DC
TIME: 5µs/Div

Over Current Protection



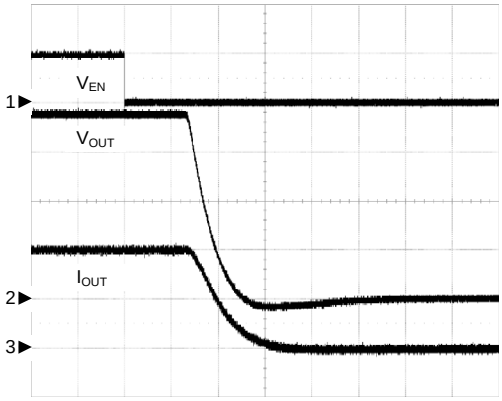
V_{IN}= 1.5V, V_{OUT}= 0.75V, I_{OUT}= 2A to 3A
CH1: V_{IN}, 0.5V/Div, DC
CH2: V_{OUT}, 0.5V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 20µs/Div, DC

Enable



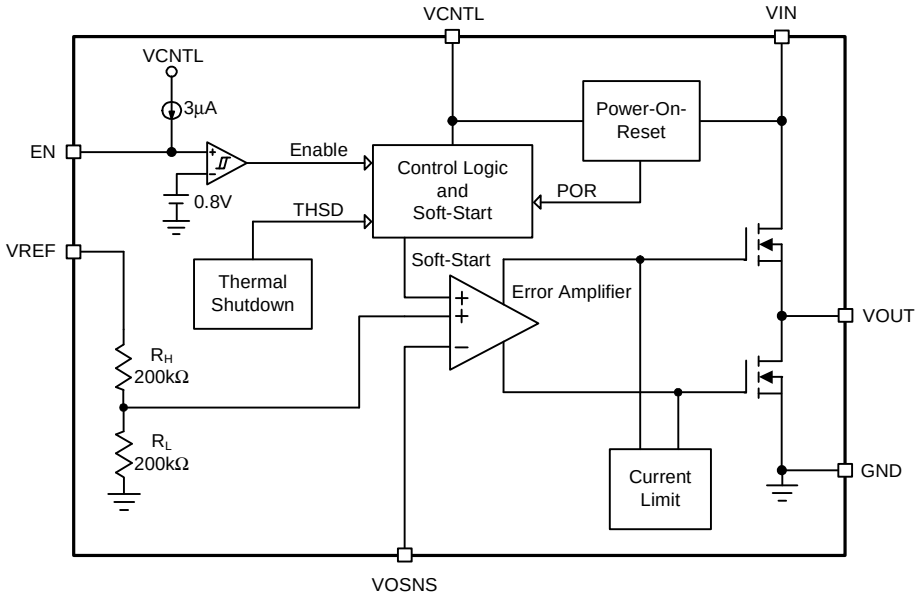
V_{IN}=1.8V, V_{REF}=1.8V, I_{OUT}=2A
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 0.2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Shutdown



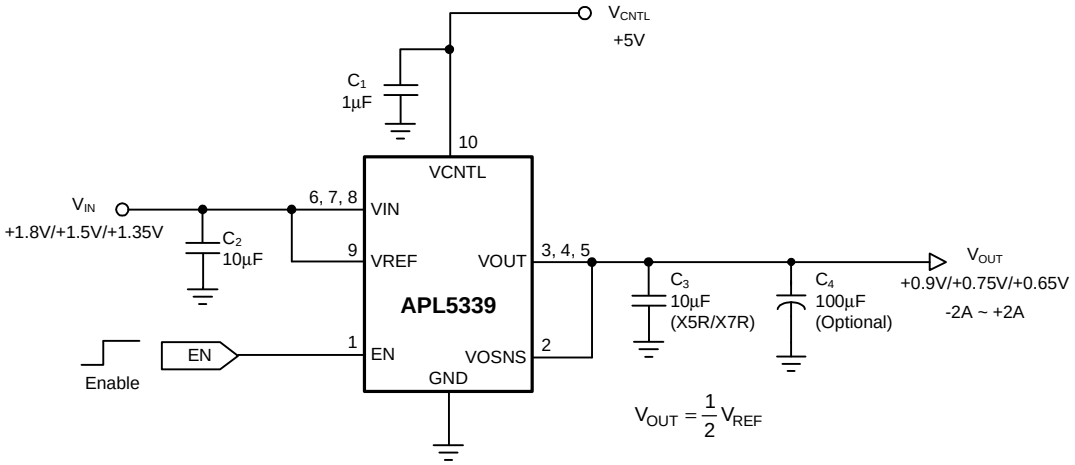
V_{IN}=1.8V, V_{REF}=1.8V, I_{OUT}=2A
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 0.2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 5µs/Div

Block Diagram



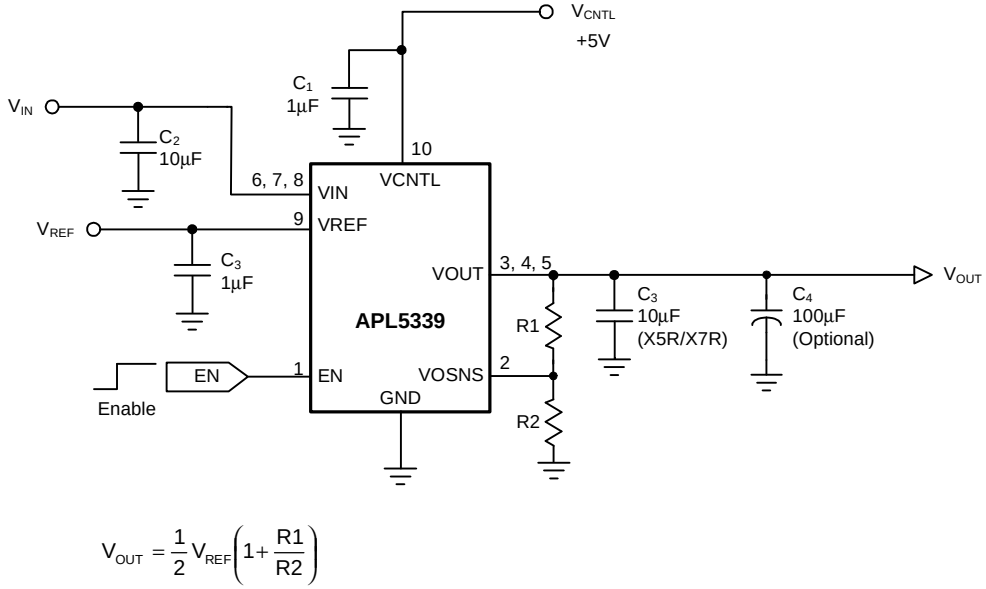
Typical Application Circuit

V_{OUT} = 0.9V/0.75V/0.675V Application



The ceramic capacitor C3 (at least 8µF) is necessary for output stability.

General Application



The ceramic capacitor C3 (at least 8µF) is necessary for output stability.

Function Description

Power-On-Reset(POR)

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR votage thresholds during powering on.

Output Voltage Regulation

The output voltage on VOUT pin is regulated to track the reference voltage applied on VREF pin. Two internal N-channel power MOSFETs controlled by high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN pin or sinking current to GND pin. An internal output voltage sense pad is bonded to the VOUT pin with a bonding wire for perfect load regulation.
For preventing the two power MOSFETs from shoot-through, a small voltage offset between the positive inputs of the two error amplifiers is designed. It results in higher output voltage while the regulator sinks light or heavy load current.

Enable/Shutdown

The APL5339 has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up by an internal current source (3μA typical) to enable normal operation.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 0.25 ms.

Current-Limit Protection

The APL5339 monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or shortcircuit (shorten from VOUT to GND or VIN) conditions.

Thermal Shutdown

An thermal shutdown circuit limits the junction temperature of the APL5339. When the junction temperature exceeds T_J = +170°C, a thermal sensor turns off the both pass transistors, allowing the device to cool. The thermal sensor allows the regulator to regulate again after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit designed with a 50°C hysteresis lowers the average T_J during continuous thermal overload conditions , increasing life time of the APL5339.

Application Information

Power Sequencing

The input sequencing of VIN and VCNTL is not necessary to be concerned.

Input Capacitor Selection

The APL5339 requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Because the parasitic inductors from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the input current, more parasitic inductance needs more input capacitance. For the APL5339, the total capacitance of input capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF. For VCNTL pin, a capacitor of 1μF (MLCC) or above is recommended for noise decoupling.

Output Capacitor Selection

The APL5339 needs a proper output capacitor to maintain
circuit stability and improve transient response. In order to insure the circuit stability, a 10μF X5R or X7R MLCC output capacitor is sufficient at all operating temperatures and it must be placed near the VOUT. The maximum distance from output capacitor to VOUT must within 2mm. Total output capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF. Table 1 provides the suitable output capacitors for APL5339.

Table 1: Output Capacitor Guide

Vendor	Description
Murata	10μF, 6.3V, X7R, 0805, GRM21BR70J106K
	10μF, 6.3V, X5R, 0805, GRM21BR60J106K

Murata website: www.murata.com

Operation Region and Power Dissipation

The APL5339 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D \le \frac{(T_J - T_A)}{\theta_{JA}}$$

Where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (Absolute Maximum Rating), the maximum power dissipation is calculated as:

$$P_{D(max)} = \frac{(150-25)}{60} = 2.08(W)$$

For normal operation, do not exceed the maximum junction temperature of T_J = 125°C. The calculated power dissipation should less than:

$$P_D = \frac{(125-25)}{60} = 1.67(W)$$

PCB Layout Considerations

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Please place the output capacitors close to the VOUT, a MLCC capacitor larger than 8μF must be placed near the VOUT. The distance from VOUT to output MLCC must be less than 2mm.
3. To place APL5339 and output capacitors near the load is good for load transient response.
4. Large current paths, the bold lines in Figure 1, must have wide tracks.
5. VREF should be connected to VIN by a separate track. VREF is the reference voltage of VOUT, so avoid any noise to get into the VREF.
6. Place the R1 and R2 near the APL5339 as close as possible to avoid noise coupling.
7. Connect the ground of the R2 to the GND pin by using a dedicated track.
8. Connect the one pin of the R1 to the load for Kelvin sensing.

Application Information (Cont.)

PCB Layout Considerations (Cont.)

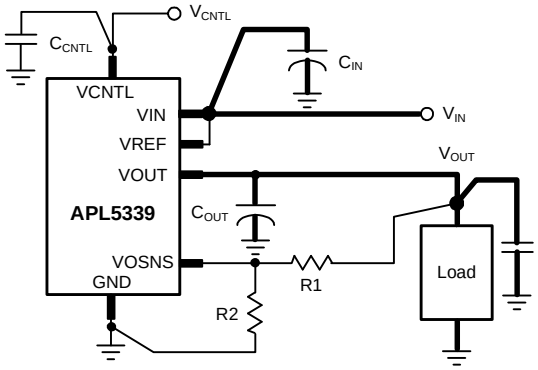
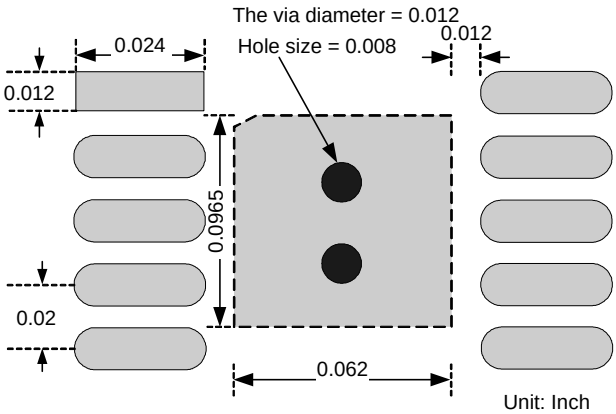


Figure 1.

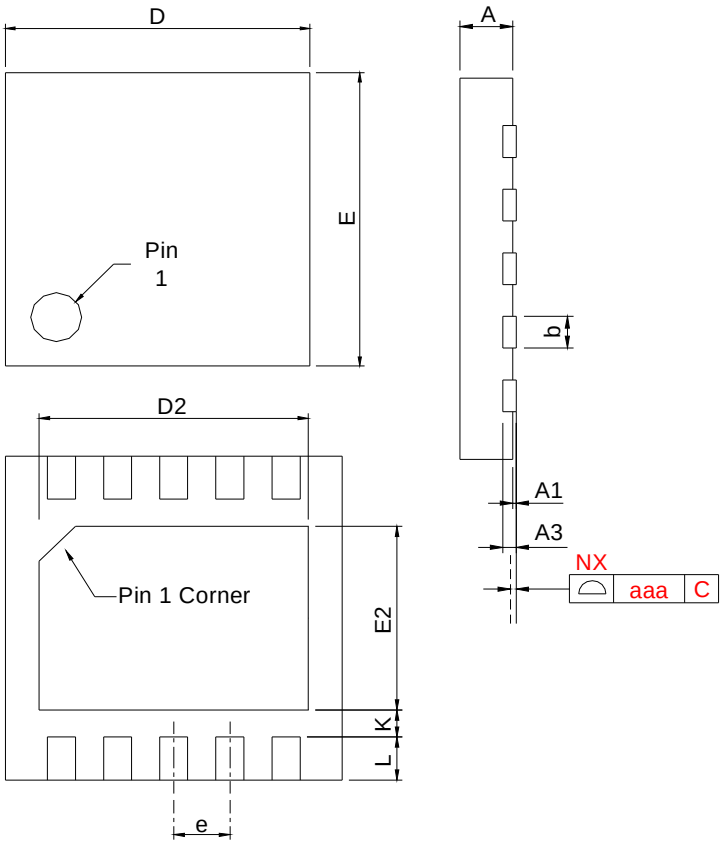
Recommanded Minimum Footprint



TDFN3x3-10

Package Information

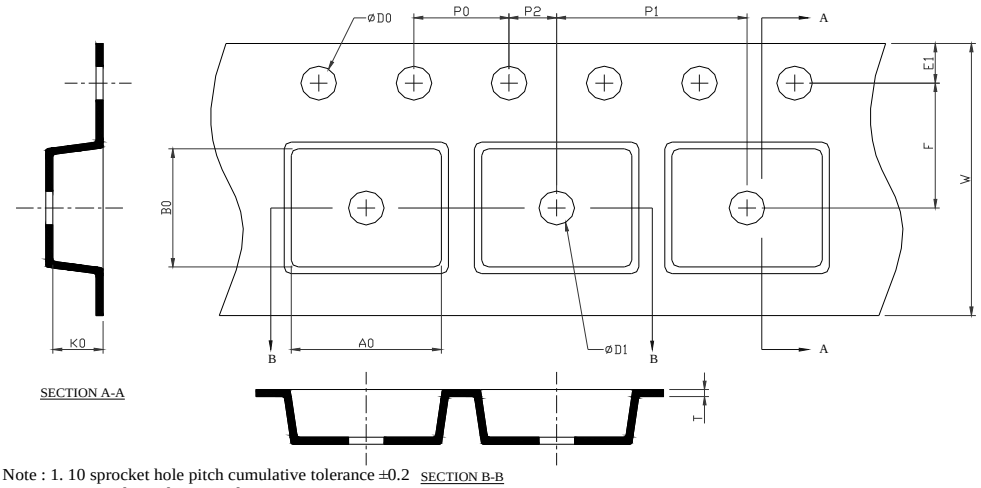
TDFN3x3-10



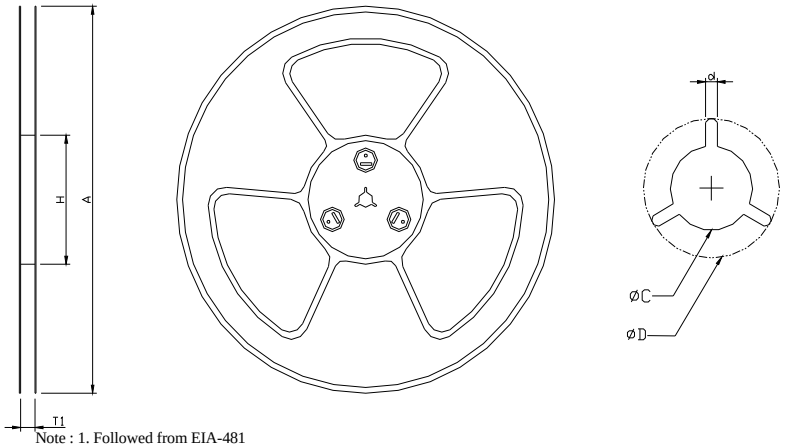
SYMBOL	TDFN3*3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note:1.Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Note : 1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Material: conductive polystyrene
3. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
4 Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier



Note : 1. Followed from EIA-481

Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

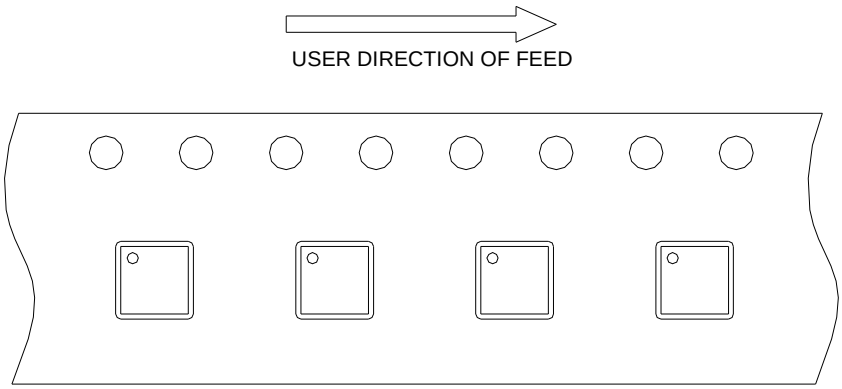
(mm)

Devices Per Unit

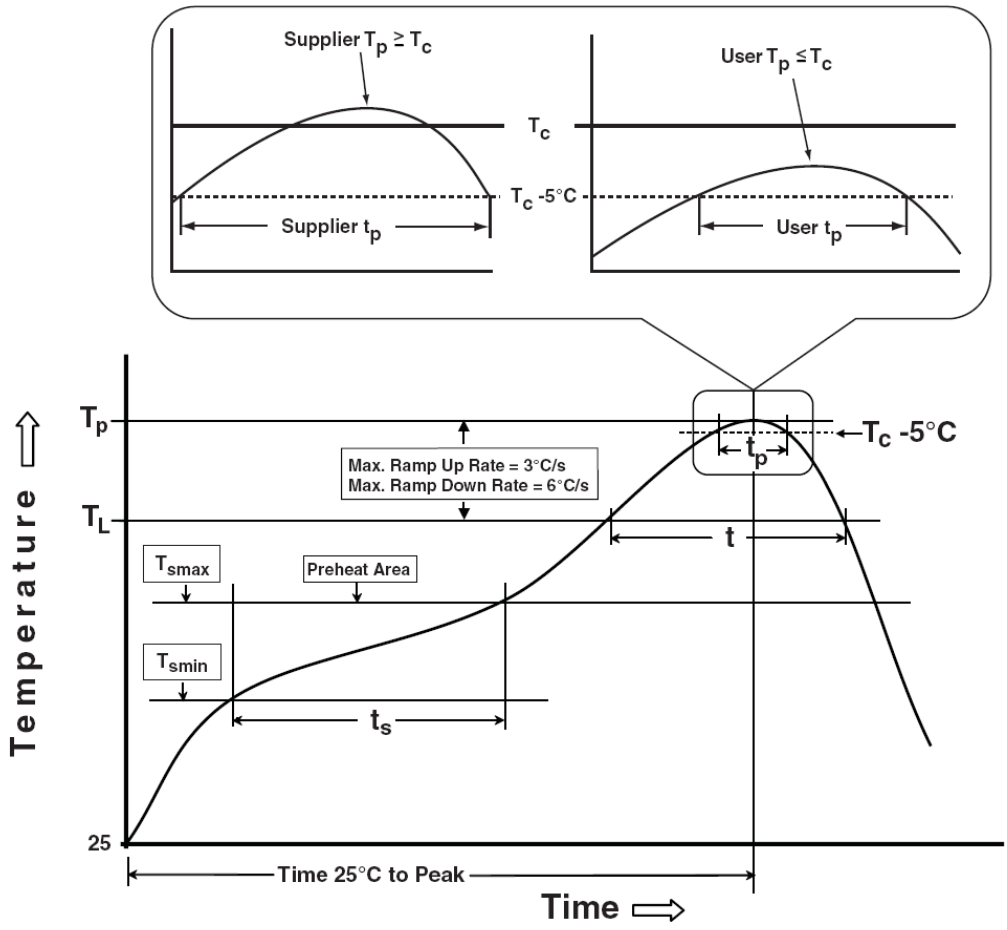
Package Type	Unit	Quantity
TDFN 3*3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838