

## High Input Voltage, Low Quiescent Current, 150mA LDO Regulator

### Features

- **Wide Input Voltage Range: 4.5V to 25V**
- **Ultra Low Ground Current: 10mA**
- **High Output Accuracy:  $\pm 2.5\%$**
- **Excellent Load/Line Transient**
- **Low Dropout Voltage: 750mV @ 150mA**
- **Fixed Output Voltages for 5V/3.3V or Adjustable Voltage**
- **Built-In Current-Limit Protection**
- **Built-In Over-Temperature Protection**
- **Zero Shutdown Current**
- **Internal Soft-Start Function**
- **POR Scheme to Prevent VOUT Spike**
- **SOT-23-5, SOT-89, and SOP-8P Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

### Applications

- **USB Power Supply**
- **Keep-Alive Supply in Notebook and Portable Computers**
- **Logic Supply for High-Voltage Batteries**
- **Battery Powered Systems**

### General Description

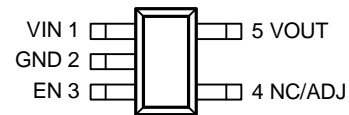
The APL5155E is a low ground current linear regulator, which operates with input voltage from 4.5V to 25V and delivers output current up to 150mA. Typical dropout voltage is only 750mV at 150mA loading. This combination of the high voltage and the low ground current makes the APL5155E ideal for USB and portable devices, using 2-cell or 3-cell Li-Ion battery inputs.

The APL5155E is stable with aluminum, tantalum, and ceramic capacitors. It requires a 1 $\mu$ F or greater capacitor for stability.

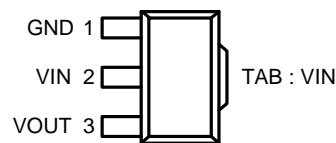
The APL5155E has many protection functions, including over-temperature, current-limit and short circuit current limit protections, which prevent the device from thermal over-load and current over-load.

The APL5155E regulator is available in miniature SOT-23-5, SOT-89, and SOP-8P packages.

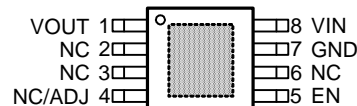
### Pin Configuration




**SOT-23-5  
(Top View)**



**SOT-89  
(Top View)**

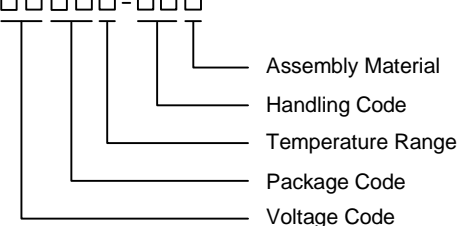


**SOP-8P  
(Top View)**

 = Thermal Pad  
(connected to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

<p>APL5155E □□□□-□□□</p>  <p>Assembly Material Handling Code Temperature Range Package Code Voltage Code</p>	<p>Package Code B : SOT-23-5 D : SOT-89 KA : SOP-8P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape &amp; Reel Voltage Code 33 : 3.3V 50 : 5.0V Blank : Adjustable Version Assembly Material G : Halogen and Lead Free Device</p>
APL5155E B : <span style="border: 1px solid black; padding: 2px;">L55X</span>	X - Date Code
APL5155E 33B : <span style="border: 1px solid black; padding: 2px;">55RX</span>	X - Date Code ; R - 3.3V
APL5155E 50B : <span style="border: 1px solid black; padding: 2px;">55ZX</span>	X - Date Code ; Z - 5.0V
APL5155E D : <span style="border: 1px solid black; padding: 2px;">APL5155E XXXXX</span>	XXXXX - Date Code
APL5155E KA : <span style="border: 1px solid black; padding: 2px;">APL5155E XXXXX ●</span>	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{IN}, V_{EN}$	VIN, EN to GND Voltage	- 0.3 to 27	V
$V_{OUT}, V_{ADJ}$	VOUT, ADJ to GND Voltage	- 0.3 to 27	V
$T_J$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature	-65 to 150	°C
$T_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Thermal Resistance-Junction to Ambient <sup>(Note 2)</sup>	SOT-23-5	235
		SOT-89	180
		SOP-8P	50
$\theta_{JC}$	Thermal Resistance-Junction to Ambient <sup>(Note 2)</sup>	SOT-23-5	130
		SOT-89	38
		SOP-8P	20

Note 2:  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V <sub>IN</sub>	V <sub>IN</sub> to GND Voltage	4.5 to 25	V
I <sub>OUT</sub>	V <sub>OUT</sub> Source Current	V <sub>IN</sub> =5.5V~25V	0 to 150
		V <sub>IN</sub> =4.5V~5.5V	0 to 50
V <sub>OUT</sub>	Adjustable Output Voltage	1.24 to 20	V
V <sub>EN</sub>	EN Pin Input Voltage	0 to 25	V
C <sub>OUT</sub>	Output Capacitance	1 to 4.7	μF
ESR	The ESR of Output Capacitance	5 to 50	mΩ
T <sub>A</sub>	Ambient Temperature	-40 to 85	°C
T <sub>J</sub>	Junction Temperature	-40 to 125	°C

Note 3: Refer to the typical application circuit.

## Electrical Characteristics

Unless otherwise noted, these specifications apply over V<sub>IN</sub>=V<sub>OUT</sub>+3V, C<sub>IN</sub>=1μF, C<sub>OUT</sub>=2.2μF, T<sub>A</sub>=-40 to 85°C.

Symbol	Parameter	Test Conditions	APL5155E			Unit
			Min.	Typ.	Max.	
<b>POWER-ON-RESET (POR) AND SUPPLY CURRENT</b>						
V <sub>IN</sub>	Input Voltage		4.5	-	25	V
	Rising V <sub>IN</sub> POR Threshold		3.9	4.1	4.3	V
	V <sub>IN</sub> POR Hysteresis		-	200	-	mV
I <sub>Q</sub>	Quiescent Current	I <sub>OUT</sub> =0mA, EN=high, Adj mode	-	10	20	μA
		I <sub>OUT</sub> =0mA, EN=high, Fix Mode	-	15	25	
I <sub>QSHDN</sub>	Shutdown Supply Current	EN=Low, V <sub>IN</sub> =19V	-	1	3	μA
<b>REFERENCE AND OUTPUT VOLTAGE</b>						
V <sub>REF</sub>	Reference Voltage	Adjustable Voltage Version	-	1.24	-	V
	VREF Voltage Accuracy	I <sub>OUT</sub> =10mA, T <sub>A</sub> =25°C	-2.5	-	2.5	%
	VREF Temperature Coefficient	T <sub>J</sub> =-40 to 125°C	-	50	-	ppm
V <sub>OUT</sub>	Output Voltage	Fixed Voltage Version	-	3.3	-	V
		Fixed Voltage Version	-	5.0	-	
	Output Voltage Accuracy	I <sub>OUT</sub> =10mA, T <sub>A</sub> =25°C	-2.5	-	2.5	%
I <sub>OUT</sub>	Load Current Range		0	-	150	mA
REG <sub>LINE</sub>	Line Regulation	V <sub>OUT</sub> +3V<V <sub>IN</sub> <25V, I <sub>OUT</sub> =1mA, V <sub>OUT</sub> =5V	-	0.1	0.5	%
REG <sub>LOAD</sub>	Load Regulation	0.1mA<I <sub>OUT</sub> <150mA, V <sub>OUT</sub> =5V	-	0.6	1.4	%
V <sub>DROP</sub>	Dropout Voltage	I <sub>OUT</sub> =30mA, V <sub>OUT</sub> =20V	-	160	240	mV
		I <sub>OUT</sub> =100mA, V <sub>OUT</sub> =20V	-	500	750	
		I <sub>OUT</sub> =150mA, V <sub>OUT</sub> =20V	-	750	1125	
		I <sub>OUT</sub> =10mA, V <sub>OUT</sub> =5V	-	150	225	
		I <sub>OUT</sub> =10mA, V <sub>OUT</sub> =3.3V	-	170	250	
<b>PROTECTIONS</b>						
T <sub>OTP</sub>	Over-Temperature Threshold	T <sub>J</sub> rising	-	150	-	°C
	Over-Temperature Hysteresis		-	30	-	°C

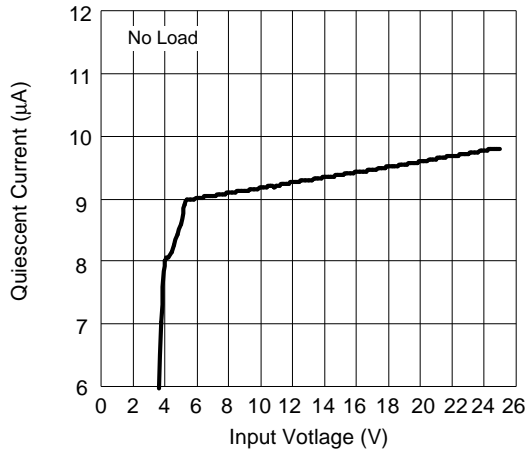
## Electrical Characteristics (Cont.)

Unless otherwise noted, these specifications apply over  $V_{IN}=V_{OUT}+3V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=2.2\mu F$ ,  $T_A=-40$  to  $85^\circ C$ .

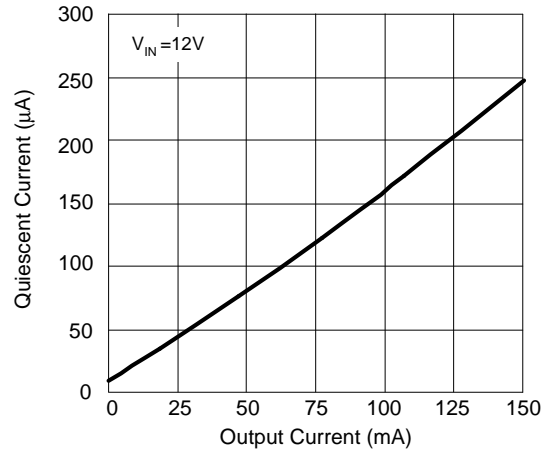
Symbol	Parameter	Test Conditions	APL5155E			Unit
			Min.	Typ.	Max.	
<b>PROTECTIONS (CONT.)</b>						
I <sub>LIMIT</sub>	Current-Limit	$V_{IN}=6V$ to $25V$ , $V_{OUT}<V_{IN}-3V$	200	-	400	mA
		$V_{IN}=4.5V$ to $6V$ , $V_{OUT}<V_{IN}-1V$	60	-	250	mA
I <sub>SHORT</sub>	Short-Circuit Current	$V_{OUT}=0V$ , only for Fix mode	-	50	-	mA
<b>SOFT-START AND SHUTDOWN</b>						
T <sub>SS</sub>	Soft-Start Interval	From $V_{EN}$ rising to $V_{OUT}=90\%$	-	1	-	ms
	EN Input Logic HIGH	IC is enabled	2.5	-	-	V
	EN Input Logic LOW	IC is shut down	0	-	0.6	V
	EN Input Logic Hysteresis	$V_{OUT}+3V < V_{IN} < 25V$	-	0.2	-	V
I <sub>EN</sub>	EN Pin Input Bias Current	$V_{EN}=25V$	-	0.1	1	$\mu A$

### Typical Operating Characteristics

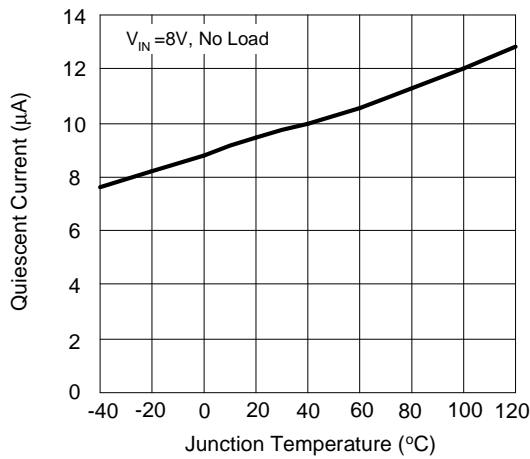
Quiescent Current vs. Input Voltage



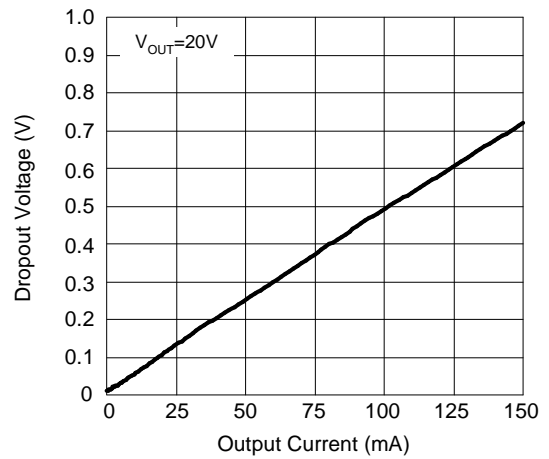
Quiescent Current vs. Output Current



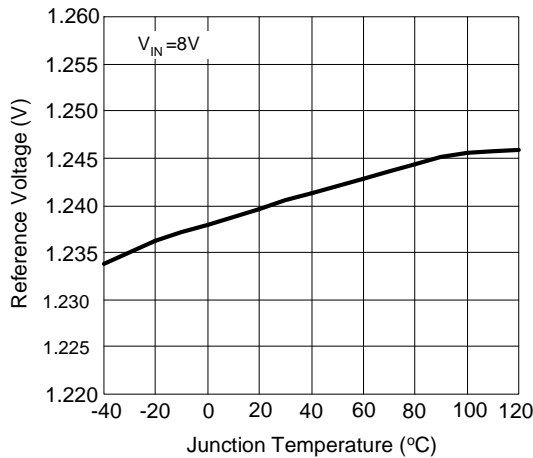
Quiescent Current vs. Junction Temperature



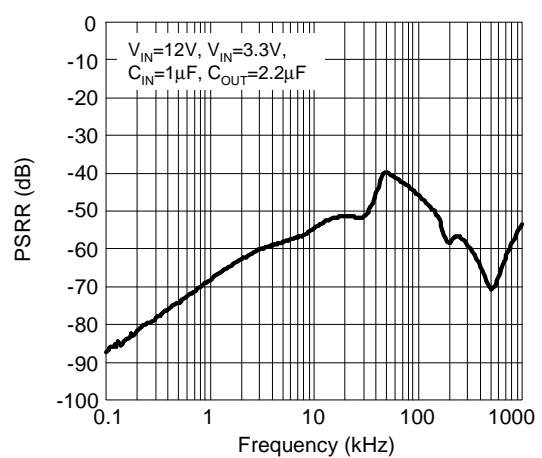
Dropout Voltage vs. Output Current



Reference Voltage vs. Junction Temperature



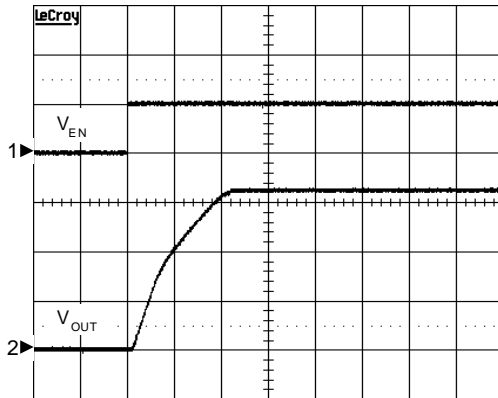
PSRR vs. Frequency



## Operating Waveforms

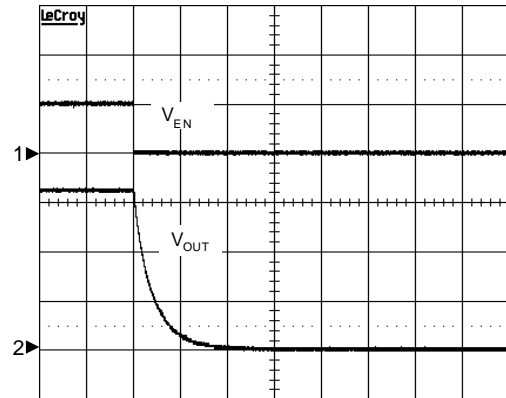
The test condition is  $T_A=25^\circ\text{C}$  unless otherwise specified.

### Turn On Response



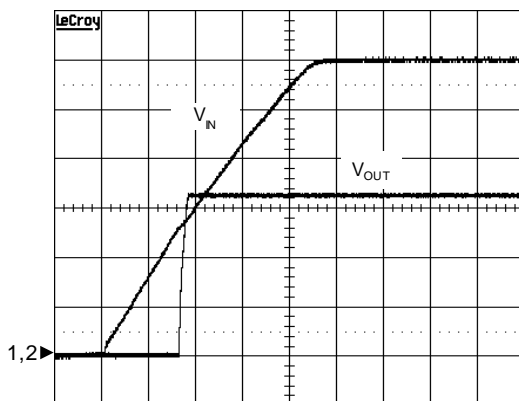
$V_{IN}=12\text{V}$ ,  $V_{OUT}=3.3\text{V}$ ,  $R_{OUT}=33\Omega$ ,  
 $C_{IN}=1\mu\text{F}/X7R$ ,  $C_{OUT}=2.2\mu\text{F}/X7R$   
 CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 TIME: 0.5ms/Div

### Turn Off Response



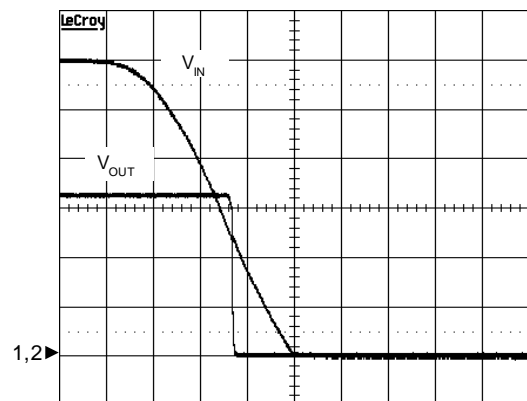
$V_{IN}=12\text{V}$ ,  $V_{OUT}=3.3\text{V}$ ,  $R_{OUT}=33\Omega$ ,  
 $C_{IN}=1\mu\text{F}/X7R$ ,  $C_{OUT}=2.2\mu\text{F}/X7R$   
 CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 TIME: 0.2ms/Div

### Power On



$V_{IN}=12\text{V}$ ,  $V_{OUT}=3.3\text{V}$ ,  $R_{OUT}=33\Omega$ ,  
 $C_{IN}=1\mu\text{F}/X7R$ ,  $C_{OUT}=2.2\mu\text{F}/X7R$   
 CH1:  $V_{IN}$ , 2V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 TIME: 5ms/Div

### Power Off

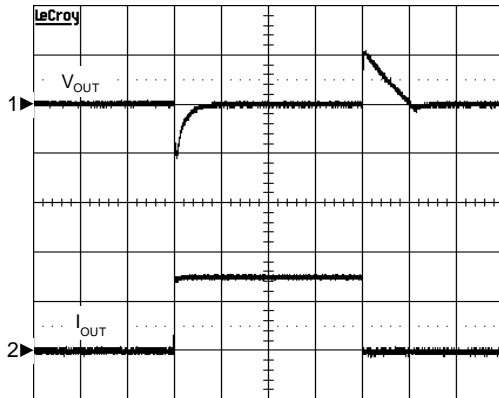


$V_{IN}=12\text{V}$ ,  $V_{OUT}=3.3\text{V}$ ,  $R_{OUT}=33\Omega$ ,  
 $C_{IN}=1\mu\text{F}/X7R$ ,  $C_{OUT}=2.2\mu\text{F}/X7R$   
 CH1:  $V_{IN}$ , 2V/Div, DC  
 CH2:  $V_{OUT}$ , 1V/Div, DC  
 TIME: 5ms/Div

## Operating Waveforms (Cont.)

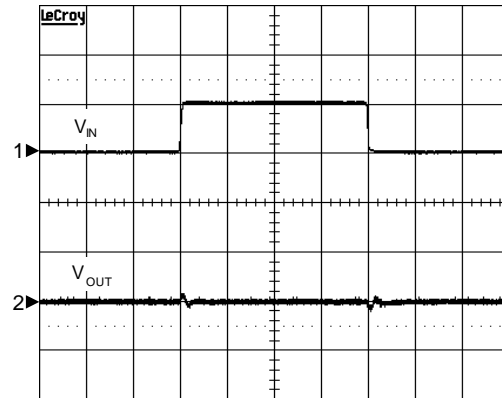
The test condition is  $T_A=25^{\circ}\text{C}$  unless otherwise specified.

### Load Transient Response



$V_{IN}=12\text{V}$ ,  $V_{OUT}=3.3\text{V}$ ,  $C_{IN}=1\mu\text{F}/\text{X7R}$ ,  
 $C_{OUT}=2.2\mu\text{F}/\text{X7R}$ ,  $I_{OUT}=3-150-3\text{mA}$ ,  
 Falling/Rising Slew Rate= $1\text{A}/\mu\text{s}$   
 CH1:  $V_{OUT}$ , 100mV/Div, offset= $3.3\text{V}$   
 CH2:  $I_{OUT}$ , 100mA/Div, DC  
 TIME: 50µs/Div

### Line Transient Response



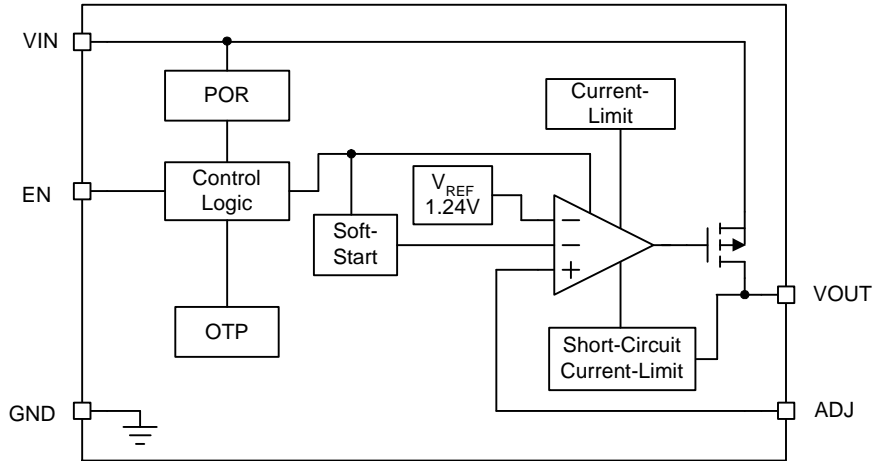
$V_{IN}=11.5-12.5-11.5\text{V}$ , Falling/Rising= $1\mu\text{s}$ ,  
 $V_{OUT}=3.3\text{V}$ ,  $I_{OUT}=10\text{mA}$ ,  $C_{IN}=1\mu\text{F}/\text{X7R}$ ,  
 $C_{OUT}=2.2\mu\text{F}/\text{X7R}$   
 CH1:  $V_{IN}$ , 1V/Div, Offset= $11.5\text{V}$   
 CH2:  $V_{OUT}$ , 50mV/Div, Offset= $3.3\text{V}$   
 TIME: 50µs/Div

## Pin Description

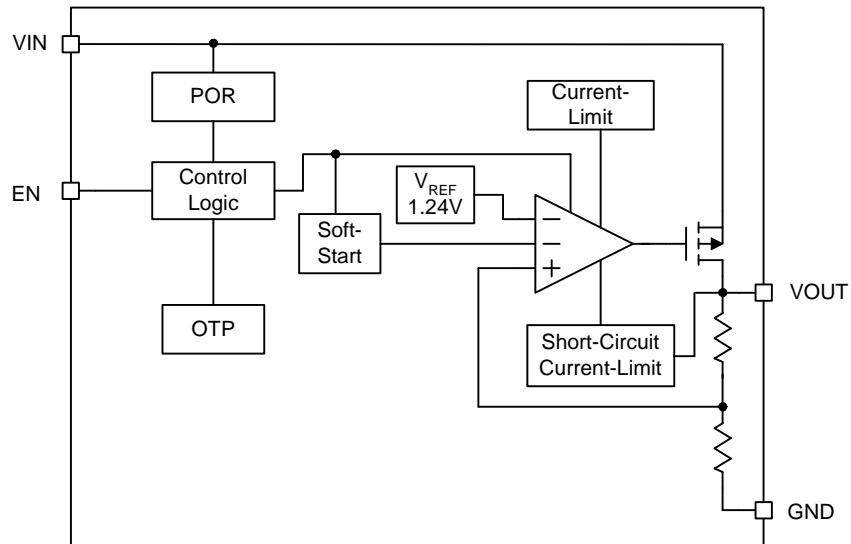
PIN			NAME	FUNCTION
NO.				
SOT-23-5	SOT-89	SOP-8P		
1	2	8	VIN	Voltage Supply Input Pin.
2	1	7	GND	Ground.
3	-	5	EN	Enable Input Pin. Logic low=shutdown; logic high=enable.
4	-	4	NC/ADJ	NC: No Connection (fixed output voltage version). ADJ: Output Voltage Feedback Pin (adjust output voltage version).
5	3	1	VOUT	Regulator Output Pin.
-	-	2, 3, 6	NC	No Connection.

## Block Diagram

### 1. Adjust Output Voltage (SOT-23-5/SOP-8P)



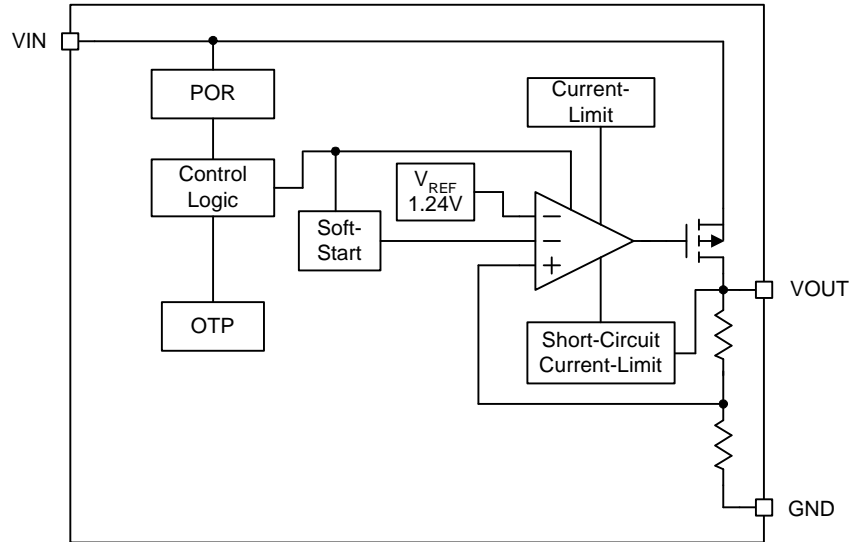
### 2. Fixed Output Voltage (SOT-23-5/SOP-8P)





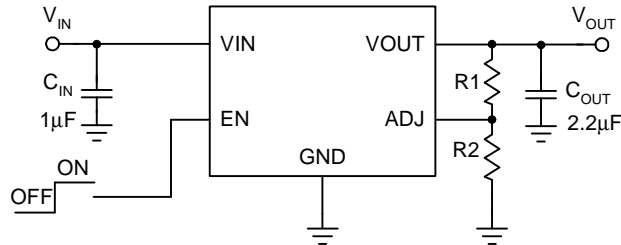
## Block Diagram (Cont.)

### 3. Fixed Output Voltage (SOT-89)



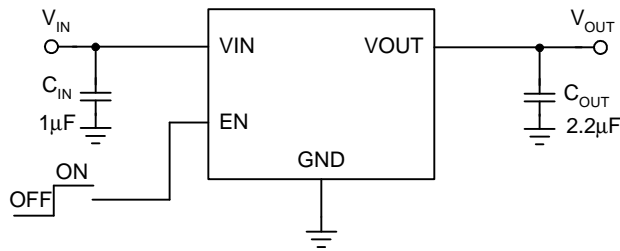
## Typical Application Circuit

### 1. Adjust Output Voltage (SOT-23-5/SOP-8P)

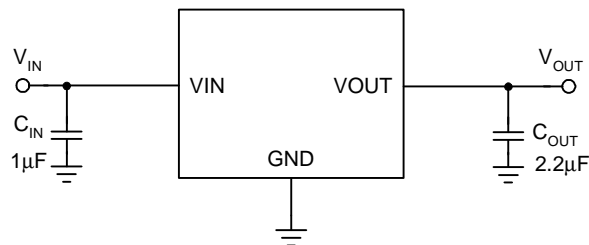


$$V_{OUT} = 1.24V \times (R1 + R2) / R2$$

### 2. Fixed Output Voltage (SOT-23-5/SOP-8P)



### 3. Fixed Output Voltage (SOT-89)



## Application Information

### Enable/Shutdown

The APL5155E features an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator, so current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The enable pin can not float.

### Input Capacitor

The APL5155E has high input voltage up to 25V. The input capacitor must be rated to sustain voltages that may be used on the input. An input capacitor may be required when the device is not near the source power supply or when supplied by a battery. Small and surface-mounted ceramic capacitors can be used for bypassing. A larger value may be required if the source supply has high ripple.

### Output Capacitor

The APL5155E requires an output capacitor for stability. The design requires 1μF or greater on the output to maintain stability. It is optimized by using low-ESR ceramic chip capacitors. The maximum allowable ESR is 3Ω. More capacitance improves transient response. Place the output capacitor as close to the VOUT pin as possible. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors change capacitance by 15% over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

### No-Load Stability

The APL5155E will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

### Thermal Consideration

The thermal resistance of junction to ambient controls the APL5155E's maximum power dissipation. The power dissipation across the device is  $P_D = I_{OUT}(V_{IN} - V_{OUT})$ , and the maximum power dissipation is:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}}$$

where  $T_J - T_A$  is the temperature difference between the junction and ambient air.  $\theta_{JA}$  is the thermal resistance between junction and ambient air.

For continual operation, do not exceed the absolute maximum junction temperature rating of  $T_J = 125^\circ\text{C}$ .

For example:

In SOT-23-5 package  $\theta_{JA} = 235^\circ\text{C/W}$ . When operates the APL5155E at  $T_A = 50^\circ\text{C}$ , the maximum power dissipation can be determined as below:

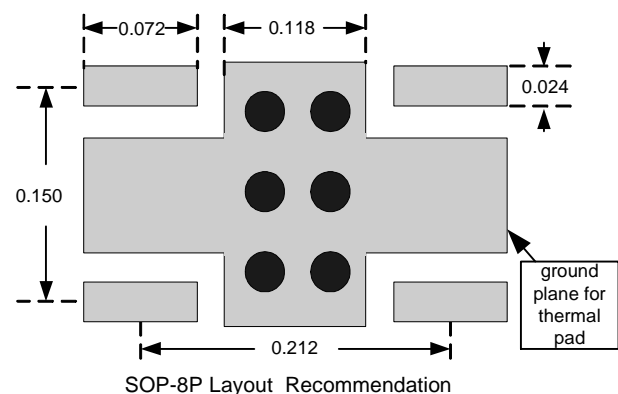
$$P_{D(MAX)} = (125^\circ\text{C} - 50^\circ\text{C}) / (235^\circ\text{C/W})$$

$$P_{D(MAX)} = 319.1\text{mW}$$

### Thermal Pad Consideration

The SOP-8P is a cost-effective package which features a small size, like a standard SOP-8, and a bottom thermal pad to minimize the thermal resistance of the package is applicable to high current applications. The thermal pad must be soldered down to the copper plane on circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 4 or 6 vias should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.



## Application Information (Cont.)

### Adjustable Regulator Application

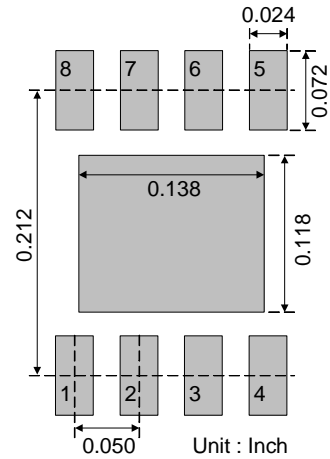
SOP-8P

The output voltage of APL5155E can be adjusted from 3V to 20V by using two external resistors. The resistors set the output voltage based on the following equation:

$$V_{OUT} = V_{REF} \left( 1 + \left( \frac{R_1}{R_2} \right) \right)$$

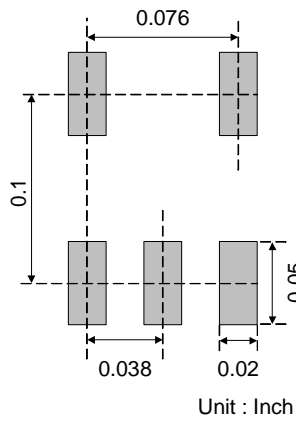
where  $V_{REF}=1.24V$

The resistors should be placed as close the device as possible to avoid noise.

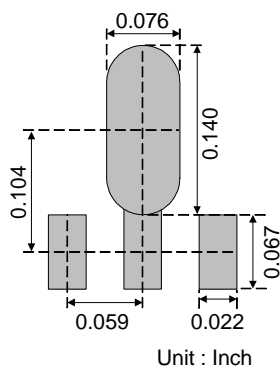


### Recommended Minimum Footprint

SOT-23-5

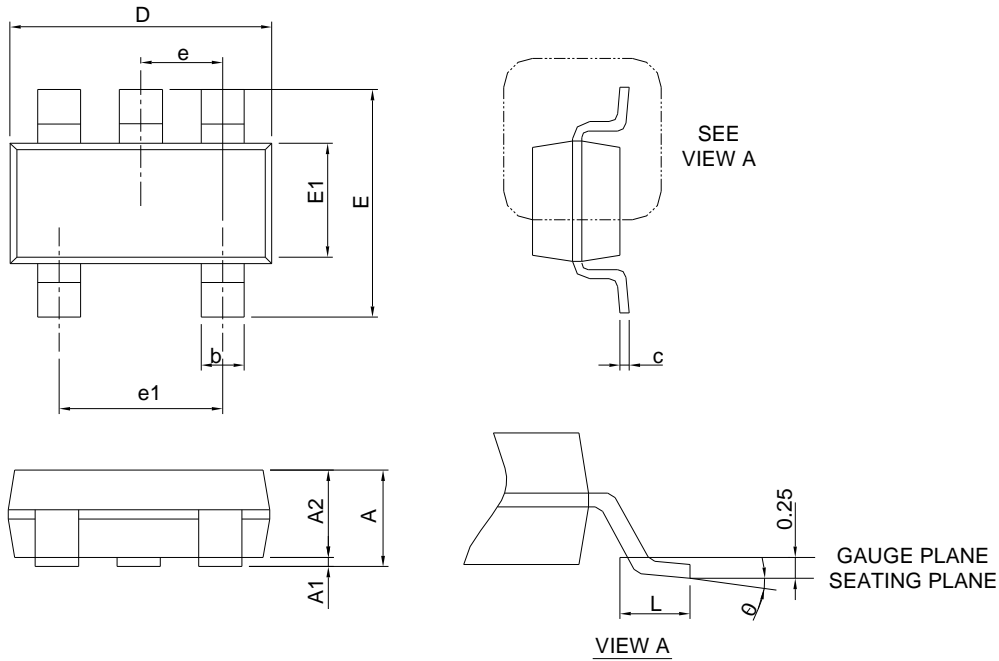


SOT-89



Package Information

SOT-23-5

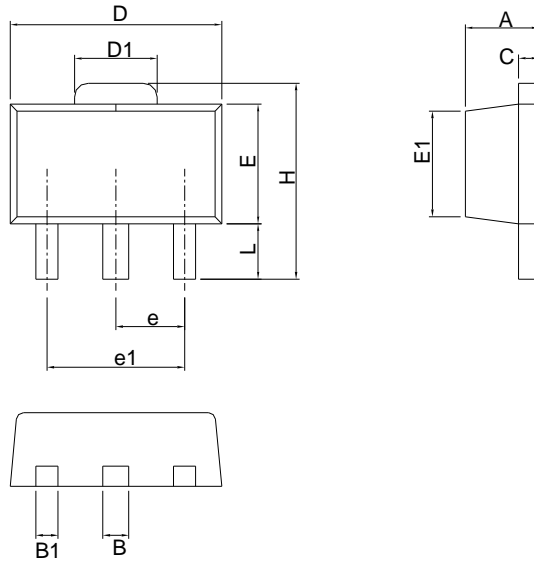


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.  
 2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOT-89

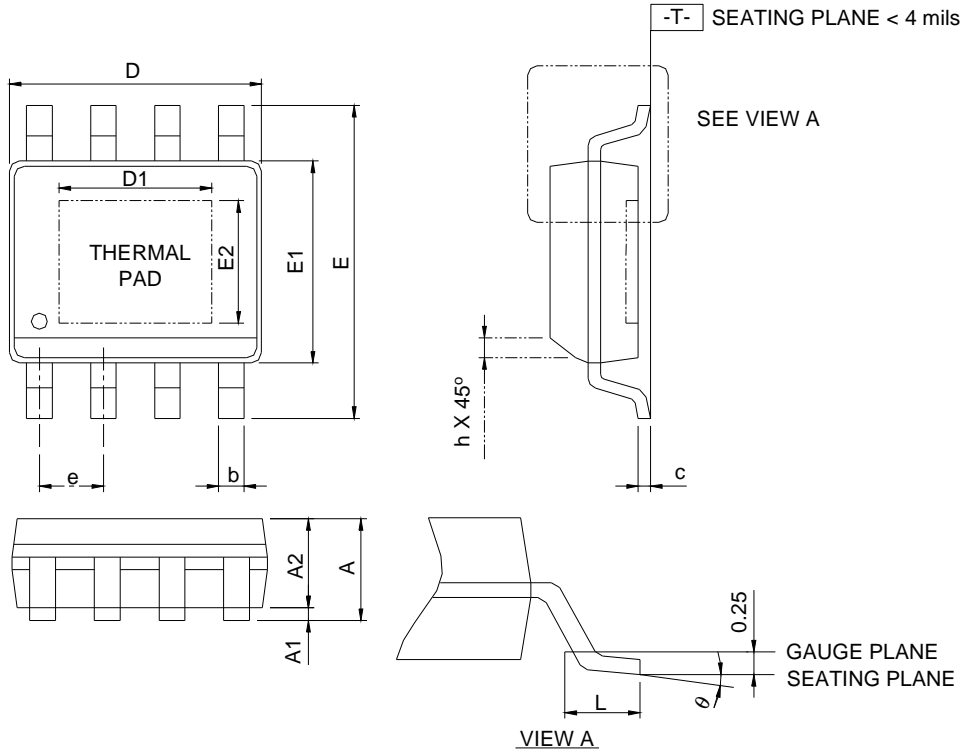


Symbol	SOT-89			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.40	1.60	0.055	0.063
B	0.44	0.56	0.017	0.022
B1	0.36	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.62	1.83	0.064	0.072
E	2.29	2.60	0.090	0.102
E1	2.13	2.29	0.084	0.090
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
H	3.94	4.25	0.155	0.167
L	0.89	1.20	0.035	0.047

Note : Follow JEDEC TO-243 AA.

Package Information

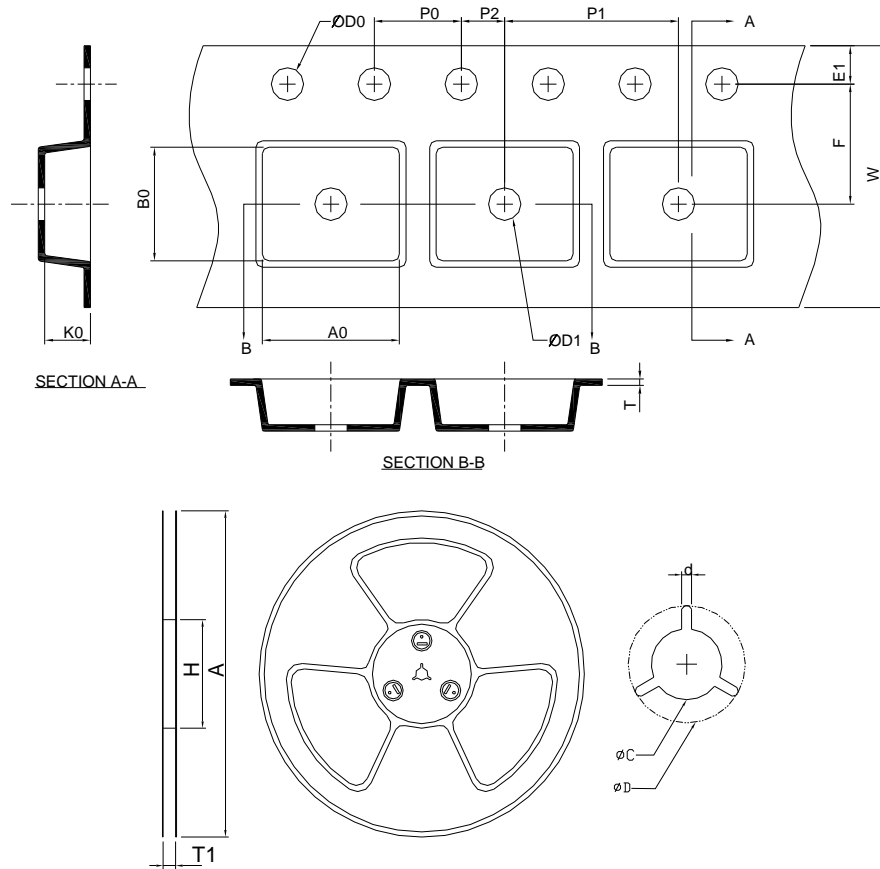
SOP-8P



Symbol	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

- Note : 1. Followed from JEDEC MS-012 BA.  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .  
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

### Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-89	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.80±0.20	4.50±0.20	1.80±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

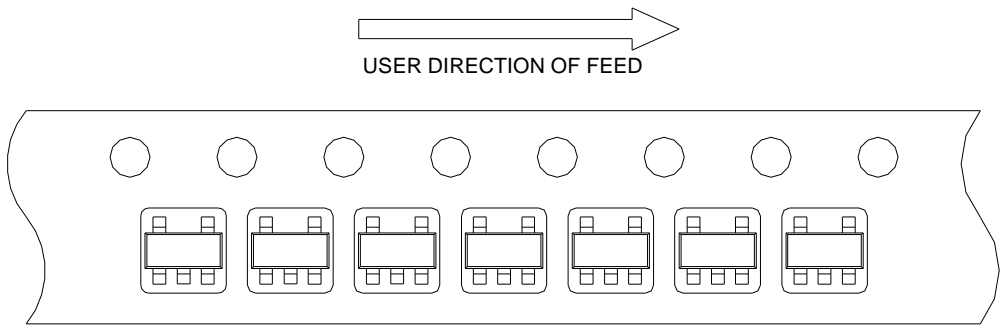


**Devices Per Unit**

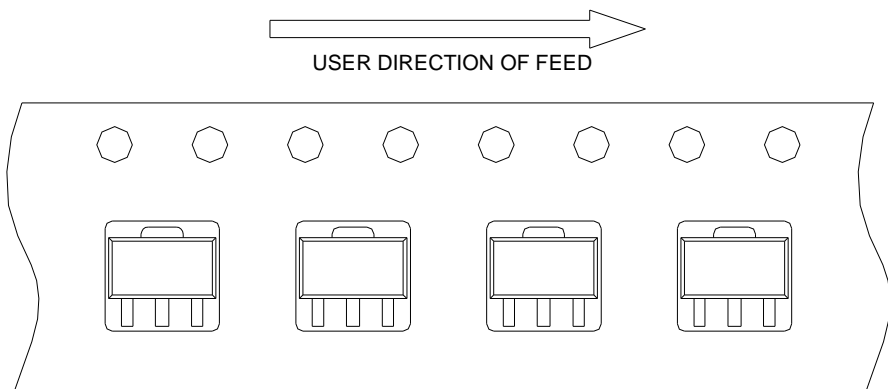
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SOT-89	Tape & Reel	1000
SOP-8P	Tape & Reel	2500

**Taping Direction Information**

**SOT-23-5**

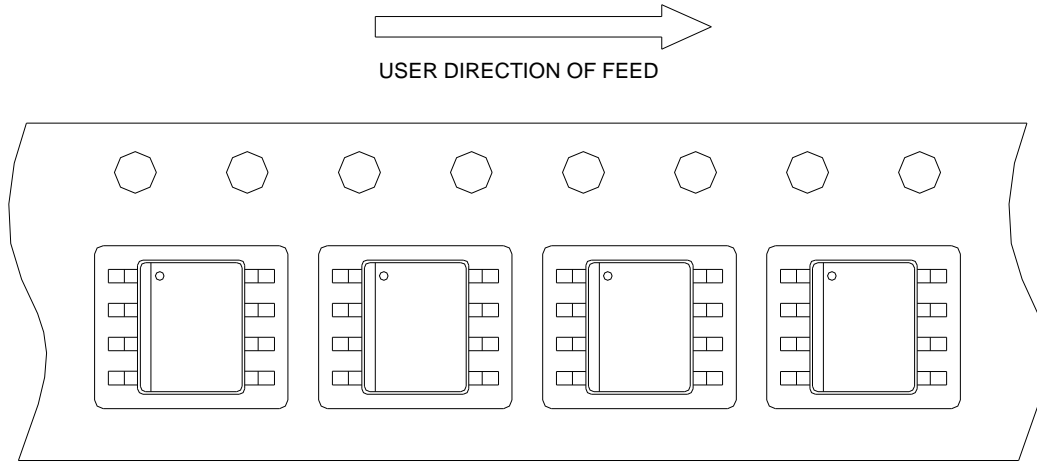


**SOT-89**

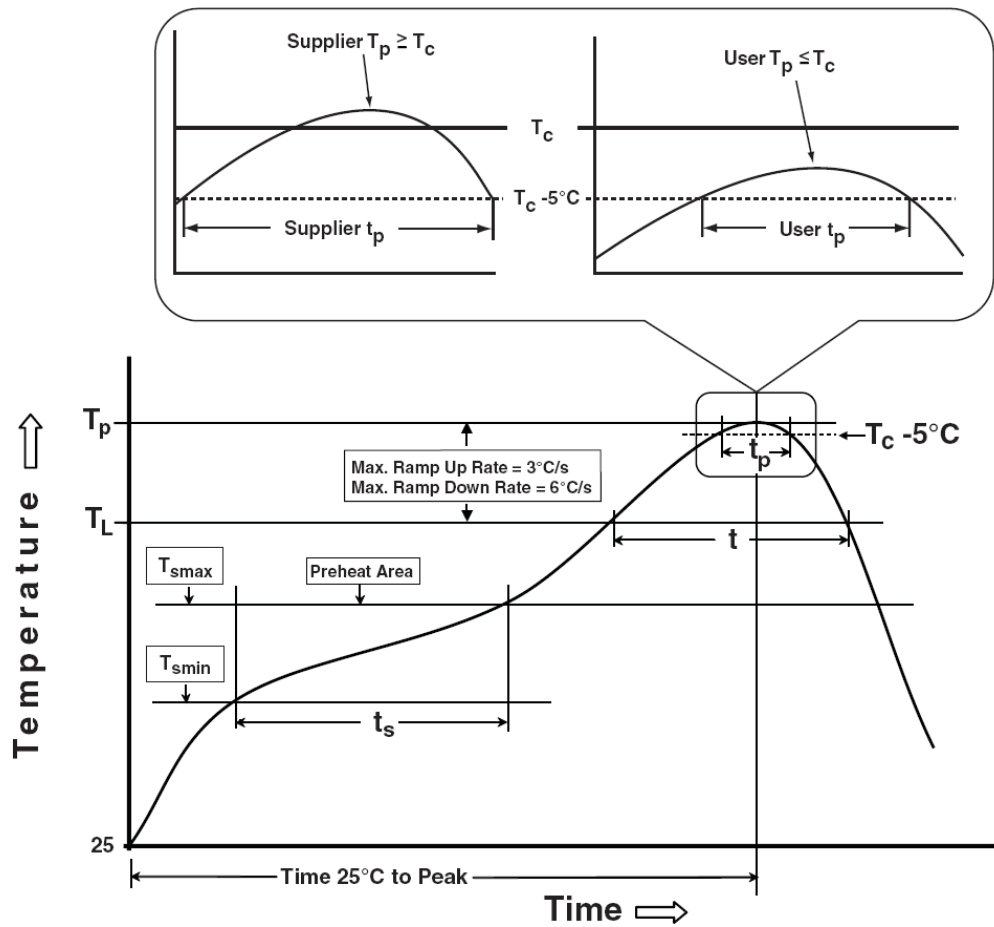


### Taping Direction Information

SOP-8P



### Classification Profile



**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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## Customer Service

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