APL3561

Programmable High Current Protection Switch

Features

- **Wide Supply Voltage Range: 2.5V to 5.5V with surge up to 15V**
- **30mΩ(typ) Power Switch On Resistance**
- **Programmable Current Limit**
- **Programmable Soft-Start Time**
- **Selectable Clamping Output Voltage Threshold**
- **PG Indicator Pin for Operation Status**
- **FLG Indicator Pin for Input Voltage Status**
- **Over-Temperature Protection**
- **Built in True Reverse-Current Blocking (TRCB)**
- **Enable Input**
- **Built in Thermal Shutdown Protection**
- **VTQFN2x2-9 Package**

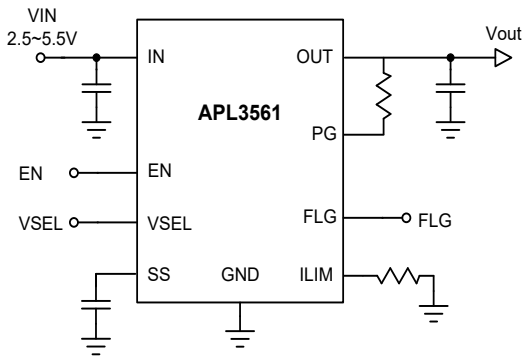
Applications

- **SSD M.2 from factor**
- **SSD dual input power application**
- **SSD load switch**

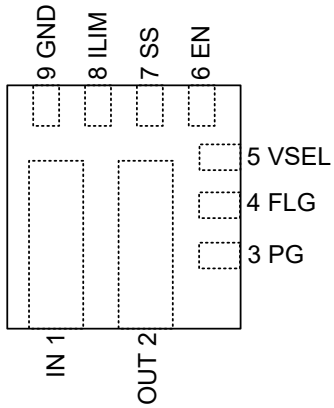
General Description

APL3561 is a programmable current limit switch with output voltage clamping. Extremely low $R_{DS(ON)}$ of the integrated protection N-channel FET helps to reduce power loss during the normal operation. Programmable soft-start time controls the slew rate of output voltage during the start-up time. This IC along with small VTQFN2x2-9 footprint provides small PCB area application.

Simplified Application Circuit



Pin Configuration



VTQFN2x2-9 (Top View)

Order and Marking Information

APL3561 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF : VTQFN2x2-9 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3561 QF: 3561 / X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note1)

Symbol	Parameter	Rating	Unit
	Voltage range on IN, VSEL, PG, FLG to GND	-0.3 to 18	V
	Output Voltage	-0.3 to 7	V
	Voltage range on SS, ILIM to GND	-0.3 to 3.6	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air	65	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air	6.5	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.5 ~ 5.5	V
	EN, VSEL,PG,PLG to GND Voltage	2.5 ~ 5.5	V
	SS, ILIM to GND Voltage	0 ~ 3.3	V
I_{OUT}	VOUT Output Current	5	A
R_{ILIM}	Current-limit threshold resistor range	2.2 ~ 11	kΩ
C_{SS}	Soft-Start Capacitor range	~ 100	nF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

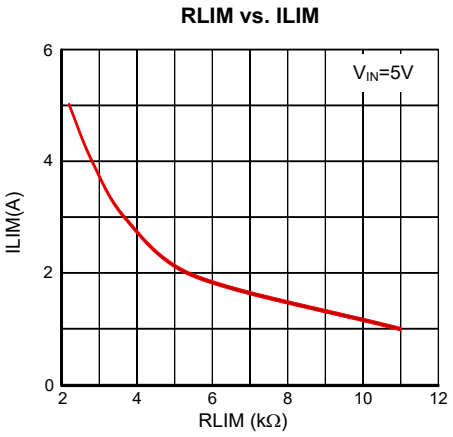
Note 3: Refer to the typical application circuit.

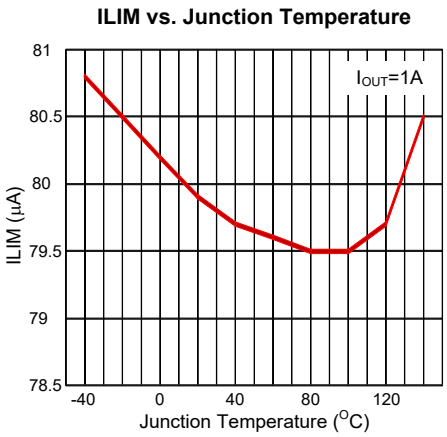
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=2.5V to 5.5V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C

Symbol	Parameter	Test Conditions		APL3561			Unit
				Min.	Typ.	Max.	
V_{IN}	Input Supply Voltage Range			2.5	-	5.5	V
SUPPLY CURRENT							
I_{SD}	Shutdown current	EN=0		-	-	10	μA
I_{BIAS}	Bias Current			-	70	-	μA
POWER SWITCH							
$R_{DS(ON)}$	Power Switch On Resistance	V_{IN}=3V, I_{OUT}=200mA, T_A= 25 °C		-	25	-	mΩ
UNDER-VOLTAGE LOCKOUT (UVLO)							
V_{IN}	VIN UVLO Threshold Voltage	V_{IN} rising, T_A= -40 ~ 85 °C		-	-	2.4	V
	VIN UVLO Hysteresis	V_{IN} falling		-	0.3	-	
OUTPUT VOLTAGE CLAMP (OUT)							
V_{CL}	Clamping Output Voltage	V_{SEL}=LOW		3.6	3.8	4	V
		V_{SEL}=HIGH		5.4	5.7	6	
CURRENT LIMIT							
I_{LIM}	Current Limit Threshold	V_{IN}=2.5V to 5.5V, T_A= -40 ~ 85 °C	R_{ILIM}=11kΩ	-	1	-	A
			R_{ILIM}=5.5kΩ	-	2	-	
			R_{ILIM}=4.4kΩ	-	2.5	-	
			R_{ILIM}=3.7kΩ	-	3	-	
			R_{ILIM}=3.1kΩ	-	3.5	-	
			R_{ILIM}=2.8kΩ	-	4	-	
			R_{ILIM}=2.4kΩ	-	4.5	-	
			R_{ILIM}=2.2kΩ	-	5	-	
	Current limit Accuracy	I_{LMT}=2A		-5	-	+5	%
POWER-OK INDICATOR							
V_{PGL}	PG Low Voltage	VIO=3.3V, ISINK=1mA		-	-	0.3	V
V_{PGLK}	PG Leakage Current	VIO=3.3V, PG high impedance		-	-	1	μA
V_{FAL}	FLG Low Voltage	VIO=3.3V, ISINK=1mA		-	-	0.3	V
V_{FALK}	FLG Leakage Current	VIO=3.3V, FLG high impedance		-	-	1	μA
	PG&FLG pull down resistance			-	100	-	Ω
REVERSE VOLTAGE PROTECT							
V_{RBT}	Reverse Current Block Threshold			-	50	-	mV
Soft Start Time							
T_{SS}	Vout=10%VIN to 90%VIN	V_{IN}=5V	C_{SS}=None	-	0.6	-	ms
			C_{SS}=10nF	-	2.3	-	
			C_{SS}=47nF	-	10.8	-	
			C_{SS}=100nF	-	23	-	
	Soft-start Time Accuracy			-30%	-	30%	T_{SST}
Control Pin Threshold							
V_{SEL_HI}	VSEL High Threshold			1	-	-	V
V_{SEL_LO}	VSEL Low Threshold			-	-	0.4	V
V_{EN_HI}	EN High Threshold			1	-	-	V
V_{EN_LO}	EN Low Threshold			-	-	0.4	V
OVERT-TEMPERATURE PROTECTION (OTP)							
T_{OTP}	Over-Temperature Threshold	T_J rising		-	150	-	°C
	Over-Temperature Hysteresis			-	20	-	

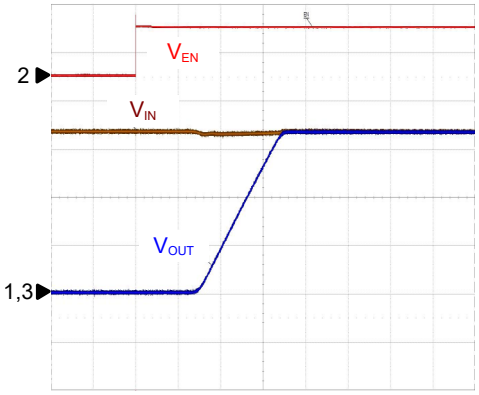
Typical Operating Characteristics





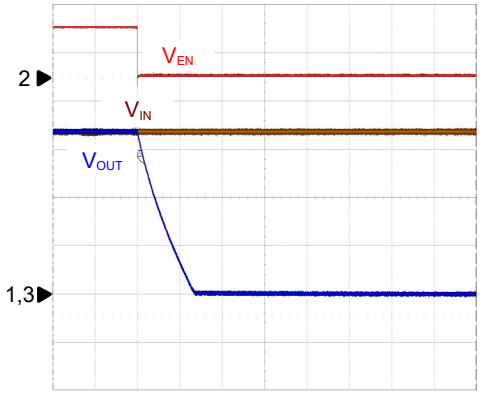
Operating Waveforms

Turn On Response



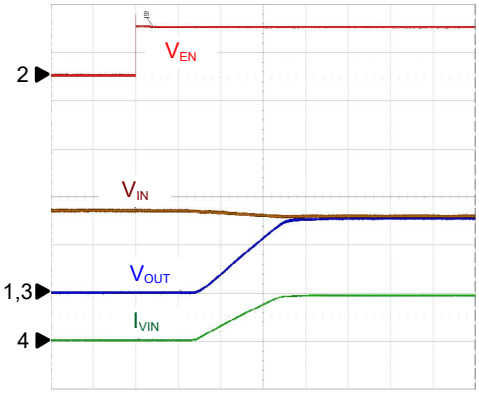
V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=0A
CH1:V_{IN},1V/Div, DC
CH2:V_{EN},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
TIME:200µs/Div

Turn Off Response



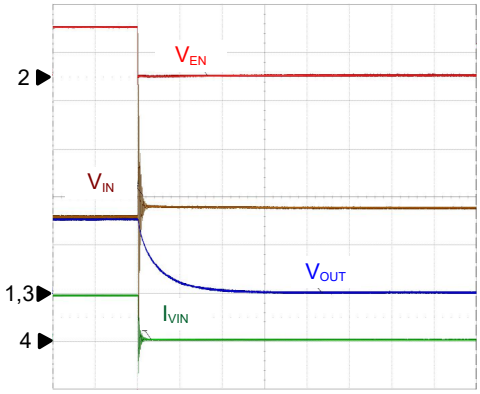
V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=50mA
CH1:V_{IN},1V/Div, DC
CH2:V_{EN},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
TIME:2ms/Div

Turn On Response



V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=5A
CH1:V_{IN},2V/Div, DC
CH2:V_{EN},5V/Div, DC
CH3:V_{OUT},2V/Div, DC
CH4:I_{VIN},5A/Div, DC
TIME:200µs/Div

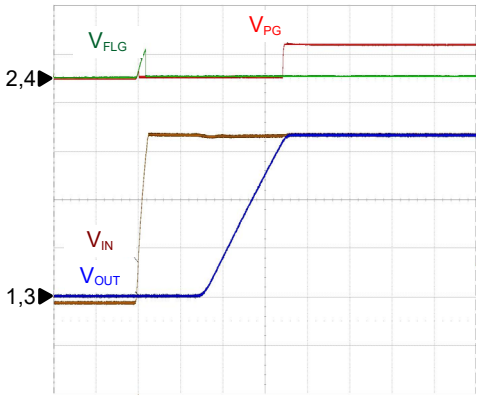
Turn Off Response



V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=5A
CH1:V_{IN},2V/Div, DC
CH2:V_{EN},5V/Div, DC
CH3:V_{OUT},2V/Div, DC
CH4:I_{VIN},5A/Div, DC
TIME:50µs/Div

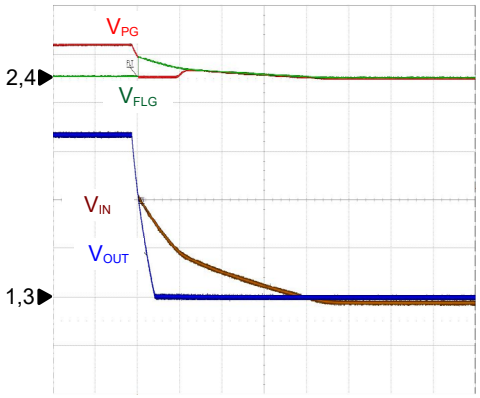
Operating Waveforms (Cont.)

UVLO at Rising



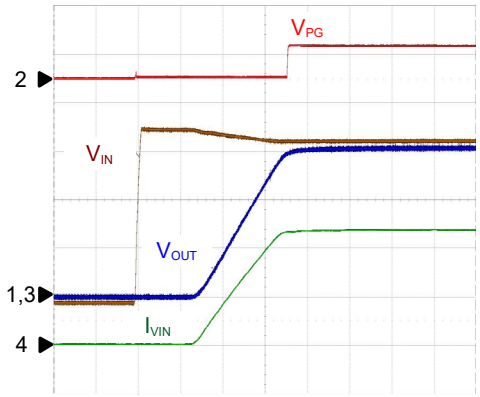
V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=0A
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:V_{FLG},5V/Div, DC
TIME:200µs/Div

UVLO at Falling



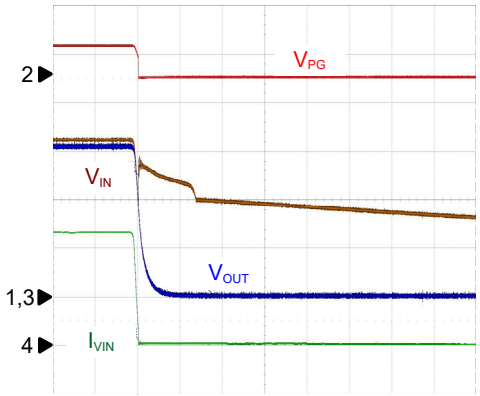
V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=50mA
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:V_{FLG},5V/Div, DC
TIME:5ms/Div

UVLO at Rising



V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=5A
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:I_{VIN},2A/Div, DC
TIME:200µs/Div

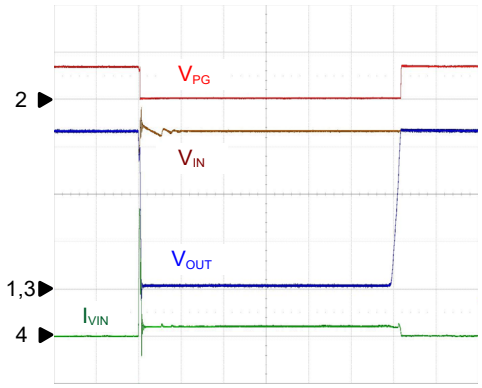
UVLO at Falling



V_{IN}=3.3V,C_{OUT}=44µF/Electrolytic,
C_{IN}=0.1µF/Electrolytic,I_{OUT}=5A
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:I_{VIN},2A/Div, DC
TIME:200µs/Div

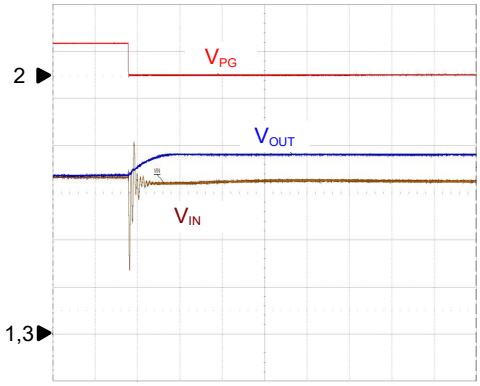
Operating Waveforms (Cont.)

Current Limit



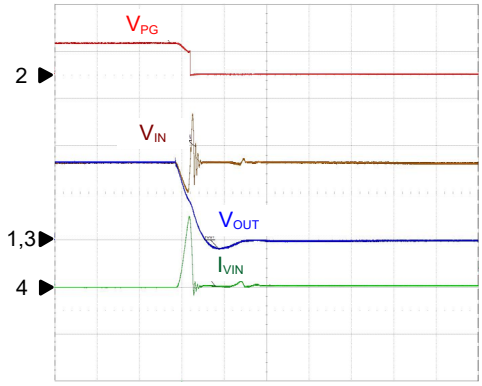
V_{IN}=3.3V,C_{OUT}=10μF/Electrolytic,
C_{IN}=10μF/Electrolytic,R_{ILIM}=2.2kΩ
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:I_{VIN},2A/Div, DC
TIME:500μs/Div

RCB



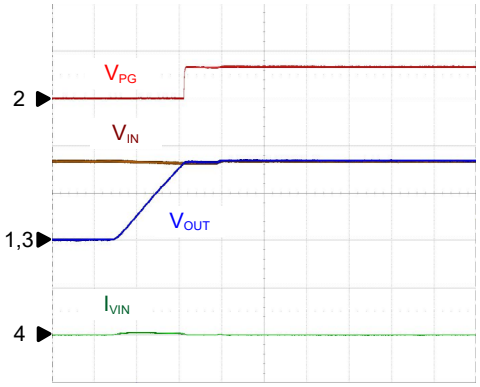
V_{IN}=3.3V,C_{OUT}=44μF/Electrolytic,
C_{IN}=0.1μF/Electrolytic
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
TIME:10μs/Div

Short Circuit



V_{IN}=3.3V,C_{OUT}=44μF/Electrolytic,
C_{IN}=0.1μF/Electrolytic,R_{ILIM}=2.2kΩ
CH1:V_{IN},2V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},2V/Div, DC
CH4:I_{VIN},5A/Div, DC
TIME:20μs/Div

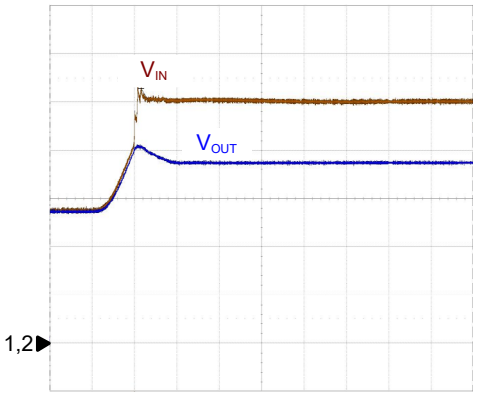
Short Circuit Release



V_{IN}=3.3V,C_{OUT}=44μF/Electrolytic,
C_{IN}=0.1μF/Electrolytic,R_{ILIM}=2.2kΩ
CH1:V_{IN},2V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},2V/Div, DC
CH4:I_{VIN},2A/Div, DC
TIME:200μs/Div

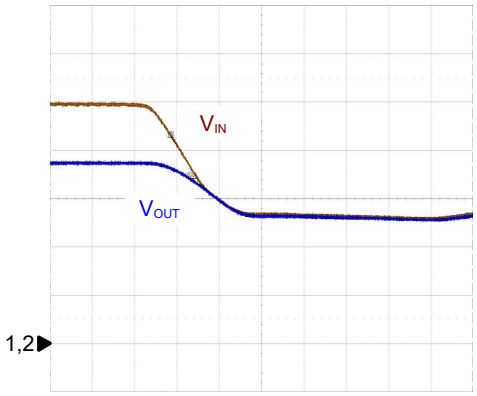
Operating Waveforms (Cont.)

VOUT Clamp



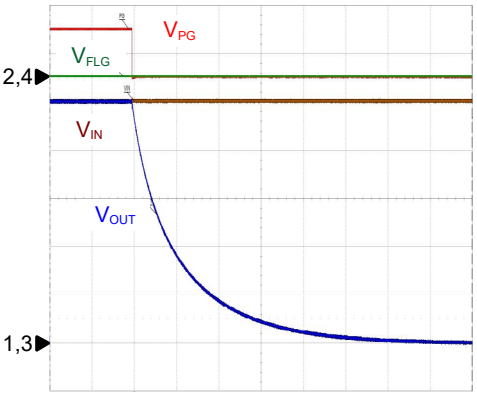
V_{IN}=3.3V,C_{OUT}=1μF/Electrolytic,
C_{IN}=1μF/Electrolytic,I_{OUT}=0.8A
CH1:V_{IN},1V/Div, DC
CH2:V_{OUT},1V/Div, DC
TIME:20μs/Div

VOUT Clamp Release



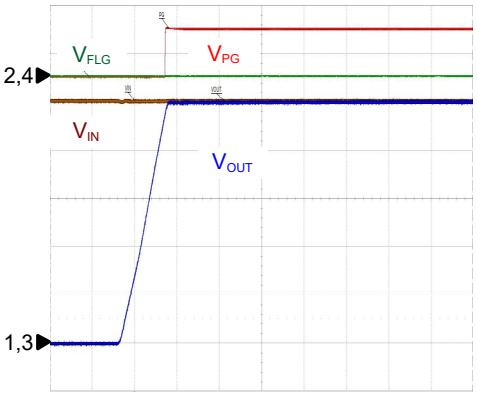
V_{IN}=3.3V,C_{OUT}=1μF/Electrolytic,
C_{IN}=1μF/Electrolytic,I_{OUT}=0.8A
CH1:V_{IN},1V/Div, DC
CH2:V_{OUT},1V/Div, DC
TIME:20μs/Div

Thermal SD



V_{IN}=5V,C_{OUT}=44μF/Electrolytic,
C_{IN}=0.1μF/Electrolytic,R_{LOAD}=100Ω
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:V_{FLG},5V/Div, DC
TIME:2ms/Div

Thermal SD Recovery

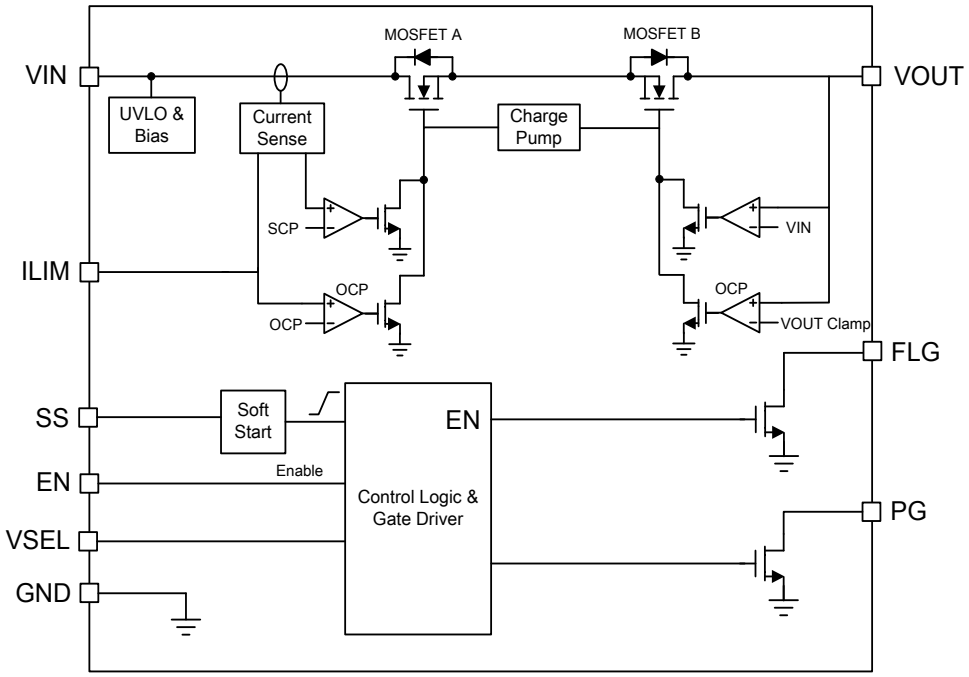


V_{IN}=5V,C_{OUT}=44μF/Electrolytic,
C_{IN}=0.1μF/Electrolytic,R_{LOAD}=100Ω
CH1:V_{IN},1V/Div, DC
CH2:V_{PG},5V/Div, DC
CH3:V_{OUT},1V/Div, DC
CH4:V_{FLG},5V/Div, DC
TIME:500μs/Div

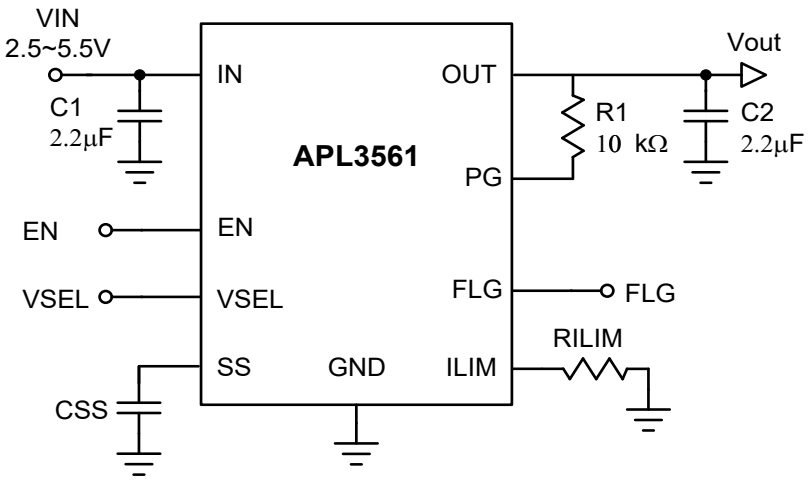
Pin Description

PIN		FUNCTION
NO. VTQFN2x2-9	NAME	
1	IN	Power input pin. Decouple high frequency noise by connecting at least 0.1uF MLCC to ground.
2	OUT	Output voltage pin.
3	PG	Open drain indicator pin. PG is pulled high when the output voltage is stablc in the normal.
4	FLG	Open drain indicator pin. FLG is pulled down when the input voltage larger than UVLO.
5	VSEL	Output clamp voltage selection based on the input voltage. Pull VSEL pin to High by connecting a resistor to IN, or pull VSEL pin to Low by connecting a resistor to ground.
6	EN	Pull high to enable. Do not leave it floating.
7	SS	Soft-start time program pin. Connect a capacitor to ground to program the soft start time. 600us(typ) for NC condition.
8	ILIM	Input current limit program pin. Connect a resistor between this pin and GND to program input current limit.
9	GND	Ground pin.

Block Diagram



Typical Application Circuit



Note: The C_{IN} is typically 2.2μF. However, the parasitic inductance before VIN pin could cause voltage spike to damage internal circuitry.If voltage spike, especially during short circuit or hot plug-in of large capacitance load, on VIN exceeds VIN's absolute maximum rating,adding at least 10μF/MLCC capacitor at VIN is strongly recommended.

Function Descriptions

Operation

The APL3561 is a current limited N-channel MOSFET power switch designed for high-side load-switching application, It incorporates back to back N-channel MOSFET, so the APL3561 prevents current flow from OUT to IN when being externally forced to a higher voltage than IN when chip is disable.

VIN Under-voltage Lockout (UVLO)

The APL3561 is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switches are N-channel MOSFETs with a low $R_{DS(ON)}$. Their body diodes are reversely connected in polarity with each other that can prevent a current flowing from the VOUT back to VIN and VIN to VOUT when IC is off.

Over Current Protection

The APL3561 supports Current limit programming. Connect a resistor R_{SET} from ILIM pin to ground to program the current limit:

$I_{LIM}=11000/R_{ILIM}(\Omega)$

The minimum current limit is 1A.
If the over current condition persists for a long time, the junction temperature may exceed 150°C, and over-temperature protection will shut down the part. Once the chip temperature drops below 110°C, the part will restart.

Over Voltage Protection

APL3561 integrated over voltage protection for input pin. The output voltage is clamped in 5.7V(typ.) when V_{SEL}=High or the output voltage is clamped in 3.8V(typ.) when V_{SEL}=Low, And the PG is pulled down when output voltage is clamped.

Revere Current Block

The APL3561 provides reverse current block function or RCB to prevent current flowing from VOUT to VIN. This function can emulate the internal MOSFET B as an ideal diode. In other words, the current is only allowed to flow from VIN to VOUT but forbidden from VOUT to VIN. During normal operation, if a voltage higher than V_{IN} appears at VOUT, the reverse current could generate a voltage drop between VOUT and VIN. When V_{OUT} - V_{IN}>50mV is triggered, the RCB function is activated then. There is another scenario when RCB can be activated. In normal operation if a short circuit happens at VIN, the RCB function can stop current flowing from VOUT to VIN, too.

When VOUT drop below VIN in RCB mode, the device immediately leaves the RCB mode and turns on MOS-B in 50us.When the VBUS greater than VIN, the device turn off MOS_B within 1us.

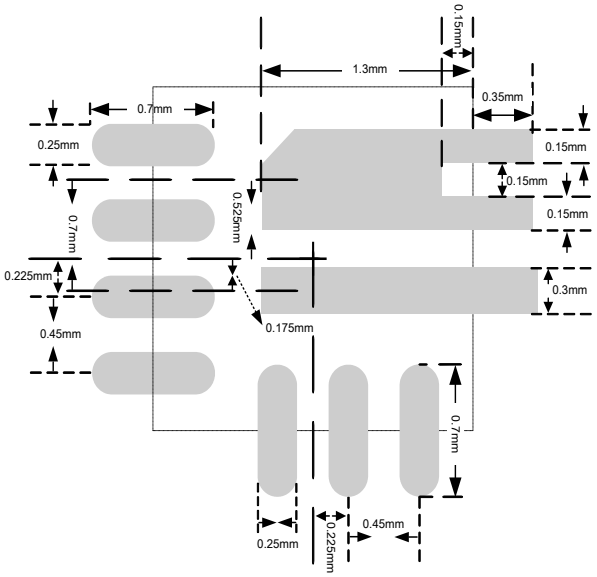
Supply Filter Capacitor

In order to prevent the input voltage drooping during hot-plug events, a 2.2μF ceramic capacitors from VIN to GND is strongly recommended. However, higher capacitor values could reduce the voltage droop on the input further. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A 2.2μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of output capacitor can be use to further reduce the voltage drop during high current application.

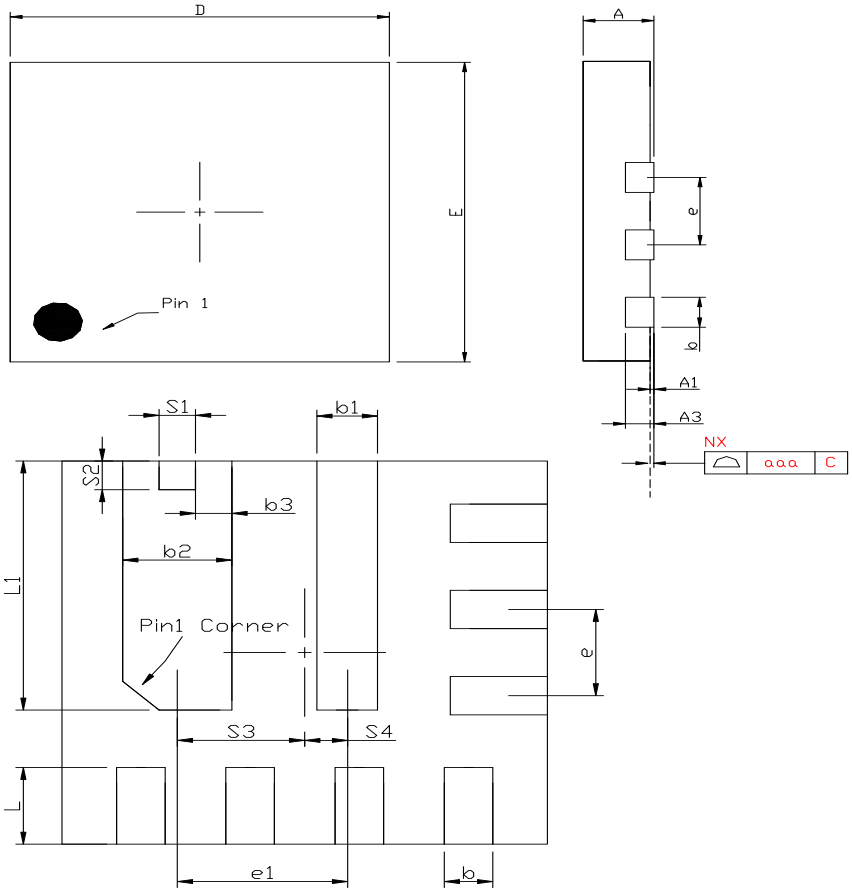
Recommended Minimum Footprint



VTQFN2x2-9

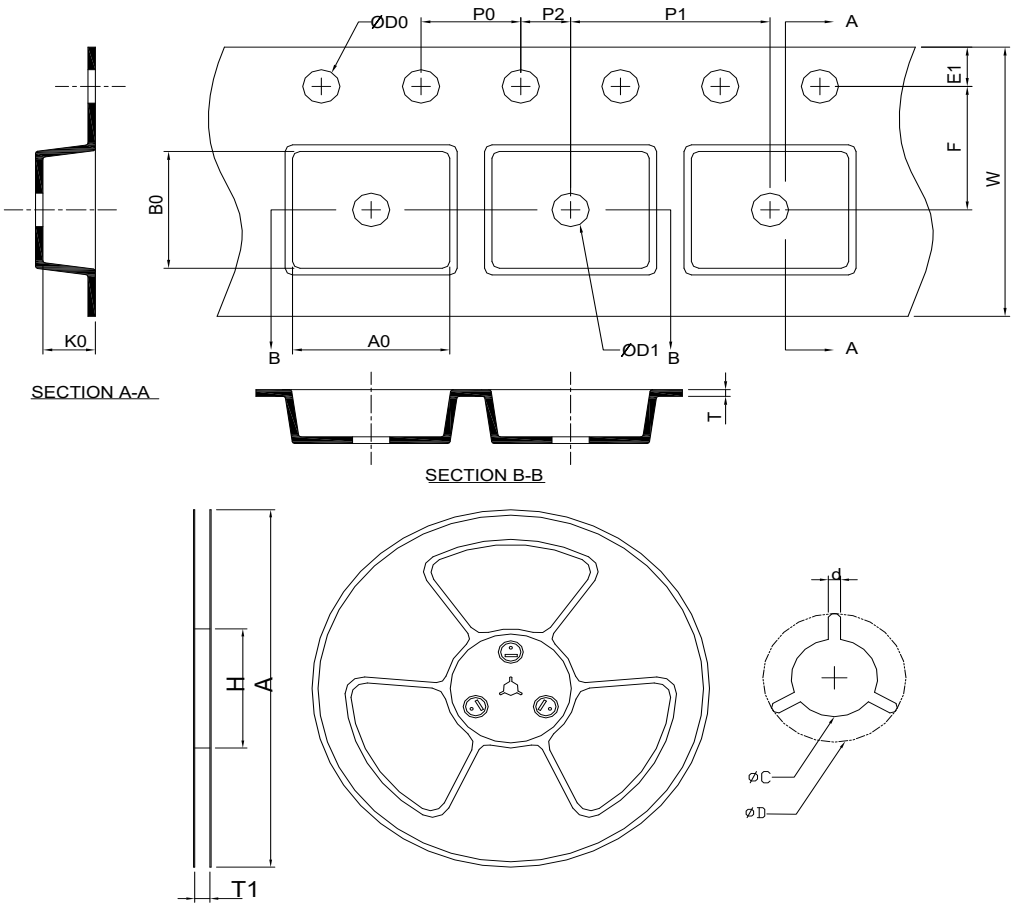
Package Information

VTQFN2x2-9



SYMBOL	VTQFN2*2-9			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.15	0.25	0.006	0.010
b1	0.20	0.30	0.008	0.012
b2	0.40	0.50	0.016	0.020
b3	0.10	0.20	0.004	0.008
D	1.90	2.10	0.075	0.083
E	1.90	2.10	0.075	0.083
e	0.45 BSC		0.018 BSC	
e1	0.70 BSC		0.028 BSC	
L	0.25	0.35	0.010	0.014
L1	1.25	1.35	0.049	0.053
S1	0.10	0.20	0.004	0.008
S2	0.10	0.20	0.004	0.008
S3	0.525 BSC		0.021 BSC	
S4	0.175 BSC		0.007 BSC	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN(2x2)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20±0.15	2.20±0.15	0.75±0.05

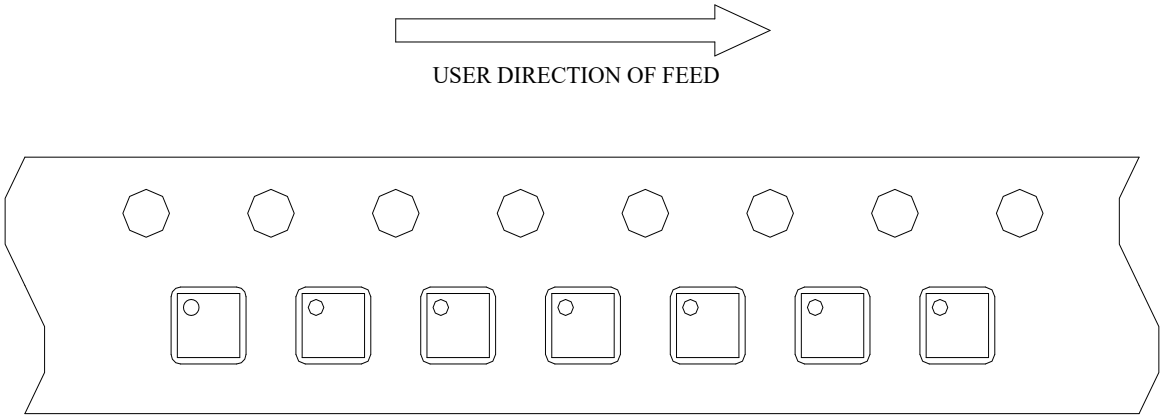
(mm)

Devices Per Unit

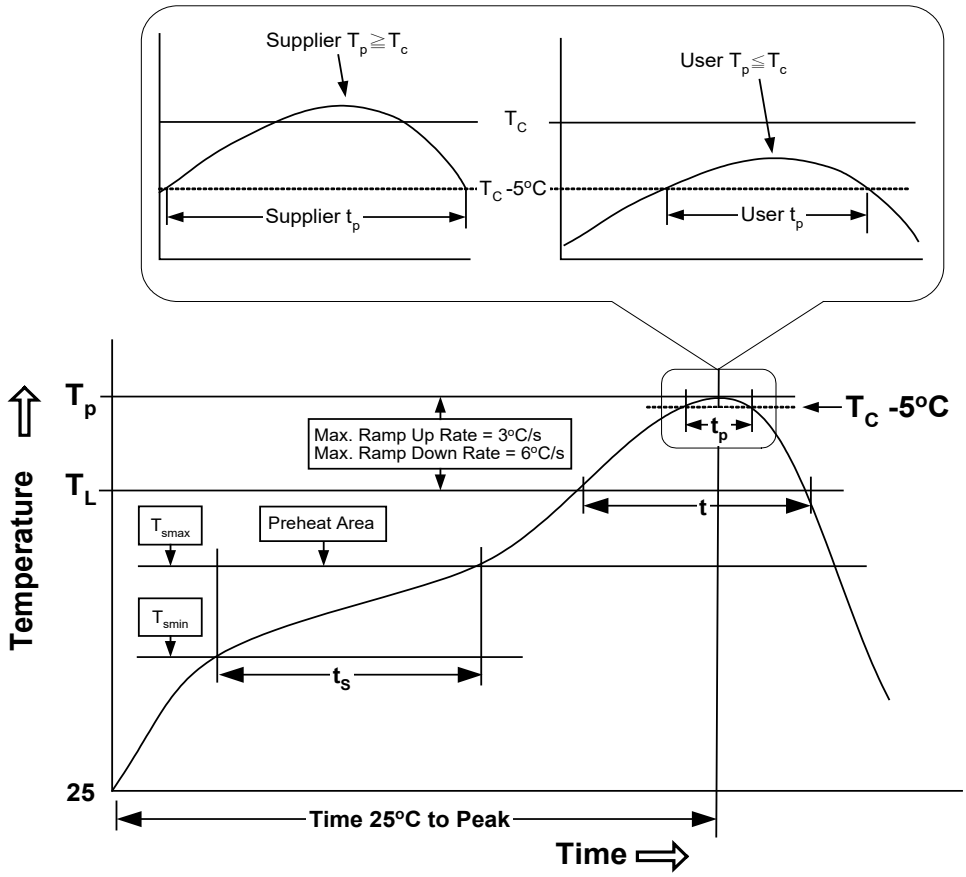
Package type	Packing	Quantity
VTQFN(2x2)	Tape & Reel	3000

Taping Direction Information

VTQFN2x2-9



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Duxing 1st Rd., East Dist.,
Hsinchu City 300096, Taiwan (R.O.C.)
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No.11, Ln. 218, Sec. 2, Zhongxing Rd., Xindian Dist.,
New Taipei City 231037, Taiwan (R.O.C.)
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838