Narrow VDC Buck-Boost Battery Charger with SMBus Interface Supporting USB OTG and USB PD EPR

Features

- **Narrow VDC Power Path Architecture**
- **Buck-Boost Charger for 2- to 4- Cell Li-ion Batteries**
- **Wide Input Voltage Range 3.9 to 30V**
- **Supports Bypass Mode to Connect System to Adapter**
- **Supports Autonomous Charging**
- **PROCHOT# Open-drain Output**
- **System Consumption Power Monitor (PSYS)**
- **Adapter and Battery Current Monitor (AMON/BMON)**
- **Integrates 8-bit ADC for Monitoring Key Parameters**
- **USB-C PD Fast Role Swap Support**
- **Two Level Adapter Current Limit**
- **Input Voltage Regulation**
- **Turbo Mode Support**
- **Trickle Charge Mode for Depleted Battery**
- **Battery Learn Mode**
- **Battery Shipping Mode**
- **Supports USB OTG**
- **Supports Supplemental Power Mode (V_{MIN} Active Protection)**
- **Adapter/System/Battery Over Voltage Protection**
- **Provides a General Purpose Comparator**
- **Supports JEITA Compliance Using an NTC**
- **SMBus Interface for Flexible Configuration**
- **TQFN4x4-32B 32 Pin Package**

Applications

- **Notebooks, Ultrabooks, Tablet PCs and Power Bank**
- **Portable Equipment with Rechargeable Batteries.**

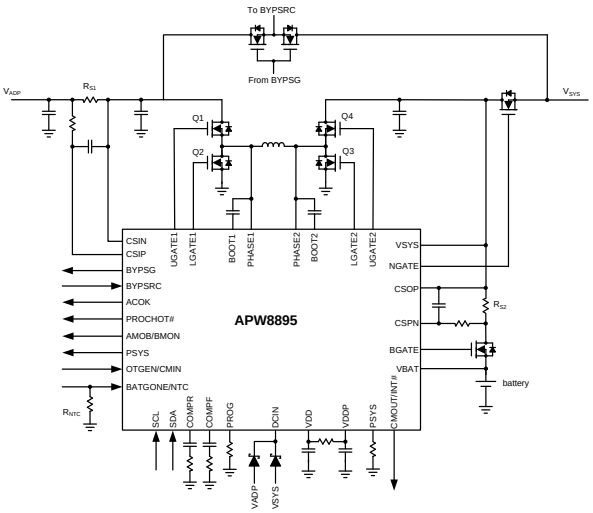
General Description

The APW8895 is a synchronous narrow VDC battery buck-boost charger controller. The buck-boost topology allows the use of 5V/12V/19V/28V or PD 20V adapter to charge 2- or 4- cell batteries. The PWM controller automatically transits modes between buck, buck-boost and boost mode based on the adapter and battery voltage. The APW8895 also supports USB OTG to provide 5 to 23.4V at USB port.

For system performance/power management, the APW8895 provides total system consumption power information through PSYS pin. Besides PSYS, it integrates two independent accurate current sense amplifiers to sense adapter current and battery current. The current information is reported at AMON/BMON pin. The host can set the ACProchot# and DCProchot# threshold to monitor the adapter and battery over current conditions. When the AC or DC Prochot# threshold is reached, a PROCHOT# signal is asserted, which can be used to notify the CPU to throttle its power consumption to the available power from adapter and battery.

The APW8895 has SMbus interface with one word (2 bytes) read/write protocols. Some critical settings, such as charging current, V_{SYS_MAX} voltage, adapter current limit threshold, etc., can be optimized for your applications.

Simplified Application Circuit

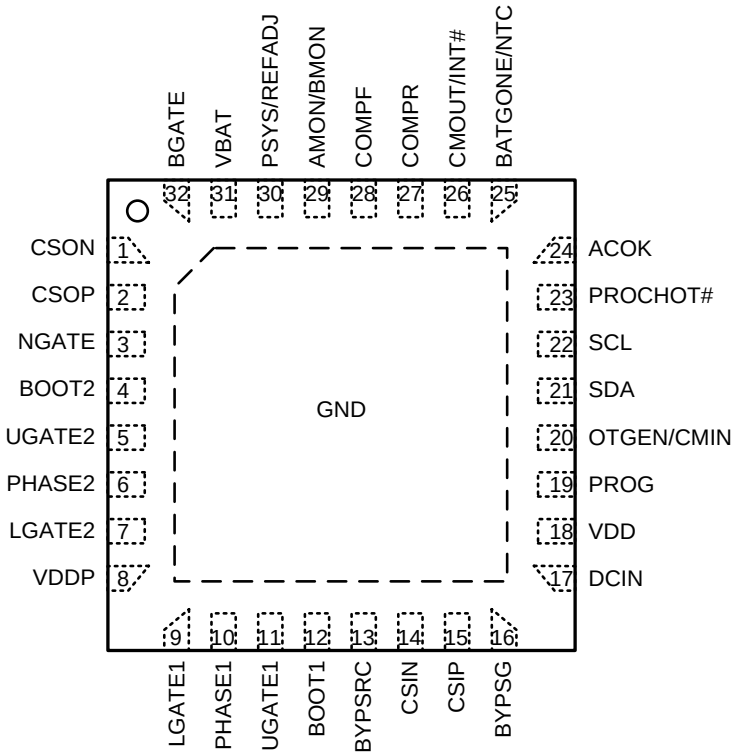


Ordering and Marking Information

APW8895 □□□ – □□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-32B Operating Junction Temperature I : - 40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW8895QB: 	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



TQFN4x4-32B
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
	CSIP, CSIN, DCIN, BYPSRC		-0.3 ~ 36	V
	PHASE1	pulse width > 20ns	-0.3 ~ 37	V
		pulse width < 20ns	-2 ~ 38	V
	PHASE2	pulse width > 20ns	-0.3 ~ 24	V
		pulse width < 20ns	-2 ~ 24	V
	BOOT1, UGATE1		-0.3 ~ VDDP+36	V
	BOOT2, UGATE2		-0.3 ~ 29	V
	BYPSG to BYPSRC, NGATE to CSOP, BGATE to VBAT		-0.3 ~ 6.5	V
	BOOT1 to PHASE1, BOOT2 to PHASE2		-0.3 ~ 6.5	V
	LGATE1, LGATE2		-0.3 ~ 6.5	V
	VDDP to LGATE1, VDDP to LGATE2		-0.3 ~ 6.5	V
	BOOT1 to UGATE1, BOOT2 to UGATE2		-0.3 ~ 6.5	V
	VBAT, VSYS, CSOP, CSON, BGATE		-0.3 ~ 24	V
	VDD, VDDP		- 0.3 ~ 6.5	V
	ACOK, AMON/BMON, PSYS		-0.3 ~ 6.5	V
	COMPF, COMPR, OTGEN/CMIN, BATGONE, PROG		-0.3 ~ 6.5	V
	SDA, SCL, PROCHOT#, CMOUT/INT#		-0.3 ~ 6.5	V
	CSIP to CSIN, CSOP to CSON		-0.3 ~ 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 175	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C
ESD Rating	Human Body Model		2.5	kV
	Charged Device Model		1	kV
	Latch-up		100	mA

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	43	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
	Adapter Voltage	3.9 ~ 30	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
BATTERY CURRENT AND QUIESCENT CURRENT						
I_{BAT1}	Battery Supply Current	V_{VBAT}=8.4V, battery only, BGATE off, NGATE off, GPCOMP off, PSYS off, BMON off, $I_{BAT1}=I_{VBAT}+I_{CSOP}+I_{CSON}+I_{DCIN}$	5	20	30	μA
I_{BAT2}		V_{VBAT}=16.8V, battery only, BGATE on, NGATE on, GPCIMP on, PSYS off, BMON off, $I_{BAT2}=I_{VBAT}+I_{CSOP}+I_{CSON}+I_{DCIN}$	15	30	55	μA
I_{BAT3}		V_{VBAT}=16.8V, battery only, BGATE on, NGATE on, GPCIMP on, PSYS on, BMON on, ADC on, $I_{BAT3}=I_{VBAT}+I_{CSOP}+I_{CSON}+I_{DCIN}$	700	1100	1200	μA
I_{Q1}	Quiescent Current	VSYS state, no switching, V_{VBAT}=12.6V, V_{ADP}=20V, I_{Q1} = $I_{VBAT}+I_{CSOP}+I_{CSON}+I_{DCIN}+I_{PH1}+I_{PH2}+I_{CSIP}+I_{CSIN}+I_{BYPSRC}$	2	2.2	2.35	mA
I_{Q2}		OTG state, no switching, V_{VBAT}=8.4V, V_{OTG}=5V, I_{Q2} = $I_{VBAT}+I_{CSOP}+I_{CSON}+I_{DCIN}+I_{PH1}+I_{PH2}+I_{CSIP}+I_{CSIN}+I_{BYPSRC}$	1.5	1.7	1.85	mA
UVLO AND ACOK						
$V_{ADPACOK\_R}$	V_{ADP} (CSIN) ACOK Rising Threshold		3.51	3.6	3.69	V
$V_{ADPACOK\_HYS}$	V_{ADP} (CSIN) ACOK Hysteresis		60	120	180	mV
V_{BAT5P2_R}	VBAT 5P2V Rising Threshold		4.95	5.2	5.65	V
V_{BAT5P2_HYS}	VBAT 5P2V Hysteresis		-	490	-	mV
V_{VDD2P7_R}	VDD 2.7V SMBUS and BGATE/BMON POR Rising Threshold		2.5	2.7	2.9	V
V_{VDD2P7_HYS}	VDD 2.7V POR Hysteresis		-	150	-	mV
V_{VDD3P8_R}	VDD 3.8V Analog, Gate Driver POR Rising Threshold		3.6	3.8	4	V
V_{VDD3P8_HYS}	VDD 3.8V POR Hysteresis		-	150	-	mV
	ACOK Input Leakage Current		-	-	1	μA
	ACIN Output Sink Current	V_{ACOK}=0.4V	4	-	-	mA
5V LDO REGULATOR						
V_{VDD}	VDD Output Voltage	6V<V_{DCIN}<23V, no load	4.5	5	5.5	V
V_{VDD_DP}	VDD Dropout Voltage	V_{DCIN}=4V, I_{LOAD}=30mA	-	85	-	mV
I_{VDD_OC}	VDD Over-Current Threshold		80	115	165	mA
ADAPTER CURRENT REGULATION						
I_{CIC}	Adapter Current Regulation Accuracy (RS1=20mΩ)	Reg0x3Fh=0x0FA0h (4A) Reg0x3Bh=0x0FA0h (4A)	-2.25	-	2.25	%
		Reg0x3Fh=0x07D0h (2A) Reg0x3Bh=0x07D0h (2A)	-2.5	-	2	%
		Reg0x3Fh=0x01F4h (0.5A) Reg0x3Bh=0x01F4h (0.5A)	-10	-	10	%
I_{ACHOT}	Adapter Current PROCHOT# Threshold (RS1=20mΩ)	Reg0x47h=0x1580h (5504mA)	-1.5	-	1.5	%
		Reg0x47h=0x0A80h (2688mA)	-3.0	-	3.0	%
		Reg0x47h=0x0400h (1024mA)	-6.0	-	6.0	%
SYSTEM RENT REGULATION						
V_{SYS_MAX}	Maximum System Voltage Accuracy	Reg0x15h=0x20C0 h (8.384V)	-0.6	-	0.6	%
		Reg0x15h=0x3120h (12.576V)	-0.5	-	0.5	%
		Reg0x15h=0x4180h (16.768V)	-0.5	-	0.5	%
V_{SYS_MIN}	Minimum System Voltage Accuracy		-3	-	3	%
	Input Voltage Regulation Accuracy	Reg0x4Bh=0x0C00h (4.096V)	3.98	-	4.22	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25 °C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
BATTERY CHARGE CURRENT REGULATION						
I_{CC}	Battery Charge Current Accuracy (RS2=10mΩ)	Reg0x14h=0x1770h (6A)	-2	-	2	%
		Reg0x14h=0x07D0h (2A)	-4	-	4	%
		Reg0x14h=0x03E8h (1A)	-6	-	6	%
		Reg0x14h=0x01F4h (0.5A)	-12	-	12	%
CHARGE PUMP GATE DRIVER						
	BYPSG Drive Current	BYPSG off, V_{BYPSG} = V_{BYPSRC} + 2V	165	190	215	μA
		BYPSG on, V_{BYPSG} = V_{BYPSRC} + 2V, V_{BYPSRC} > 3.9V	15	40	70	μA
	NGATE Drive Current	NGATE off, V_{NGATE} = V_{CSOP} + 2V	165	190	215	μA
		NGATE on, V_{NGATE} = V_{CSOP} + 2V, V_{CSOP} > 3.9V	15	40	70	μA
	BGATE Drive Current	BGATE off, V_{BGATE} = V_{VBAT} + 2V	165	190	215	μA
		BGATE on, V_{BGATE} = V_{VBAT} + 2V, V_{VBAT} > 2.7V	15	40	70	μA
TRICKLE CHARGE CURRENT REGULATION						
$I_{TRICKLE}$	Trickle Charge Current Accuracy (RS2=10mΩ)	Reg0x3Dh[15:13]=001b (64mA)	20	64	100	mA
		Reg0x3Dh[15:13]=010b (96mA)	55	96	135	mA
		Reg0x3Dh[15:13]=011b (128mA)	80	128	170	mA
		Reg0x3Dh[15:13]=100b (160mA)	112	160	208	mA
		Reg0x3Dh[15:13]=101b (192mA)	134	192	250	mA
		Reg0x3Dh[15:13]=110b (224mA)	157	224	291	mA
		Reg0x3Dh[15:13]=111b (256mA)	180	256	333	mA
END OF CHARGE CURRENT						
I_{EOC}	End of Charge Current (RS2=10mΩ, Autonomous Charging)	Reg0x38h[9:8]=00b (105mA)	40	105	170	mA
		Reg0x38h[9:8]=01b (55mA)	5	55	120	mA
		Reg0x38h[9:8]=10b (190mA)	120	190	270	mA
		Reg0x38h[9:8]=11b (145mA)	75	145	230	mA
AUTO RECHARGE THRESHOLD						
	Auto Recharge Threshold (Relative to Maximum System Voltage)	2-cell battery	-	430	-	mV
		3-cell battery	-	600	-	mV
		4-cell battery	-	700	-	mV
IDEAL DIODE MODE						
	Entering Ideal Diode Mode Threshold	BGATE off, V_{VSYS} falling, V_{VBAT} - V_{VSYS}	110	180	255	mV
	Exiting Ideal Diode Mode Threshold	R_{S2}=10mΩ, detect battery discharging current (with de-bounce time 40ms)	25	125	230	mA
		R_{S2}=10mΩ, detect battery charging current (without de-bounce time)	60	160	255	mA
INPUT CURRENT SENSE AMPLIFIER						
	CSIP/CSIN Input Voltage Range		4	-	23	V
	AMON GAIN		-	17.97	-	V/V
	AMON Accuracy (RS1=20mΩ) (V_{AMON}=AMON Gain*(V_{CSIP} - V_{CSIN})	V_{CSIP}-V_{CSIN}=100mV (5A)	-2.5	-	2.5	%
		V_{CSIP}-V_{CSIN}=20mV (1A)	-5.5	-	5.5	%
		V_{CSIP}-V_{CSIN}=10mV (0.5A)	-12	-	12	%
		V_{CSIP}-V_{CSIN}=2mV (0.1A)	-55	-	55	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
BATTERY CURRENT SENSE AMPLIFIER						
	Reverse AMON GAIN		-	17.9	-	V/V
	Reverse AMON Accuracy (RS1=20mΩ) (V_{AMON}=Reverse AMON gain*(V_{CSIN}-V_{CSIP})	V_{CSIN}-V_{CSIP}=80mV (4A)	-3.5	-	3.5	%
		V_{CSIN}-V_{CSIP}=20mV (1A)	-6.5	-	6.5	%
		V_{CSIN}-V_{CSIP}=10mV (0.5A)	-12	-	12	%
		V_{CSIN}-V_{CSIP}=5.12mV (0.256A)	-25	-	25	%
	AMON Minimum Output Voltage	V_{CSIP}-V_{CSIN}=0V	-	-	30	mV
	BMON GAIN (Charging)		-	35.78	-	V/V
	BMON Accuracy (RS1=20mΩ) (V_{BMON}=BMON Gain*(V_{CSON}-V_{CSOP})	V_{CSOP}-V_{CSON}=60mV (6A), V_{CSON}=8V	-3	-	3	%
		V_{CSOP}-V_{CSON}=40mV (4A), V_{CSON}=8V	-4	-	4	%
		V_{CSOP}-V_{CSON}=10mV (1A), V_{CSON}=8V	-10	-	10	%
		V_{CSOP}-V_{CSON}=5mV (0.5A), V_{CSON}=8V	-25	-	25	%
	Reverse BMON GAIN (Discharging)		-	17.97	-	V/V
	Reverse BMON Accuracy (RS2=10mΩ) (V_{BMON}=Reverse BMON gain*(V_{CSON}-V_{CSOP})	V_{CSON}-V_{CSOP}=100mV (10A), V_{CSON}=8V	-2	-	2	%
		V_{CSON}-V_{CSOP}=20mV (2A), V_{CSON}=8V	-6	-	6	%
		V_{CSON}-V_{CSOP}=10mV (1A), V_{CSON}=8V	-10	-	10	%
		V_{CSON}-V_{CSOP}=6mV (0.6A), V_{CSON}=8V	-20	-	20	%
	BMON Minimum Output Voltage	V_{CSOP}-V_{CSON}=0V	-	-	30	mV
	Battery Discharge Current PROCHOT# Threshold (DCProchot)	R_{S2}=10mΩ, Reg0x48h=0x0800h (2.048A)	1.77	2.08	2.39	A
		R_{S2}=10mΩ, Battery only, Reg0x39h[4:3]=11b (6A)	4.5	6	8	A
		R_{S2}=10mΩ, Battery only, Reg0x39h[4:3]=00b (12A)	9.4	13	17	A
	AMON/BMON Source Resistance (Note 4)		-	-	5	Ω
	AMON/BMON Sink Resistance (Note 4)		-	-	5	Ω
OTGEN AND BATGONE INPUT PIN						
	OTGEN High-Level Input Voltage		0.9	-	-	V
	OTGEN Low-Level Input Voltage		-	-	0.4	V
	BATGONE High-Level Input Voltage		VDD-0.6	-	-	V
	BATGONE Low-Level Input Voltage		-	-	VDD-1.2	V
	Pull-up Current	V_{OTGEN}=5V, $V_{BATGONE}$=5V	-	1	-	μA
	NTC Step1 Pull-up Current		62	65	68	μA
	NTC Step2 Pull-up Current		126	130	134	μA
	NTC Step3 Pull-up Current		250	260	270	μA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
PROCHOT# OUTPUT PIN						
	PROCHOT# Debounce Time	Reg0x3Dh[10:9]=11b	0.85	1	1.15	ms
		Reg0x3Dh[10:9]=10b	0.425	0.5	0.575	ms
	PROCHOT# Duration Time	Reg0x3Dh[8:6]=001b	17	20	23	ms
		Reg0x3Dh[8:6]=000b	8.5	10	11.5	ms
	Low VSYS PROCHOT# Trip Threshold	Reg0x3Ch[2:0]=000b	5.3	5.5	5.7	V
		Reg0x3Ch[2:0]=001b	5.5	5.5	5.9	V
		Reg0x3Ch[2:0]=010b	5.7	5.9	6.1	V
		Reg0x3Ch[2:0]=011b	5.9	6.1	6.3	V
		Reg0x3Ch[2:0]=100b	6.1	6.3	6.5	V
		Reg0x3Ch[2:0]=101b	6.3	6.5	6.7	V
		Reg0x3Ch[2:0]=110b	6.5	6.7	6.9	V
		Reg0x3Ch[2:0]=111b	6.7	6.9	7.1	V
	PROCHOT# Input Leakage Current		-	-	1	μA
	PROCHOT# Output Sink Current	V_{ACOK}=0.4V	4	-	-	mA
PSYS OUTPUT PIN						
	PSYS Output Current (R_{S1}=20mΩ, R_{S2}=10mΩ, Reg0x4Eh[11]=0b)	Reg0x4Ch[9:8]=11b (0.646uA/W), VCSIP=12V, V_{CSIP}-V_{CSIN}=80mV, V_{VBAT}=12V, V_{CSOP}-V_{CSON}=0mV, IPSYS=PSYS Gain*(system power)	-5	-	5	%
		Reg0x4Ch[9:8]=11b (0.646uA/W), VCSIP=20V, V_{CSIP}-V_{CSIN}=0mV, V_{VBAT}=8.4V, V_{CSOP}-V_{CSON}=50mV, IPSYS=PSYS Gain*(system power)	-5	-	5	%
		Reg0x4Ch[9:8]=11b (0.646uA/W), VCSIP=20V, V_{CSIP}-V_{CSIN}=80mV, V_{VBAT}=12V, V_{CSOP}-V_{CSON}=20mV, IPSYS=PSYS Gain*(system power)	-5	-	5	%
		Reg0x4Ch[9]=1b (0.723uA/W), battery only, V_{VBAT}=12.6V, V_{CSOP}-V_{CSON}=-10mV, IPSYS=PSYS Gain*(system power)	-15	-	15	%
	Maximum PSYS Output Voltage		4	-	-	V
	PSYS Gain (R_{S1}=20mΩ, R_{S2}=10mΩ, Reg0x4Eh[11]=0b)	Reg0x4Ch[9:8]=00b, 0μA < IPSYS < 110μA, Offset=1.352μA	-	0.896	-	μA/W
		Reg0x4Ch[9:8]=01b, 0μA < IPSYS < 100μA, Offset=2.047μA	-	1.315	-	μA/W
		Reg0x4Ch[9:8]=10b, 0μA < IPSYS < 90μA, Offset=0.626μA	-	0.431	-	μA/W
		Reg0x4Ch[9:8]=11b, 0μA < IPSYS < 80μA, Offset=0.959μA	-	0.646	-	μA/W
	PSYS Gain (R_{S1}=10mΩ, R_{S2}=10mΩ, Reg0x4Eh[11]=1b)	Reg0x4Ch[9:8]=00b, 0μA < IPSYS < 110μA, Offset=1.773μA	-	0.907	-	μA/W
		Reg0x4Ch[9:8]=01b, 0μA < IPSYS < 100μA, Offset=2.654μA	-	1.337	-	μA/W
		Reg0x4Ch[9:8]=10b, 0μA < IPSYS < 90μA, Offset=0.831μA	-	0.434	-	μA/W
		Reg0x4Ch[9:8]=11b, 0μA < IPSYS < 80μA, Offset=1.265μA	-	0.653	-	μA/W

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
USB OTG						
	OTG Voltage	Reg0x49h=0x0D08h (5.004V)	4.93	5	5.25	V
	OTG Current Limit Threshold (R_{S1}=20mΩ)	Reg0x4Ah=0x0200h (512mA)	450	512	585	mA
		Reg0x4Ah=0x0400h (1024mA)	960	1024	1100	mA
		Reg0x4Ah=0x1000h (4096mA)	3975	4096	4240	mA
	Fast Role Swap Digital Filter (Note 4)	When configured OTG_EN from 0 to 1	-	-	1	μs
	Analog Support of OTG Output (Note 4)	When configured OTG_EN=1	-	-	150	μs
GENERAL PURPOSE COMPARATOR						
	General Purpose Comparator Rising Threshold	Reg0x3D[4]=0b (1.2V)	1.15	1.2	1.25	V
		Reg0x3D[4]=1b (2V) (not available in battery only mode)	1.95	2	2.05	V
	General Purpose Comparator Hysteresis	Reg0x3D[4]=0b or Reg0x3D[4]=1b	25	40	50	mV
	CMOUT/INT# Input Leakage Current		-	-	1	μA
	CMOUTIN# Output Sink Current	V_{CMOUT}=0.4V	4	-	-	mA
PROTECTION						
	VSYS Over-voltage Rising Threshold	V_{VSYS_MAX}=8.4V	8.9	9.15	9.35	V
	VSYS Over-voltage Hysteresis		250	400	550	mV
	VSYS OK Threshold		0.45	0.6	0.75	V
	VSYS OK Source Current		-	10	-	mA
	Adapter Way Overcurrent Rising Threshold (Note 4)	R_{S1}=20mΩ	7.5	12	25	A
	Battery Discharge Overcurrent Rising Threshold (Note 4)	R_{S2}=10mΩ	9	20	38	A
	Over Temperature Threshold (Note 4)		140	150	160	℃
	Adapter Over-voltage Rising Threshold	APW8895	22.5	23.4	24	V
		APW8895A	-	33.3	-	V
	Adapter Over-voltage Hysteresis		-	400	-	mV
	OTG Under-voltage Falling Threshold	Reg0x49h=0x0D08h (OTG Voltage=5.004V)	3.45	3.8	4.25	V
	OTG Over-voltage Rising Threshold	Reg0x49h=0x0D08h (OTG Voltage=5.004V)	5.8	6.2	6.6	V
OSCILLATOR						
	Oscillator Frequency, Digital Core Only		0.85	1	1.15	MHz
	Digital Debounce Time Accuracy (Note 4)		-15	-	15	%
BATTERY LEARN MODE						
	Switching Frequency Accuracy		-15	-	15	%
	Battery Learn Mode Auto-Exit Threshold	V_{VSYS_MIN}=5.376V, Reg0x3Ch[13]=1b	5.05	5.35	5.7	V
	Battery Learn Mode Auto-Exit Hysteresis (Note 4)		180	330	480	mV
SDA, SCL PINS						
	SDA/SCL Input Low Voltage		-	-	0.7	V
	SDA/SCL Input High Voltage		1.5	-	-	V
	SDA/SCL Input Bias Current	V=3.3V	-	-	1	μA
	SDA Sink Current	V_{SDA}=0.4V, on	4	-	-	mA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CSIP}=V_{CSIN}=5V and 20V, V_{SYS}=V_{VBAT}=V_{CSOP}=V_{CSON}=8V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW8895			Unit
			Min.	Typ.	Max.	
GATE DRIVER						
	UGATE1 Pull-up Resistance	100mA source current	-	0.8	1.2	Ω
	UGATE1 Source Current	V_{BOOT1}-V_{UGATE1}=2.5V	1.3	2	-	A
	UGATE1 Pull-down Resistance	100mA sink current	-	0.35	0.475	Ω
	UGATE1 Sink Current	V_{UGATE1}-V_{PHASE1}=2.5V	1.9	2.8	-	A
	LGATE1 Pull-up Resistance	100mA source current	-	0.8	1.2	Ω
	LGATE1 Source Current	V_{VDDP}-V_{LGATE1}=2.5V	1.3	2	-	A
	LGATE1 Pull-down Resistance	100mA sink current	-	0.3	0.45	Ω
	LGATE1 Sink Current	V_{LGATE1}-V_{GND}=2.5V	2.3	3.5	-	A
	UGATE2 Pull-up Resistance	100mA source current	-	0.8	1.2	Ω
	UGATE2 Source Current	V_{BOOT2}-V_{UGATE2}=2.5V	1.3	2	-	A
	UGATE2 Pull-down Resistance	100mA sink current	-	0.3	0.45	Ω
	UGATE2 Sink Current	V_{UGATE2}-V_{PHASE2}=2.5V	2.3	3.5	-	A
	LGATE2 Pull-up Resistance	100mA source current	-	0.8	1.2	Ω
	LGATE2 Source Current	V_{VDDP}-V_{LGATE2}=2.5V	1.3	2	-	A
	LGATE2 Pull-down Resistance	100mA sink current	-	0.3	0.45	Ω
	LGATE2 Sink Current	V_{LGATE2}-V_{GND}=2.5V	2.3	3.5	-	A
	UGATEx to LGATEx Dead Time		10	20	40	ns
	LGATEx to UGATEx Dead Time		10	20	40	ns
SMBUS TIMING						
	SMBus Frequency Range		10	-	400	kHz
	Bus Free Time		4.7	-	-	μs
	Start Condition Hold Time from SCL		4	-	-	μs
	Start Condition Set-up Time from SCL		4.7	-	-	μs
	Stop Condition Set-up Time from SCL		4	-	-	μs
	SDA Hold Time From SCL		300	-	-	μs
	SDA Set-up Time from SCL		250	-	-	μs
	SCL Low Period		4.7	-	-	μs
	SCL High Period		4	-	-	μs
	SMBus Inactivity Timeout (Note 4)	Maximum Charging Period without a SMBus Write to Max System Voltage or Charge Current register, Reg4C[12:11]=00b	-	175	-	sec

Note 4: Guaranteed by design, not production tested.

Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	CSON	The negative input pin of the error amplifier for battery charge/discharge current sense.
2	CSOP	The positive input pin of the error amplifier for battery charge/discharge current sense.
3	NGATE	The gate driver output pin for driving an external N-channel MOSFET. When the NGATE is enabled via SMBus, the NGATE pin output voltage is V_{CSOP}+5V. If the NGATE is not used, leave this pin floating.
4	BOOT2	The high-side gate driver supply voltage input pin of buck-boost charger phase 2. A 0.22μF X5R ceramic capacitor is connected from this pin to the PHASE2 pin to provide a bootstrap voltage for the gate driver to drive the upper N-MOSFET.
5	UGATE2	The high-side gate driver output pin of the buck-boost charger's phase 2. The UGATE2's output voltage is supplied from BOOT2.
6	PHASE2	Current return path for the high-side gate driver of the buck-boost charger's phase 2. This node is also used to detect zero-cross current of phase 2. Connect this node to the junction of the high side power MOSFET Q4's source and the low side power MOSFET Q3's drain.
7	LGATE2	The low-side gate driver output pin of the buck-boost charger's phase 2.
8	VDDP	Power supply for the gate drivers. Connect to VDD pin through a R/C filter 4.7Ω/10μF.
9	LGATE1	The low-side gate driver output pin of the buck-boost charger's phase 1.
10	PHASE1	Current return path for the high-side gate driver of the buck-boost charger's phase 1. This node is also used to detect zero-cross current of phase 1. Connect this node to the junction of the high side power MOSFET Q1's source and the low side power MOSFET Q2's drain.
11	UGATE1	The high-side gate driver output pin of the buck-boost charger's phase 1. The UGATE1's output voltage is supplied from BOOT1.
12	BOOT1	The high-side gate driver supply voltage input pin of buck-boost charger phase 1. A 0.22μF X5R ceramic capacitor is connected from this pin to the PHASE2 pin to provide a bootstrap voltage for the gate driver to drive the upper N-MOSFET.
13	BYPSRC	The input reference for the external bypass FETs' source terminals. If the Bypass mode is used, connect this pin to the bypass N-channel MOSFET source terminals. Otherwise, connect this pin to VDDP if Bypass mode function is not used.
14	CSIN	The negative input pin of the error amplifier for adapter output/OTG output current sense.
15	CSIP	The positive input pin of the error amplifier for adapter output/OTG output current sense.
16	BYPSG	Gate driver output pin for driving the external bypass MOSFETs. Connect this pin to the gate of the external bypass N-channel MOSFETs if Bypass mode is used. When Bypass is enabled via SMBus, the output voltage of BYPSG is V_{BYPSRC}+5V. Leave this pin floating if Bypass mode function is not used.
17	DCIN	Power supply input of an internal 5V LDO. Bypass this pin to ground with an MLCC capacitor. Connect this pin with diode OR to V_{SYS} and adapter output.
18	VDD	Internal 5V LDO output. This pin provides the power for the usage of internal circuitry. Bypass this pin to ground with a 10μF.
19	PROG	An input pin for programming some settings, for more details please refer to "PROG Pin Programming Option" table.
20	OTGEN/ CMIN	A multiple function pin. This pin is configured between OTG mode enable input and comparator input pin via SMbus registers.

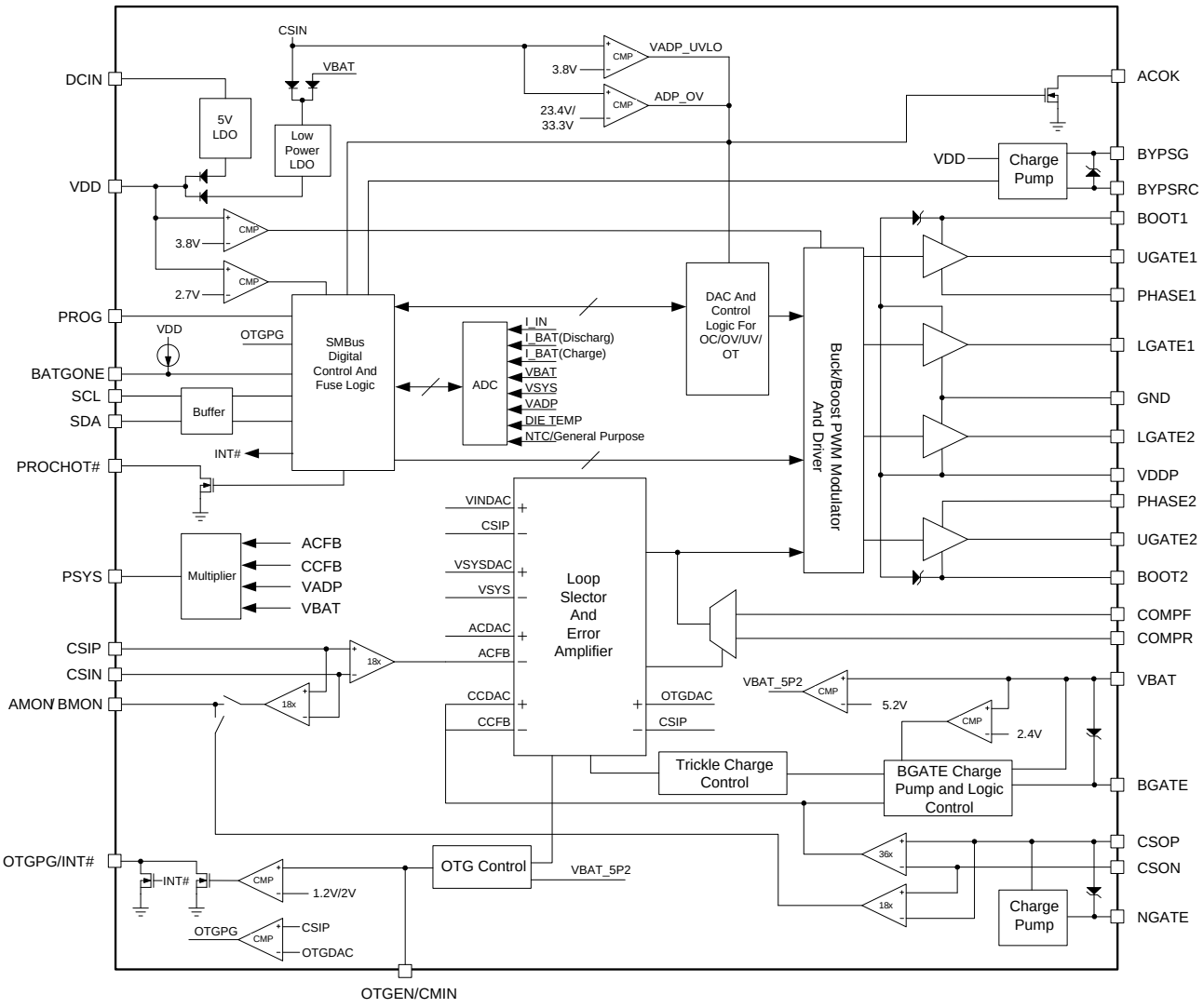
Reg0x3C[11]	Reg0x3D[3]	Pin 20
0	0	pin20 is selected as CMIN (default)
0	1	pin20 is selected neither CMIN nor OTGEN
1	0	pin20 is selected as CMIN
1	1	pin20 is selected as OTGEN

21	SDA	SMBus interface. Externally pull high to 1.8V or 3.3V with 10kΩ at each pin.
22	SCL	
23	PROCHOT#	An open drain output pin. The PROCHOT# is pulled low to ground in the conditions of ACHOT, DCHOT and Low_VSYS. This pin also is used as an indication of autonomous charging mode, pulled low in autonomous charging state. Pull this pin to 3.3V via a 10kΩ if it is used.
24	ACOK	An open drain output pin. The ACOK high output logic shows the adapter voltage is ok. Pull this pin to 3.3V via a 10kΩ if it is used.

Pin Descriptions (Cont.)

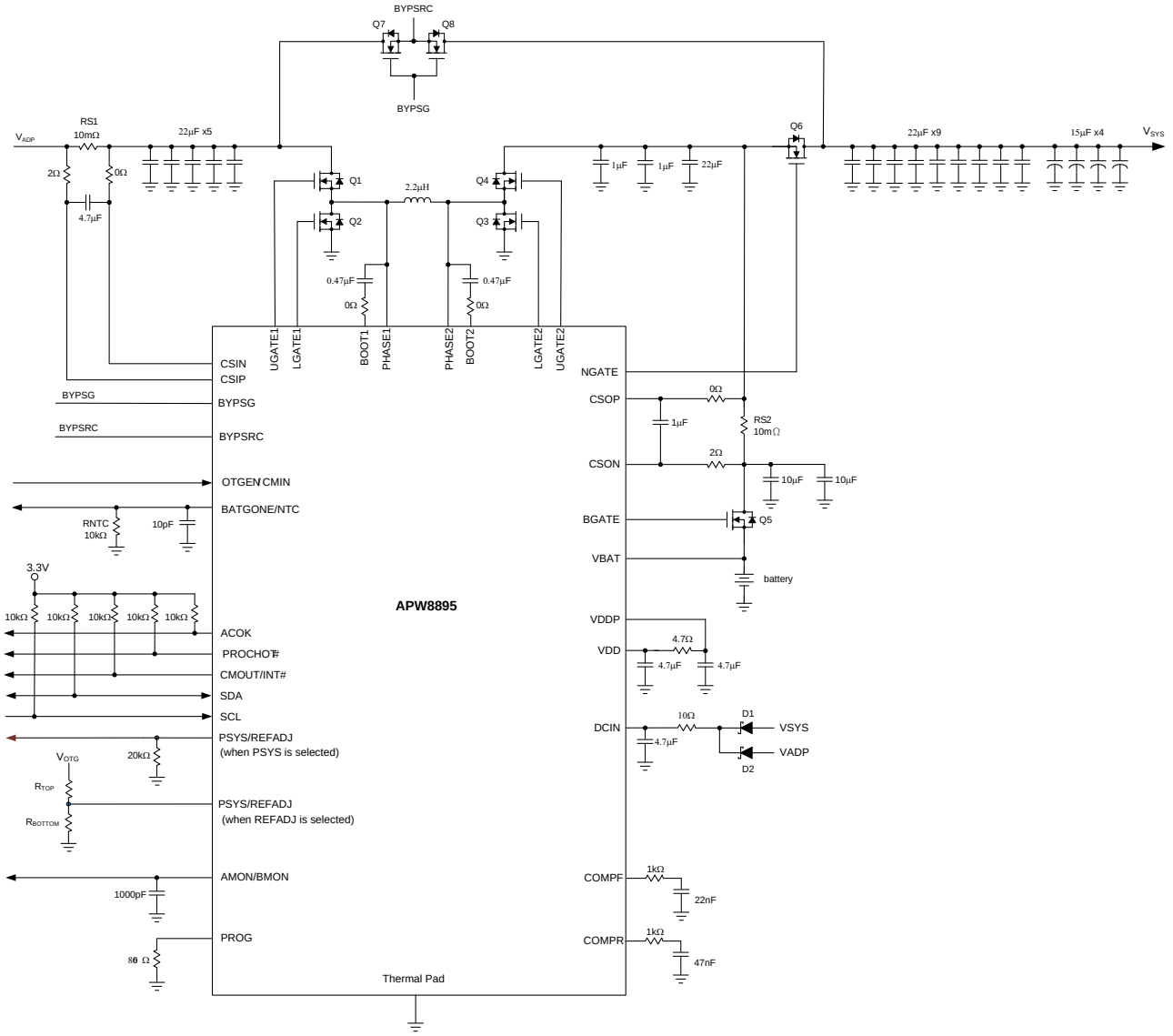
<table>
<tr><th colspan="2">PIN</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>NO.</th><th>NAME</th></tr>
<tr><td>25</td><td>BATGONE</td><td>An input pin for battery presence. Logic low to this pin indicates the battery is present while logic high indicates the battery has been removed.
The charger is allowed to enter charging mode or OTG mode only when the BATGONE is low.</td></tr>
<tr><td>26</td><td>CMOUT/
INT#</td><td>A multiple function pin.
This pin is configured between comparator output pin and interrupt output pin via SMbus registers.
<table>
<tr><th>Reg0x3D[3]</th><th>Pin 26</th></tr>
<tr><td>0</td><td>pin26 is selected as CMOUT (default)</td></tr>
<tr><td>1</td><td>pin26 is selected as INT#</td></tr>
</table></td></tr>
<tr><td>27</td><td>COMPR</td><td>The error amplifier output pin for reverse/OTG mode.
Connect an R in series with a C to ground for loop stability compensation.</td></tr>
<tr><td>28</td><td>COMPF</td><td>The error amplifier output pin for forward/charging mode.
Connect an R in series with a C to ground for loop stability compensation.</td></tr>
<tr><td>29</td><td>AMON/
BMON</td><td>The current monitor pin for Adapter side (AMON) or battery side(BMON).
The monitor path is selected via Reg0x3C[4], and the current direction is selected via Reg0x4C[3].
The 4 possible AMON/BMOB usages are listed as below table.
<table>
<tr><th>Reg0x3C[4]</th><th>Reg0x4C[3]</th><th>AMON/BMON Usage</th><th>AMON/BMON Output Voltage</th></tr>
<tr><td>0</td><td>0</td><td>AMON, adapter output current monitor (default)</td><td>17.97*(V_{CSIP}-V_{CSIN})</td></tr>
<tr><td>0</td><td>1</td><td>AMON, OTG mode output current monitor</td><td>17.9*(V_{CSIN}-V_{CSIP})</td></tr>
<tr><td>1</td><td>0</td><td>BMON, battery charging current monitor</td><td>35.78*(V_{CSOP}-V_{CSON})</td></tr>
<tr><td>1</td><td>1</td><td>BMON, battery discharging current monitor</td><td>17.97*(V_{CSON}-V_{CSOP})</td></tr>
</table></td></tr>
<tr><td>30</td><td>PSYS/REFADJ</td><td>A multi-function pin whose functionality is determined by the PROG readout.
As a PSYS pin, this pin outputs a current source in proportion to the whole system power consumption.
As an REFADJ, it is used as the OTG output voltage feedback pin.</td></tr>
<tr><td>31</td><td>VBAT</td><td>Battery voltage sense pin. Bypass this pin to ground with a 1μF MLCC capacitor.</td></tr>
<tr><td>32</td><td>BGATE</td><td>The gate driver output pin for the external battery P-MOSFET. This pin is low to turn on the power P-MOSFET between V_{SYS} and battery during fast charging mode or operates in a linear way to regulates the trickle charging current.</td></tr>
<tr><td>Thermal Pad</td><td>GND</td><td>Ground. Connect this thermal pad to a large copper area of ground plane for heat dissipation.</td></tr>
</table>

Block Diagram



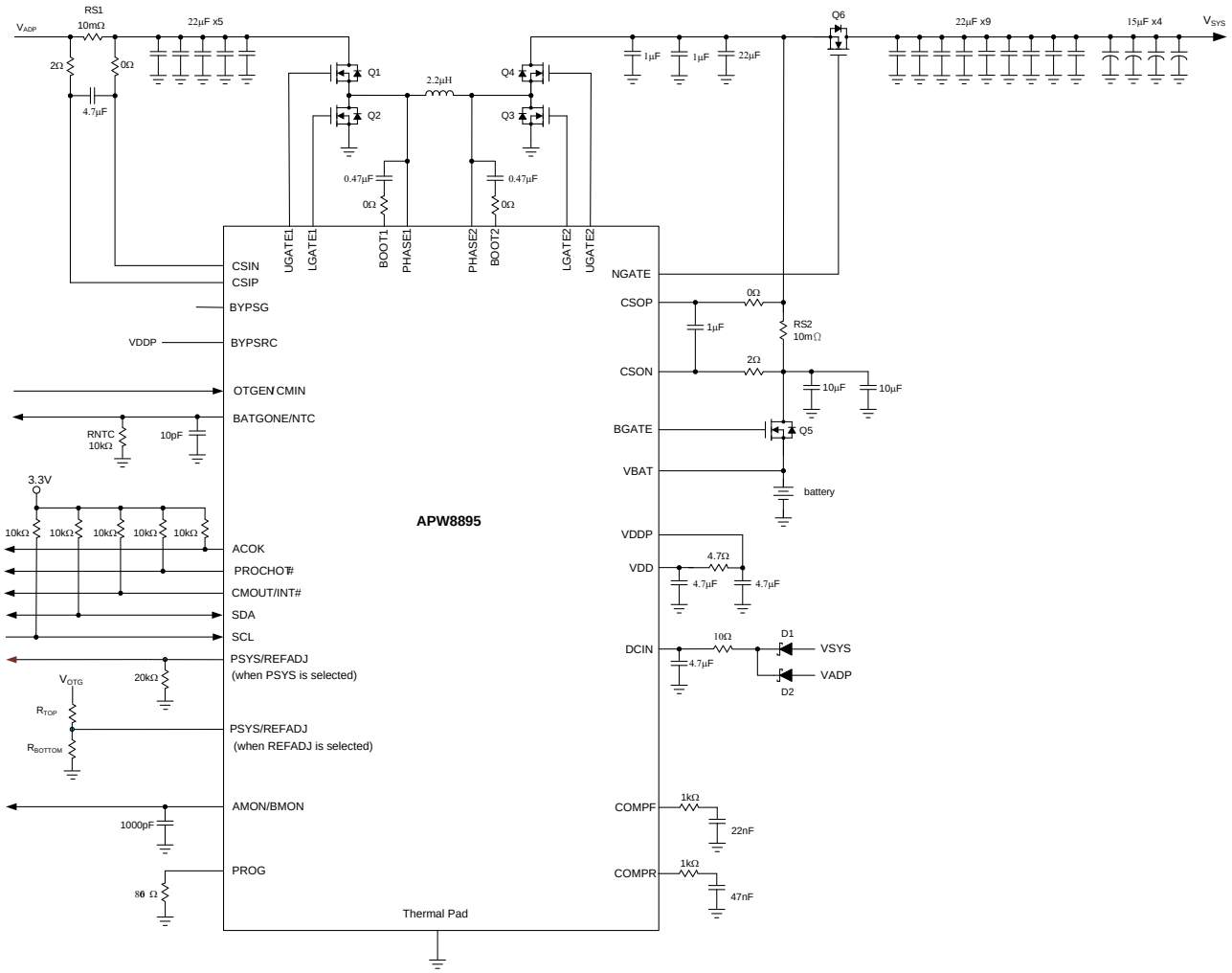
Typical Application Circuit

NVDC with Bypass mode



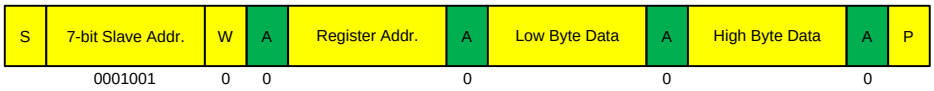
Typical Application Circuit (Cont.)

NVDC only

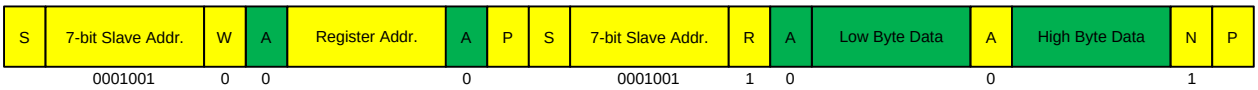


I²C/SMBus Programming

APW8895 has an I2C/SMbus interface. The APW8895 acts as a slave device. The host can access the APW8895 internal registers for configuration or investigation via I2C bus. The internal registers are 16-bit, so the APW8895 supports one word (16 bit) read and write protocols. The I2C/SMBus slave address is a hard-coded 7 bit address 0001001. The read and write protocols are as follows.



The Write Protocol of I2C interface writing to the APW8895



The Read Protocol of I2C interface Reading from the APW8895

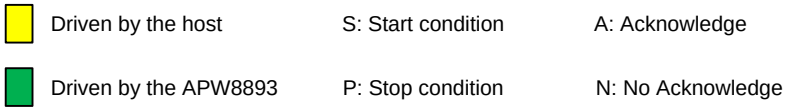


Figure 1: The I2C/SMBus Read and Write Protocols

The APW8895 Registers Summary

Register Address	Register Name	Read/ Write	Description	Default
0x14	ChargeCurrentLimit	R/W	Charge current limit DAC, 4mA/step, maximum 6.14A at R_{S2}=10mΩ	0x0000
0x15	MaxSystemVoltage	R/W	Maximum system voltage DAC, 8mV/step, maximum 18.304V, default value is set by PROG pin	0x20C0 (2-cell) 0x3120 (3-cell) 0x4180 (4-cell)
0x38	Control7	R/W	2-level adapter current limit duration, EOC, Supplemental mode period, Buck-boost stretch CCM period	0x0000
0x39	Control0	R/W	various charger options	0x0000
0x3A	Information1	R	various charger status	0x0000
0x3B	AdapterCurrentLimit2	R/W	Adapter current limit level-2 DAC, 4mA/step, maximum 6.14A at R_{S1}= 20mΩ	0x05DC
0x3C	Control1	R/W	various charger options	set by PROG pin
0x3D	Control2	R/W	various charger options	0x0000
0x3E	MinSystemVoltage	R/W	Minimum system voltage DAC, 64mV/step, 16.32V maximum	0x0000 (0V)
0x3F	AdapterCurrentLimit1	R/W	Adapter current limit level-1 DAC, 4mA/step, 6.14A maximum at R_{S1}=20mΩ	set by PROG pin
0x40	ACOK Reference	R/W	ACOK Reference DAC, 0V(disabled), 96mV~24.48V	0x0000
0x43	Control6	R/W	Interrupt trigger level direction	01FFF
0x47	ACProchot#	R/W	Adapter current Prochot# threshold DAC, 128mA//step, 6.4A maximum at R_{S1}=20mΩ	0x0C00
0x48	DCProchot#	R/W	Battery discharge current Prochot# threshold DAC, 256mA//step, maximum 12.8A at R_{S2}=10mΩ	0x1000
0x49	OTG Voltage	R/W	OTG mode voltage DAC, 12mV/step, 23.4V maximum	0x0D08
0x4A	OTG Current	R/W	OTG mode current limit threshold DAC, 32mA/step, 6.112A maximum	0x0200
0x4B	V_{IN} Voltage	R/W	V_{IN} loop regulation voltage DAC, 85mV/step, 16.384V maximum	0x0C00
0x4C	Control3	R/W	various charger options	0x0000
0x4D	Information2	R	various charger status	0x0000
0x4E	Control4	R/W	various charger options	0x0000
0x4F	Control5	R/W	Interrupt mask control	0x0000
0x80	NTC ADC Results	R	ADC result for NTC/General Purpose measurement	0x0000
0x81	VBAT ADC Results	R	ADC result for V_{VBAT} measurement, LSB=64mV	0x0000
0x82	TJ ADC Results	R	ADC result for internal junction temperature measurement, LSB=8mV	0x0000
0x83	IADP ADC Results	R	ADC result for adapter current measurement, LSB=22.2mV	0x0000
0x84	DC ADC Results	R	ADC result for battery discharge measurement, LSB=44.4mV	0x0000
0x85	CC ADC Results	R	ADC result for battery charge current measurement, LSB=22.2mV	0x0000
0x86	VSYS ADC Results	R	ADC result for V_{SYS} (CSOP) measurement, LSB=96mV	0x0000
0x87	VIN ADC Results	R	ADC result for V_{IN} (CSIN) measurement, LSB=96mV	0x0000
0x90	Information3	R	Interrupt status, masked/un-masked by Reg0x4F	0x0000
0x91	Information4	R	Interrupt real-time status	0x0000
0xFE	Manufacturer ID	R	Manufacturer ID	TBD
0xFF	Device ID	R	Device ID	TBD

Charge Current Limit Register 0x14

Bit	Bit Name	Read/Write	Bit Definition	
15:13	Not used	R		
12:2	ChargeCurrentLimit[10:0]	R/W	Charge current limit setting (4mA/step): (4mA/step, Sense Resistor=**10mΩ**) 00000000000: 0mA (default) 00000000001: 4mA 00000000010: 8mA 00000000011: 12mA 00000000100: 16mA . . 10111110000: 6080mA (maximum value) Value above 10111110001 will be clamped at 10111110000	Charge current limit setting (8mA/step): (8mA/step, Sense Resistor=**5mΩ**) 00000000000: 0mA (default) 00000000001: 8mA 00000000010: 16mA 00000000011: 24mA 00000000100: 32mA . . 10111110000: 12160mA (maximum value) Value above 10111110001 will be clamped at 10111110000
1:0	Not used	R		

Max System Voltage Register 0x15

Bit	Bit Name	Read/Write	Read/Write
15	Not used	R	
14:3	MaxSystemVoltage[11:0]	R/W	Maximum system voltage setting (12 bits, 8mV/step): 000000000000: 0mV 000000000001: 8mV 000000000010: 16mV 000000000011: 24mV 000000000100: 32mV . . 010000011000: 8384mV (default for 2-cell) . . 011000100100: 12576mV (default for 3-cell) . . 100000110000: 16.768mV (default for 4-cell) . . 100011110000: 18304mV (maximum value) Value above 10001111001 will be clamped at 100011110000
2:0	Not used	R	

Control7 Register 0x38

Bit	Bit Name	Read/ Write	Bit Definition
15:13	T2[2:0]	R/W	AdapterCurrentLimit2 duration setting (for Two Level ACLIM function): 000: 10μs (default) 001: 100μs 010: 500μs: 011: 1ms 100: 300μs 101: 750μs 110: 2ms 111: 10ms
12:10	T1[2:0]	R/W	AdapterCurrentLimit1 duration setting (for Two Level ACLIM function): 000: 10ms (default) 001: 20ms 010: 15ms: 011: 5ms 100: 1ms 101: 0.5ms 110: 1.0ms 111: 0ms
9:8	End of Charge (EOC) Current	R/W	End of charge current settings when Autonomous charging mode is enabled: 00: 105mA (default) 01: 55mA 10: 190mA 11: 145mA
7	Analog OV Control		Analog overvoltage enable/disable control: 0: Normal, OV pulls down on comp and disables switching (default) 1: Disable
6	GM_SUPN	R/W	Supplemental mode loop gain setting: 0: 1x (default) 1: 2x
5	T_SUP Multiplier (T_SUPM)	R/W	Supplemental mode period(T_SUPM) multiplier setting: 0: 1x (default) 1: 0.5x
4:2	T_SUP	R/W	Supplemental Buck mode period (T_SUP) setting: 000: Standard T_SUP (default) 001: 7/6 * Standard T_SUP 010: 8/6 * Standard T_SUP 011: 9/6 * Standard T_SUP 100: 10/6 * Standard T_SUP 101: 11/6 * Standard T_SUP 110: 12/6 * Standard T_SUP 111: 13/6* Standard T_SUP
1:0	Buck-Boost Stretch CCM Period	R/W	Buck-boost stretch CCM period (T2 TIME) setting: 00: 2x (default) 01: 3x 10: 1x 11: 0.6x

Control0 Register 0x39

Bit	Bit Name	Read/ Write	Bit Definition
15	CSIN Discharge	R/W	CSIN Discharge enable/disable control: 0: Disable, 10mA sink turned off (default) 1: Enable, 10mA sink turned on
14	CSIN Auto Discharge	R/W	CSIN auto discharge for 50ms enable/disable control when entering the ready state: 0: Disable (default) 1: Enable
13	CSOP Discharge	R/W	CSOP Discharge enable/disable control: 0: Disable, 10mA sink turned off (default) 1: Enable, 10mA sink turned on
12	NGATE Off	R/W	NGATE enable/disable control: 0: NGATE on (NGATE=CSOP + 5V); (default) 1: NGATE off (NGATE=CSOP)
11	BYPASS On	R/W	BYPSG enable/disable control: 0: BYPSG off (BYPSG=BYPSRC) (default) 1: BYPSG on (BYPSG=BYPSRC + 5V)
10	BGATE Force On	R/W	BGATE force on control: 0: BGATE normal operation (default) 1: BGATE forced on (BGATE=VBAT + 5V)
9:8	Dither Enable	R/W	PWM switching frequency dithering control: 00: Disable dither (default) 01: Dither1x 10: Dither2x 11: Dither3x
7	SMBus Timeout	R/W	SMBus Timert enable/disable control: 0: Enable the SMBus timeout function (default) 1: Disable the SMBus timeout function The SMbus Timeout timer is 175 seconds. When SMBus timeout function is enabled, the host must send a write command to the MaxchargeVoltage or ChargeCurrentLimit within 175 seconds to prevent timeout occurrence. If a timeout occurs, the charging will be terminated. Writing MaxchargeVoltage or ChargeCurrentLimit register will re-start charging and the 175s timer will re-start too.
6	Enable Charge Pumps to 100% duty cycle	R/W	BGATE and NGATE charge pump 100% duty enable/disable control: 0: Normal operation (reduced supply current) (default) 1: Enable charge pumps 100% of the time to ensure the charge pump good bit does not toggle due to gate leakage
5	BYP VIN<VOUT Comparator to turn off BYPSG	R/W	Bypass comparator enable/disable control: 0: Disable (default) 1: Enable When VIN/VOUT comparator is enabled, BYPSG is controlled by the comparator in this way: ●VCSIN falls to and below VCSOP+400mV, BYPSG turns off. ●VCSIN rises to and above VCSOP+800mV, BYPSG turns on.
4:3	DCProchot# Threshold in Battery Only Low Power Mode[1:0]	R/W	In battery only mode, the IC enters low power mode when PSYS function is not enabled. When the battery discharge current exceeds this threshold the PROCHOT# will be asserted. 00: 12A (default) 01: 10A 10: 8A 11: 6A (R_{S2}=10mΩ)
2	Input Voltage Regulation Loop	R/W	Input Voltage Regulation Loop Enable/Disable Control: 0: Enable (default) 1: Disable (Input Voltage Regulation Voltage is set by Reg0x4B)
1	VSYS Regulation Offset Voltage Adder	R/W	Adds offset above the VSYSMAX register setting when not charging. 0 = 0mV (default) 1 = 384mV (384mV is always added to MinsysVoltage in Trickle Charge mode - irrespective of this bit) (When the device is not charging but is in the VSYS state and Regx039[1]=0, the system voltage is regulated to the same setting as the DAC. When Regx039[1]=1, then system voltage is regulated to the DAC plus an offset of 384mV, which is useful to avoid discharging a full battery in VSYS state when there is a system load transient.
0	Not used	R	

Information1 Register 0x3A

Bit	Bit Name	Read/Write	Bit Definition
15	Low Power Mode	R	The indication of low power mode: 0: The IC is in low power mode 1: The IC is not in low power mode
14:13	Active Control Loop[1:0]	R	The indication of internal active control loop: 00: MaxSystemVoltage control loop is active 01: Charging current loop is active 10: Adapter current limit loop is active 11: Input voltage regulation loop is active
12	ACProchot#	R	The indication to show if ACProchot#/OTGCURRENTProchot# is tripped or not: 0: Normal 1: ACProchot#/OTGCURRENTProchot# has been tripped (ACProchot# threshold is set by Reg0x47[12:7])
11	DCProchot#	R	The indication to show if DCProchot# is tripped or not: 0: Normal 1: DCProchot# has been tripped (DCProchot# threshold is set by Reg0x48[13:8] or Reg0x39[4:3])
10	Low VSYS Prochot#	R	The indication to show if Low VSYS Prochot# is tripped or not: 0: Normal 1: Low VSYS Prochot# has been tripped (Low VSYS Prochot# threshold is set by Reg0x3C[1:0])
9:7	Not used	R	
6	BGATE Power Good Status	R	The indication of BGATE charge pump power good: 0: BGATE charge pump is not good. 1: BGATE charge pump is not good.
5	CSIN CSOP Comparator Status	R	The indication of CSIN to CSOP comparator result: 0: $V_{CSIN} < V_{CSOP}$ 1: $V_{CSIN} > V_{CSOP}$
4	Trickle Charge	R	The indication to show if trickle charge mode is active or not: 0: Trickle charge mode is not active 1: Trickle charge mode is active
3	NGATE Power Good Status	R	The indication of NGATE charge pump power good: 0: NGATE charge pump is not good. 1: NGATE charge pump is not good.
2	BYPSG Power Good Status	R	The indication of BYPSG charge pump power good: 0: BYPSG charge pump is not good. 1: BYPSG charge pump is not good.
1	Reverse Turbo Mode Status	R	The indication to show if Reverse Turbo Mode is active or not: 0: Reverse Turbo Mode is not active 1: Reverse Turbo Mode is active
0	Ideal Diode Mode Status	R	The indication to show if Ideal Diode Mode is active or not: 0: Ideal Diode Mode is not active 1: Ideal Diode Mode is active

Adapter Current Limit2 Register 0x3B

Bit	Bit Name	Read/Write	Bit Definition	
15:13	Not used	R		
12:2	AdapterCurrentLimit2 [10:0]	R/W	Adapter current limit level 2 setting (4mA/step): (4mA/step, Sense Resistor=**20mΩ**) 00000000000: 0mA 00000000001: 4mA 00000000010: 8mA 00000000011: 12mA 00000000100: 16mA . . 00101110111: 1500mA (default) . . 10111111111: 6140mA (maximum value) Value above 11000000000 will be clamped at 10111111111	Adapter current limit level 2 setting (8mA/step): (8mA/step, Sense Resistor=**10mΩ**) 00000000000: 0mA 00000000001: 8mA 00000000010: 16mA 00000000011: 24mA 00000000100: 32mA . . 00101110111: 3000mA (default) . . 10111111111: 12280mA (maximum value) Value above 11000000000 will be clamped at 10111111111
1:0	Not used	R		

Control1 Register 0x3C

Bit	Bit Name	Read/Write	Bit Definition
15:14	General Purpose Comparator Assertion Debounce Time[1:0]	R/W	General Purpose Comparator Assertion Debounce Time: 00: 2μs (default) 01: 12μs 10: 2ms 11: 720μs
13	Exit Learn Mode Option	R/W	The options to exit Learn mode when battery voltage is lower than MinSystemVoltage: 0: Stay in Learn mode even if V_{BAT} < MinSystemVoltage register setting (default) 1: Exit Learn mode if V_{BAT} < MinSystemVoltage register setting
12	Learn Mode	R/W	Battery Learn mode enable/disable control: 0: Disable (default) 1: Enable
11	OTG Function	R/W	OTG function enable/disable control: 0: Disable (default) 1: Enable
10	Supplemental Support Mode	R/W	Supplemental Support Mode (Intel V_{MIN} Active Protection) enable/disable control: 0: Disable (default) 1: Enable
9:7	Switching Frequency[2:0]	R/W	PWM switching frequency setting: 000: 1420kHz 001: 1180kHz 010: 1020kHz 011: 890kHz 100: 808kHz 101: 724kHz 110: 656kHz 111: 600kHz To keep the switching frequency set by the PROG pin resistor, leave Bit[9:7] as it is read.
6	'BGATE Force Off	R/W	Disables BGATE. This forces the BGATE FET to turn off and overwrite Turbo mode. 0 = Normal operation (default) 1 = Force BGATE Off (BGATE = VBAT) (also disables Turbo mode/Ideal Diode mode)
5	AMON/BMON Function	R/W	AMON/BMON function enable/disable control: 0: Enable (default) 1: Disable This bit is only valid in battery only mode. When adapter is present, this bit becomes invalid.
4	AMON or BMON	R/W	The selection of output signal of AMON/BMON pin when AMON/BMON function is enabled. 0: AMON (default) 1: BMON
3	PSYS	R/W	PSYS function enable/disable control: 0: Disable (default) 1: Enable
2:0	Low VSYS Prochot# Threshold[2:0]	R/W	The Low_VSYS_Prochot# assertion and supplemental support mode activation threshold setting: 000: 5.4V 001: 5.6V 010: 5.8V 011: 6.0V (default) 100: 6.2V 101: 6.4V 110: 6.6V 111: 6.8V

Control2 Register 0x3D

Bit	Bit Name	Read/Write	Bit Definition
15:13	Trickle Charging Current[2:0]	R/W	Trickle Charging Current Setting: 000: do not use 001: 64mA 010: 96mA 011: 128mA (default) 100: 160mA 101: 192mA 110: 224mA 111: 256mA
12	Two-level Adapter Current Limit Function	R/W	Two-level Adapter Current Limit function enable/disable control: 0: Disable (default) 1: Enable
11	Fault Timer Debounce Time for OT and WOCP	R/W	The debounce time for over temperature and WOCP events: 0: 1.3s (default) 1: 150ms
10:9	PROCHOT# Debounce[1:0]	R/W	The Prochot# assertion debounce time for ACProchot# and DCProchot#: 00: 7μs (default) 01: 100μs 10: 500μs 11: 1ms The Low_VSYS_Prochot# assertion debounce time is fixed at 7μs.
8:6	PROCHOT# Duration[2:0]	R/W	The minimum duration of the Prochot# signal after assertion: 000: 10ms (default) 001: 20ms 010: 15ms 011: 5ms 100: 1ms 101: 500μs 110: 100μs 111: 0s
5	JEITA Control Bit[1]	R/W	JEITA Control Bit[1](=Reg3D[5]) + JEITA Control Bit[0](=Reg4E[14])=JEITA Control[1:0]: 00 - General purpose ADC input, NTC current source OFF (default) 01 - Original JEITA profiles, NTC current source ON 10 - Profile 1, NTC current source ON 11 - Profile 2, NTC current source ON
4	CMIN Reference	R/W	The option of reference voltage of internal general purpose comparator: 0: 1.2V (default) 1: 2V (this option is not available in Battery Only mode)
3	General Purpose Comparator	R/W	The general purpose comparator function enable/disable control: 0: Enable (default) 1: Disable
2	CMOUT Polarity	R/W	The option of the general purpose comparator output polarity: 0: CMOUT is high when CMIN is higher than reference (default) 1: CMOUT is low when CMIN is higher than reference
1	Internal Resistor Compensation for COMPR RCOMP	R/W	Changes the internal compensation resistor to speed up or slow down the loop response for reverse modulator operations (OTG). 0: Faster (default) 1: Slower
0	Internal Resistor Compensation for COMPF RCOMP	R/W	Changes the internal compensation resistor to speed up or slow down the loop response for forward modulator operations and Reverse Turbo Boost mode. 0: Faster (default) 1: Slower

Min System Voltage Register 0x3E

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:6	MinSystemVoltage[7:0]	R/W	Minimum system voltage setting (64mV/step): 00000000: 0mV (default) 00000001: 64mV 00000010: 128mV 00000011: 192mV 00000100: 256mV .. 11111111: 16320mV (maximum value)
5:0	Not used	R	

Adapter Current Limit1 Register 0x3F

Bit	Bit Name	Read/Write	Bit Definition	
15:13	Not used	R		
12:2	AdapterCurrentLimit1[10:0]	R/W	Adapter current limit level 1 setting (4mA/step): (4mA/step, Sense Resistor=**20mΩ**) 00000000000: 0mA 00000000001: 4mA 00000000010: 8mA 00000000011: 12mA 00000000100: 16mA . . 10111111111: 6140mA Value above 11000000000 will be clamped at 10111111111	Adapter current limit level 1 setting (8mA/step): (8mA/step, Sense Resistor=**10mΩ**) 00000000000: 0mA 00000000001: 8mA 00000000010: 16mA 00000000011: 24mA 00000000100: 32mA . . 10111111111: 12280mA Value above 11000000000 will be clamped at 10111111111
1:0	Not used	R		

ACOKREF Register 0x40

Bit	Bit Name	Read/Write	Bit Definition
15:12	Not used	R	
13:6	ACOKREF[7:0]	R/W	ACOK reference for V_{IN} (CSIN) comparison, LSB=96mV, programming range=0~24.48V, 00000000: disabled (default) 00000001: 96mV 00000010:192mV 00000011: 288mV 00000100: 384mV . . 11111111: 24480mV
5:0	Not used	R	

Control6 Register 0x43

Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12	SMBus timeout timer expired	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
11	12-hour charge timer expired for Autonomous Charging mode only	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
10	SYS OV	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
9	ADP OV	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
8	ADP VMIN	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
7	ADP current	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
6	Thermal warning	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
5	OTGPG	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
4	Battery charging terminated for Autonomous Charging mode	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
3	Battery charging CC to CV	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
2	FET fault state	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
1	Enter READY	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)
0	Changed NTC temperature boundary	R/W	Interrupt trigger level selection: 0 = Event triggers when low 1 = Event triggers when high (default)

ACProchot# Register 0x47

Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12:7	ACProchot#[5:0]	R/W	ACProchot# threshold setting (128mA/step): 000000: 0mA 000001: 128mA 000010: 256mA 000011: 384mA 000100: 512mA . . 011000: 3072mA (default) . . 110010: 6400mA (maximum value) Value above 110011 will be clamped at 110010
6:0	Not used	R	

DCProchot# Register 0x48

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:8	DCProchot#[5:0]	R/W	DCProchot# threshold setting (256mA/step): 000000: 0mA 000001: 256mA 000010: 512mA 000011: 768mA 000100: 1024mA . . 010000: 4096mA (default) . . 110010: 12800mA (maximum value) Value above 110011 will be clamped at 110010
7:0	Not used	R	

OTG Voltage Register 0x49

Bit	Bit Name	Read/Write	Bit Definition
15	Not used	R	
14:3	OTGVOLTAGE[110]	R/W	OTG mode output voltage setting (12mV/step): 000000000000: 0mV 000000000001: 12mV 000000000010: 24mV 000000000011: 36mV 000000000100: 48mV . . 000110100001: 5004mV (default) . . 100011110000: 27456mV (maximum value) Value above 100011110001 will be clamped at 100011110000
2:0	Not used	R	

OTG Current Register 0x4A

Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12:5	OTGCURRENT[7:0]	R/W	OTG current limit threshold setting (32mA/step): 00000000: 0mA 00000001: 32mA 00000010: 64mA 00000011: 96mA 00000100: 128mA . . 00010000: 512mA (default) . . 10111111: 6112mA (maximum value) Value above 11000000 will be clamped at 10111111
4:0	Not used	R	

VIN Voltage Register 0x4B

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:6	INPUT VOLTAGE[7:0]	R/W	Input voltage regulation threshold setting (85mV/step): 00000000: 0mV 00000001: 85mV 00000010: 171mV 00000011: 256mV 00000100: 341mV . 00001000: 683mV . 00010000: 1365mV . 00100000: 2731mV . 00110000: 4096mV (default) . 01000000: 5461mV . 10000000: 10923mV . . 11000000: 16384mV (maximum value) Value above 11000001 will be clamped at 11000000
5:0	Not used	R	

Control3 Register 0x4C

Bit	Bit Name	Read/Write	Bit Definition
15	Digital OV Control and OTG UV Control	R/W	0: Normal digital overvoltage, shuts down switching after debounce time (default) 1: Disables the undervoltage for OTG and overvoltage digital for OTG and VSYS for Programmable Power Supply operations
14	Reload ACLIM	R/W	This bit sets if re-load AdapterCurrentLimit1 register set by PROG pin resistor on the falling edge of ACOK: 0: Re-load 1: Do not re-load
13	Autonomous Charging Termination Time	R/W	The option of autonomous charging termination time: 0: 20ms (default) 1: 200ms
12:11	Charger Timeout[1:0]	R/W	The option of SMBus charger timeout time: 00: 175s (default) 01: 87.5s 10: 43.75s 11: 4.95s
10	DCM/CCM Hysteresis	R/W	Sets the hysteresis of DCM to CCM boundary: 0 = Hysteresis enabled for the DCM to CCM boundary (default) 1 = Hysteresis disabled
9:8	PSYS Gain[1:0]	R/W	The option of system power monitor PSYS output gain: (When Reg0x4E[11]=0b to select R_{S1}:R_{S2}=2:1) 00: 0.896μA/W (I_{PSYS}=System Power*PSYS Gain+1.352μA) 01: 1.315μA/W (I_{PSYS}=System Power*PSYS Gain+2.047μA) 10: 0.431μA/W (I_{PSYS}=System Power*PSYS Gain+0.626μA) 11: 0.646μA/W (I_{PSYS}=System Power*PSYS Gain+0.959μA) (default) (When Reg0x4E[11]=1b to select R_{S1}:R_{S2}=1:1) 00: 0.907μA/W (I_{PSYS}=System Power*PSYS Gain+1.773μA) 01: 1.337μA/W (I_{PSYS}=System Power*PSYS Gain+2.654μA) 10: 0.434μA/W (I_{PSYS}=System Power*PSYS Gain+0.831μA) 11: 0.653μA/W (I_{PSYS}=System Power*PSYS Gain+1.265μA) (default)
7	Autonomous Charging Mode	R/W	The Autonomous Charging mode enable/disable control: 0: Disable (instead, IC will enter SMBus controlled charging mode; charging is configured/controlled by host via SMBus) 1: Enable
6	AC and CC Feedback Gain	R/W	The option of AC and CC feedback gain for high current: 0: x1 (default) 1: x0.5
5	Input Current Limit Loop	R/W	The input current limit loop enable/disable control: 0: Enable (default) 1: Disable
4	Input Current Limit Loop When BATGONE=1	R/W	The input current limit loop when BATGONE=1 enable/disable control: 0: Enable (default) 1: Disable
3	AMON/BMON Direction	R/W	The AMON/BMON current monitor direction control: 0: Adapter current monitor/battery charging current monitor (default) 1: OTG output current monitor/battery discharging current monitor
2	Digital Reset	R/W	To reset all SMBus registers' value to default values, including re-reading PROG settings: 0: Idle (default) 1: Reset
1	T2DCM	R/W	Buck-Boost T2 time in DCM (T2DCM), reduces input ripple. 0 = Reduced T2 time (increases switching frequency in DCM) (default) 1 = Normal T2 time
0	Enable ADC	R/W	ADC function enable/disable control: 0 = ADC is enabled only when battery charging. (default) 1 = ADC is enabled for all modes.

Information2 Register 0x4D

Bit	Bit Name	Read/Write	Bit Definition
15	Not used	R	
14	ACOK	R	ACOK output pin status: 0: ACOK pin is low; adapter is not present 1: ACOK pin is high; adapter is present
13	CMOUT	R	Comparator output pin (CMOUT) status: 0: CMOUT pin is low 1: CMOUT pin is high
12	BATGONE	R	BATGONE input pin status: 0: BATGONE pin is low; battery is present 1: BATGONE pin is high; no battery
11:8	Machine Status[3:0]	R	TBD
7:5	Buck Boost Mode[2:0]	R	Buck Boost charger operation mode indication: 001: Forward Boost mode 010: Forward Buck mode 011: Forward Buck-boost mode 101: OTG boost mode 110: OTG buck mode 111: OTG buck-boost mode
4:0	PROG Pin Read Out[4:0]	R	PROG pin resistor read out

Control4 Register 0x4E

Bit	Bit Name	Read/Write	
15	BATGONE Disable	R/W	BATGONE pin input disable: 0: Normal BATGONE input (default) 1: Ignore BATGONE input
14	JEITA Control Bit[0]	R/W	JEITA Control Bit[1](=Reg3D[5]) + JEITA Control Bit[0](=Reg4E[14])=JEITA Control[1:0]: 00: General purpose ADC input, NTC current source OFF (default) 01: Original JEITA profiles, NTC current source ON 10: Profile 1, NTC current source ON 11: Profile 2, NTC current source ON
13	Slew Rate Control	R/W	VSYS and VOTG DAC Slew Rate Control: 0: Slew Rate Control Disabled (default) 1: Slew Rate enabled to ramp DAC voltage; OTG 12mV/μs and VSYS 8mV/μs;
12	Disable GP Comparator	R/W	GP comparator enable/disable setting in Battery Only mode: 0: Enabled for all modes (default) 1: Disabled for Battery Only mode (REF = 1.2V in Battery Only mode)
11	PSYS Rsense Ratio	R/W	RSENSE (R_{S1}:R_{S2}) ratio for PSYS. 0: 2:1 (default) 1: 1:1
10	Force Buck Mode	R/W	Forward PWM force buck and reverse PWM force boost control: 0: Normal modulator operations (default) 1: Forward Force Buck/Reverse Force Boost
9	WOCP Function	R/W	Way overcurrent function enable/disable setting: 0: Enable way overcurrent detection (default) 1: Disable
8	VSYS Short Check	R/W	Enables or disables VSYS short detection before enabling the modulator. 0: Enable (default) 1: Disable
7	OTGCURRENT PROCHOT#	R/W	OTGCURRENT event trigger PROCHOT# assertion enable/disable control: 0: Disable (default) 1: Enable
6	BATGONE PROCHOT#	R/W	BATGONE rising trigger PROCHOT# assertion enable/disable control: 0: Disable (default) 1: Enable
5	ACOK PROCHOT#	R/W	ACOK falling trigger PROCHOT# assertion enable/disable control: 0: Disable (default) 1: Enable
4	GP Comparator PROCHOT#	R/W	General Purpose Comparator output rising trigger PROCHOT# assertion enable/disable control: 0: Disable (default) 1: Enable
3:2	ACOK Falling or BATGONE Rising Debounce[1:0]	R/W	The option of the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip: 00: 2μs 01: 25μs 10: 125μs 11: 250μs
1	PROCHOT# Clear	R/W	To clear PROCHOT# assertion: 0: Idle 1: Clear PROCHOT# assertion
0	PROCHOT# Latch	R/W	The PROCHOT# assertion behavior option: 0: PROCHOT# becomes de-asserted when the trigger event disappears. 1: PROCHOT# keeps asserted and latched once tripped.

Control5 Register 0x4F

Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12	SMBus timeout timer expired	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
11	12-hour charge timer expired for Autonomous Charging mode only	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
10	SYS OV	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
9	ADP OV	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
8	ADP VMIN	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
7	ADP current	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
6	Thermal warning	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
5	OTGPG	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
4	Battery charging terminated for Autonomous Charging mode	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
3	Battery charging CC to CV	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
2	FET fault state	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
1	Enter READY	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked
0	Changed NTC temperature boundary	R/W	Interrupt mask control: 0 = Event mased (default) 1 = Event unmasked

NTC Voltage ADC Register 0x80

Bit	Bit Name	Read/Write	Bit Definition
15:10	Not used	R	
9:0	NTC Voltage[9:0]	R	NTC Voltage ADC result, 0~2.04V, LSB=1.992mV. NTC Voltage is sampled from BATGONE pin. If NTC function is not enabled (eq., Reg3D[5])=0b andReg4E[14]=0b) but ADC function is enabled, the BATGONE is a general purpose ADC input, APW8895 directly samples the voltage on BATGONE and stores the ADC result into NTC Voltage[9:2], LSB=7.969mV

VBAT Voltage ADC Register 0x81

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:6	VBAT Voltage[7:0]	R	Battery Voltage ADC result, 0~16.32V, LSB=63.57mV.
5:0	Not used	R	

TJ ADC Register 0x82

Bit	Bit Name	Read/Write	Bit Definition
15:8	Not used	R	
7:0	TJ[7:0]	R	Internal die temperature ADC result, 0~2.04V, LSB=7.969mV. TJ[7:0] (decimal)=251.7-0.6154*TJ

Adapter Current ADC Register 0x83

Bit	Bit Name	Read/Write	Bit Definition
15:8	Not used	R	
7:0	IADP[7:0]	R	Adapter current ADC result (R_{S1}=20mΩ), 0~5.68A, LSB=22.2mA.

Battery Discharge Current ADC Register 0x84

Bit	Bit Name	Read/Write	Bit Definition
15:8	Not used	R	
7:0	IBAT_DC[7:0]	R	Battery discharge current ADC result (R_{S2}=10mΩ), 0~11.37A, LSB=44.4mA.

Battery Charge Current ADC Register 0x85

Bit	Bit Name	Read/Write	Bit Definition
15:8	Not used	R	
7:0	IBAT_CC[7:0]	R	Battery discharge current ADC result (R_{S2}=10mΩ), 0~5.68A, LSB=22.2mA.

VSYS Voltage ADC Register 0x86

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:6	VSYS[7:0]	R	VSYS voltage (CSOP) ADC result 0~24.48, LSB=95.625mV.
5:0	Not used	R	

Adapter Voltage ADC Register 0x87

Bit	Bit Name	Read/Write	Bit Definition
15:14	Not used	R	
13:6	VADP[7:0]	R	Adapter voltage (CSIN) ADC result 0~24.48, LSB=95.625mV.
5:0	Not used	R	

Information3 Register 0x90

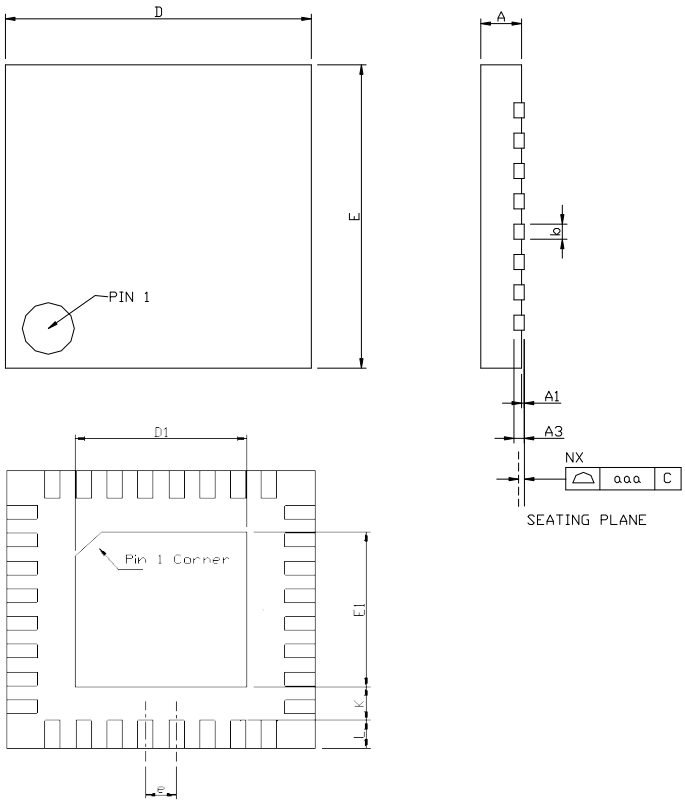
Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12	SMBus timeout timer expired	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
11	12-hour charge timer expired for Autonomous Charging mode only	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
10	SYS OV	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
9	ADP OV	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
8	ADP VMIN	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
7	ADP current	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
6	Thermal warning	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
5	OTGPG	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
4	Battery charging terminated for Autonomous Charging mode	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
3	Battery charging CC to CV	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
2	FET fault state	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
1	Enter READY	R/W	Event status if not masked: 0 = no event (default) 1 = event is set
0	Changed NTC temperature boundary	R/W	Event status if not masked: 0 = no event (default) 1 = event is set

Information4 Register 0x91

Bit	Bit Name	Read/Write	Bit Definition
15:13	Not used	R	
12	SMBus timeout timer expired	R/W	Event real time status: 0 = not in state (default) 1 = event is set
11	12-hour charge timer expired for Autonomous Charging mode only	R/W	Event real time status: 0 = not in state (default) 1 = event is set
10	SYS OV	R/W	Event real time status: 0 = not in state (default) 1 = event is set
9	ADP OV	R/W	Event real time status: 0 = not in state (default) 1 = event is set
8	ADP VMIN	R/W	Event real time status: 0 = not in state (default) 1 = event is set
7	ADP current	R/W	Event real time status: 0 = not in state (default) 1 = event is set
6	Thermal warning	R/W	Event real time status: 0 = not in state (default) 1 = event is set
5	OTGPG	R/W	Event real time status: 0 = not in state (default) 1 = event is set
4	Battery charging terminated for Autonomous Charging mode	R/W	Event real time status: 0 = not in state (default) 1 = event is set
3	Battery charging CC to CV	R/W	Event real time status: 0 = not in state (default) 1 = event is set
2	FET fault state	R/W	Event real time status: 0 = not in state (default) 1 = event is set
1	Enter READY	R/W	Event real time status: 0 = not in state (default) 1 = event is set
0	Changed NTC temperature boundary	R/W	Event real time status: 0 = not in state (default) 1 = event is set

Package Information

TQFN4x4-32B



SYMBOL	TQFN4x4-32B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	3.90	4.10	0.154	0.161
D1	2.50	2.80	0.098	0.110
E	3.90	4.10	0.154	0.161
E1	2.50	2.80	0.098	0.110
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

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