3W Stereo Class D Audio Power Amplifier and Class AB Headphone Driver (DC Volume Control, UVP, AGC)

Features

- **Operating Voltage: 3.1V-5.8V**
- **High Efficiency 85% at P_O=3W, 4Ω Speaker, V_{DD}=5V**
- **Filter-free Class D Amplifier**
- **Low Shutdown Current**
  - I_{DD}=1μA at VDD=5V
- **64 Steps Volume Adjustable from -80dB to +20dB by DC Voltage with Hysteresis**
- **AGC (Non-Clip) Function**
  - Disable : 0.45VDD~VDD, Floating
  - Max, Power : Internal set limit level
  AGC<0.27VDD
- **Under Voltage Protection Function**
  - Disable : Floating
- **Output Power at THD+N=1%**
  BTL mode
  - 2.55W at V_{DD}=5V, R_L=4Ω
  - 1.44W at V_{DD}=5V, R_L=8Ω
  SE mode
  - 75mW at V_{DD}=5V, R_L=32Ω
  Output Power at THD+N=10%
  - 3.14W at V_{DD}=5V, R_L=4Ω
  - 1.77W at V_{DD}=5V, R_L=8Ω
- **Less External Components Required**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/BTL pin**
- **Input signal and Headphone Output Signal in phase**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Power Enhanced Packages**
  QFN4x4-20A (APA2609)
  QFN3x3-20 (APA2609A)
- **Lead Free and Green Device Available(RoHS Compliant)**

Applications

- **LCD TVs**
- **DVD Player**
- **Active Speakers**

General Description

The APA2609 provides DC volume control, gain range is from +20dB (V_{VOLUME}=0V) to -80dB (V_{VOLUME}=5V) with gain range from. It's easy to get the suitable amplifier's gain with the 64 steps gain setting. The filter-free architecture eliminates the output filters compared to the traditional Class-D audio amplifier, and reduces the external component counts and the components height, it could save the PCB space, system cost, simplifies the design and the power loss at filter.

APA2609 provides an AGC (Non-Clip) function, which limits output swing from overstress speaker. It reduces internal gain instead of clipping peak to maintain low THD.

The APA2609 also integrates the de-pop circuitry that reduces the pops and click noises during power on/off or shutdown enable process.

The APA2609 has built-in over-current and thermal protection that prevent the chip being destroyed by short circuit or over temperature situation.

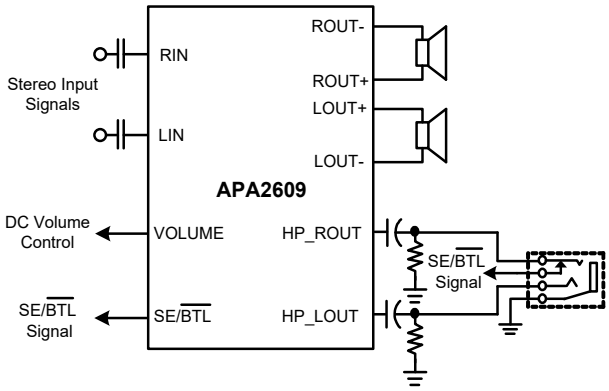
APA2609 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.

APA2609 is capable of driving 3W at 5V into 4Ω speaker. The efficiency can archived 85% at R_L=4Ω when P_O=3W at V_{DD}=5V.

APA2609 is capable of driving 75mW at 5V into 32Ω Headphone.

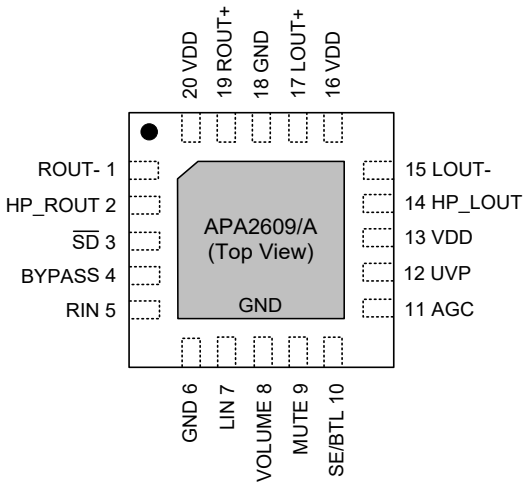
UVP function minimize power off induced pop noise.

Simplified Application Circuit



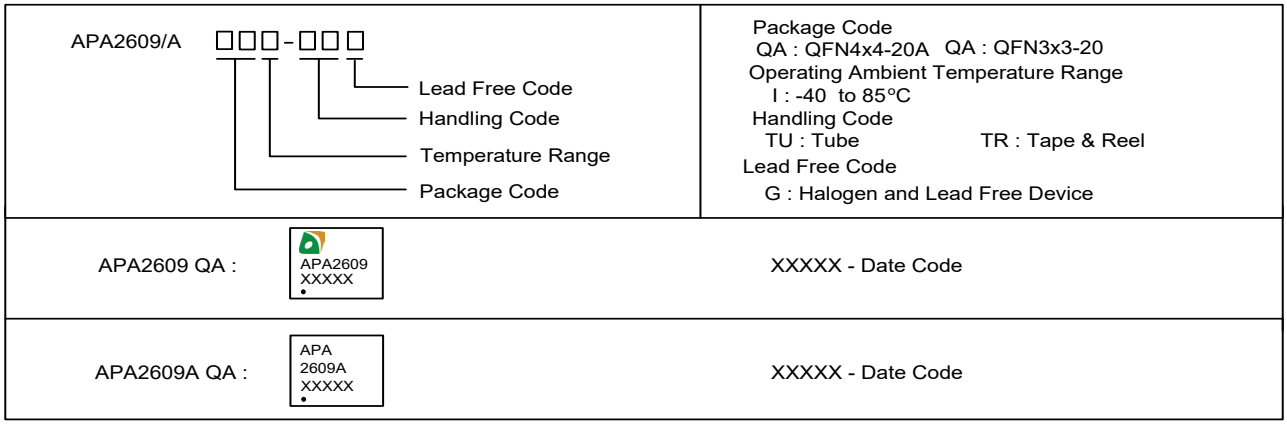
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configurations



QFN4x4-20A(APA2609)
QFN3x3-20(APA2609A)

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{DD}	Supply Voltage (VDD to GND)		-0.3 to 6	V
	Input Voltage (LIN, RIN to GND)		-0.3 to V_{DD}+0.3	
	Input Voltage ($\overline{SD}$, MUTE, AGC, UVP, VOLUME and SE/BTL, BYPASS to GND)		-0.3 to V_{DD}+0.3	
V_{OUTX}	Output Voltage (OUT_X to GND_XX)	<30ns pulse width	-2 to 8.2	V
		>30ns pulse width	-0.3 to V_{DD}+0.3	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to +150	
T_{SDR}	Soldering Temperature Range		260, 10 seconds	
P_D	Power Dissipation		Internally Limited	W

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Copyright©ANPEC Electronic Corp.

Thermal Characteristics (Note 2, 3)

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note 2) QFN3x3-20 QFN4x4-20A	 65 52	°C /W
θ_{JC}	Thermal Resistance-Junction to Case(Note 3) QFN3x3-20 QFN4x4-20A	 10 7	

Note 2: Please refer to "Layout Recommendation", the PGND PIN on the central of the IC should connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.
Note 3: The case temperature is measured at the center of the PGND PIN on the underside of the SSOP-24 package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		3.1 ~ 5.8	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$, MUTE	1.4 ~ V_{DD}	
		SE/$\overline{BTL}$	0.8 V_{DD} ~ V_{DD}	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$, MUTE	0 ~ 0.5	
		SE/$\overline{BTL}$	0 ~ 1.0	
V_{ICM}	Common Mode Input Voltage		1 ~ V_{DD}-1	
T_A	Ambient Temperature Range		-40 ~ 85	°C
T_J	Junction Temperature Range		-40 ~ 125	
R_L	Speaker Resistance		3.5 ~	Ω

Electrical Characteristics

V_{DD}=5V, V_{GND}=0V, T_A=25°C, Gain=20dB (unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (BTL)	V_{MUTE}=0V, $V_{\overline{SD}}$=5V, No Load	-	8	20	mA
I_{DD}	Supply Current (SE)	V_{MUTE}=0V, $V_{\overline{SD}}$=5V, No Load	-	2	5	mA
I_{MUTE}	Supply Current (BTL Mute Mode)	V_{MUTE}=5V, $V_{\overline{SD}}$=5V, No Load	-	8	20	mA
I_{MUTE}	Supply Current (SE Mute Mode)	V_{MUTE}=5V, $V_{\overline{SD}}$=5V, No Load	-	2	5	mA
I_{SD}	Supply Current (SD Mode)	V_{MUTE}=0V, $V_{\overline{SD}}$=0V, No Load	-	-	1	μA
I_i	Input Current	$\overline{SD}$, MUTE, VOLUME	-	-	1	
F_{OSC}	Oscillator Frequency	(V_{DD}=3.3~5.5V, T_A= -40~85°C)	400	500	600	kHz
R_i	Input Resistance(BTL)	Gain=20dB	-	36	-	kΩ
R_i	Input Resistance(SE)	Gain=3.5dB	-	59	-	kΩ

Copyright©ANPEC Electronic Corp.

Electrical Characteristics (Cont.)

V_{DD}=5V, V_{GND}=0V, T_A=25°C, Gain=20dB (unless otherwise noted)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
R_{DSON}	Static Drain-Source On-State Resistance	V_{DD}=5.5V, I_L=0.8A	P-channel Power MOSFET	-	220	-	mΩ
			N-channel Power MOSFET	-	200	-	
		V_{DD}=4.5V, I_L=0.6A	P-channel Power MOSFET	-	230	-	
			N-channel Power MOSFET	-	210	-	
		V_{DD}=3.6V, I_L=0.4A	P-channel Power MOSFET	-	250	-	
			N-channel Power MOSFET	-	220	-	
$T_{START-UP}$	Start-Up Time from shutdown	Bypass Capacitor, Cb=2.2μF		-	1.4	-	S
V_{BYPASS}		VDD=5V, CB=2.2uF		-	2.5	-	V
V_{UVP}	External undervoltage detection			1.125	1.25	1.375	V
I_{hys}	External undervoltage detection hystereis current	UVP Release		4.5	5	5.5	μA
		UVP		0.9	1	1.1	μA

Operating Characteristics, BTL mode

V_{DD}=5V, TA=25°C, Gain=20dB

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	2.2	2.55	-	W
			R_L=8Ω	1.0	1.44	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	3.14	-	
			R_L=8Ω	-	1.77	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω P_O=1.7W	-	0.1	0.3	%
			R_L=8Ω P_O=1W	-	0.08	0.2	
Crosstalk	Channel separation	P_O=0.2W, R_L=4Ω, f_{in}=1kHz		-	-95	-	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-55	-	
			f_{in}=1kHz	-	-60	-	
SNR	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=8Ω		-	-86	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-90	-	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-120	-	
V_n	Output Noise	With A-weighting Filter (Gain=20dB)		-	50	-	μVrms
V_{OS}	Output Offset Voltage	R_L=4Ω (Gain=20dB)		-	5	30	mV

Operating Characteristics, BTL mode

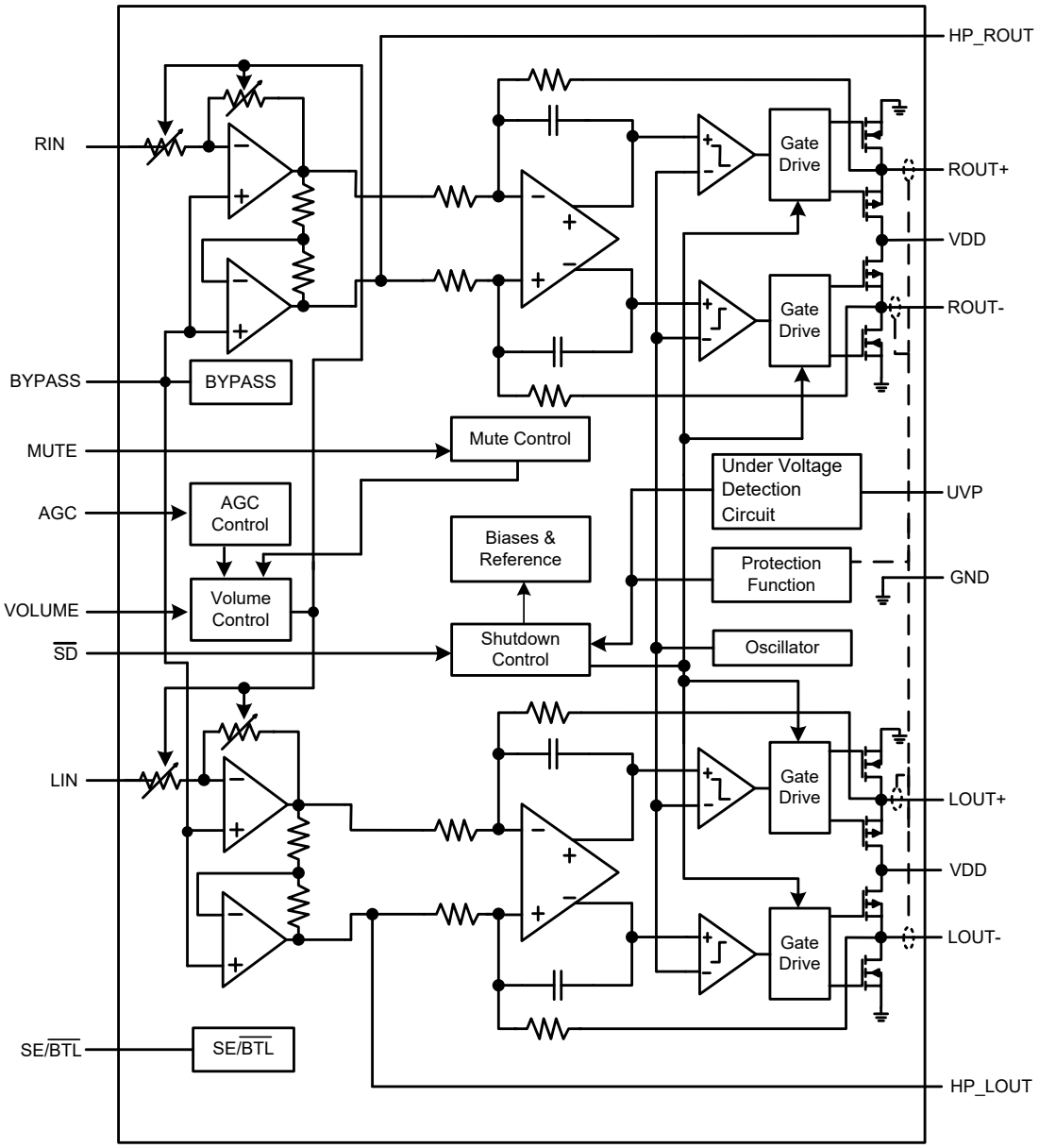
V_{DD}=3.6V, TA=25°C, Gain=20dB							
Symbol	**Parameter**	**Test Condition**		**Min.**	**Typ.**	**Max.**	**Unit**
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	1.1	1.29	-	W
			R_L=8Ω	0.6	0.74	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	1.58	-	
			R_L=8Ω	-	0.9	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω P_O=0.8W	-	0.2	0.3	%
			R_L=8Ω P_O=0.5W	-	0.1	0.3	
Crosstalk	Channel separation	P_O=0.1W, R_L=4Ω, f_{in}=1kHz		-	-95	-	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-55	-	
			f_{in}=1kHz	-	-60	-	
SNR	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=8Ω		-	-86	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-90	-	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-120	-	
V_n	Output Noise	With A-weighting Filter (Gain=20dB)		-	50	-	μVrms
V_{OS}	Output Offset Voltage	R_L=4Ω (Gain=20dB)		-	5	30	mV

Operating Characteristics, SE mode

V_{DD}=5V, TA=25°C, Gain=3.5dB							
Symbol	**Parameter**	**Test Condition**		**Min.**	**Typ.**	**Max.**	**Unit**
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=16Ω	90	120	-	mW
			R_L=32Ω	60	75	-	
		THD+N=10% f_{in}=1kHz	R_L=16Ω	-	150	-	
			R_L=32Ω	-	95	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=32Ω P_O=42.5mW	-	0.02	-	%
Crosstalk	Channel separation	P_O=6mW, R_L=32Ω, f_{in}=1kHz		-	-90	-	dB
PSRR	Power Supply Rejection Ratio	R_L=32Ω, Input AC-Ground	f_{in}=100Hz	-	-70	-	
			f_{in}=1kHz	-	-70	-	
SNR	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=32Ω		-	-100	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=32Ω, V_{in}=1V_{rms}		-	-100	-	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=32Ω, V_{in}=1V_{rms}		-	-100	-	
V_n	Output Noise	With A-weighting Filter (Gain=3.5dB)		-	10	-	μVrms

Copyright©ANPEC Electronic Corp.

Block Diagram

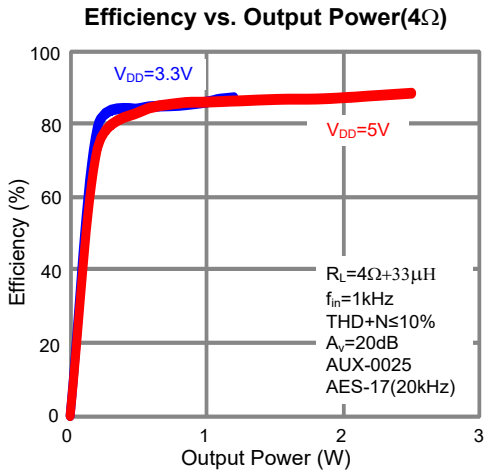


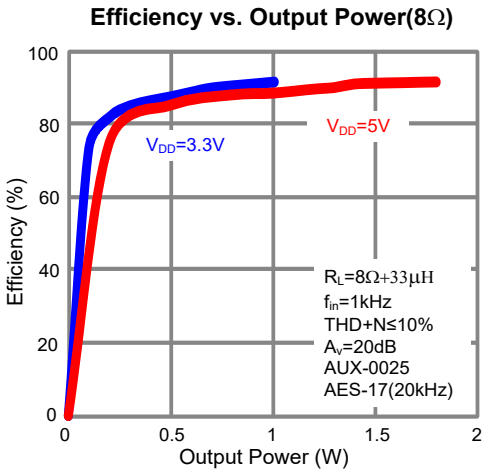
Pin Function Description

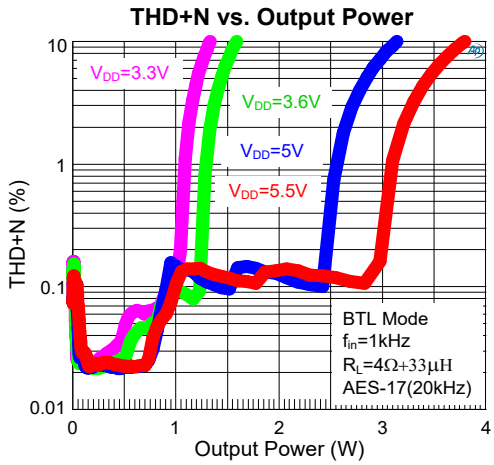
NO.	Name	Function Description
3	$\overline{SD}$	Shutdown mode control input. Pulling low voltage on this pin shuts off the IC.
4	BYPASS	Bias voltage for power amplifiers.
5	RIN	Negative input of right channel power amplifier.
6, 18	GND	Power amplifier's ground.
7	LIN	Negative input of left channel power amplifier.
8	VOLUME	Internal gain setting input.
9	MUTE	Mute control signal input, hold low for normal operation, hold high to mute.
10	SE/$\overline{BTL}$	Output mode control input, high for SE output mode and low for BTL mode.
11	AGC	Maximum output power setting input.
12	UVP	Under voltage protection input.
13, 16, 20	VDD	Control and bias block's power supply.
14	HP_LOUT	Headphone output of left channel power amplifier.
2	HP_ROUT	Headphone output of right channel power amplifier.
15	LOUT-	Negative output of left channel power amplifier.
17	LOUT+	Positive output of left channel power amplifier.
19	ROUT+	Positive output of right channel power amplifier.
1	ROUT-	Negative output of right channel power amplifier.

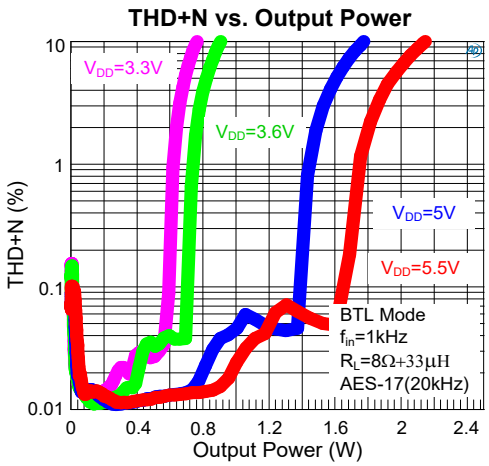
Copyright©ANPEC Electronic Corp.

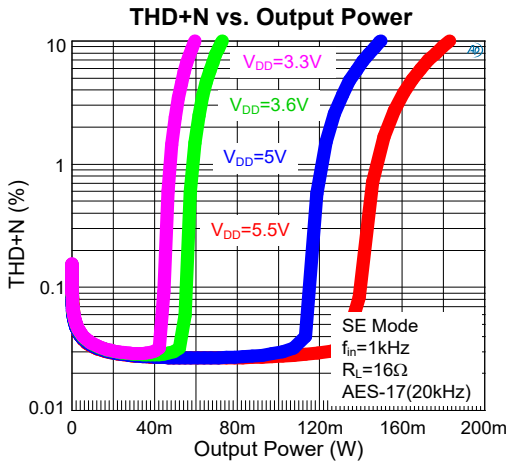
Typical Operating Characteristics

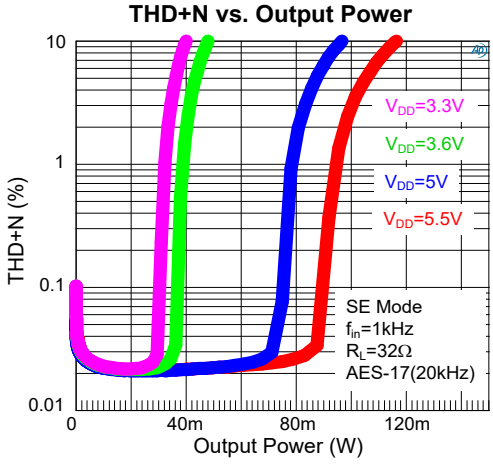






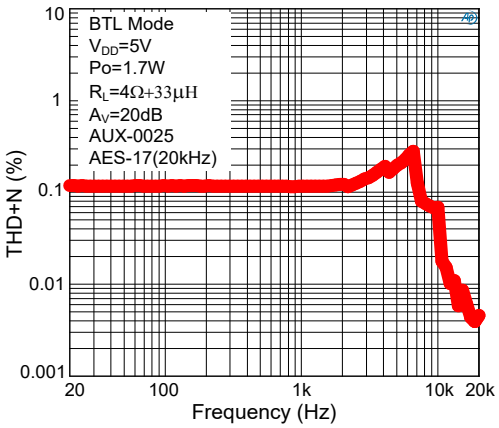




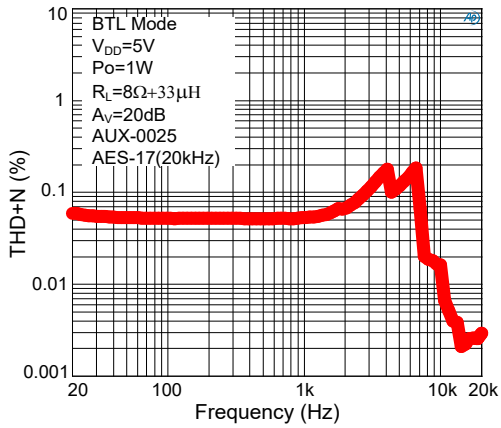


Typical Operating Characteristics

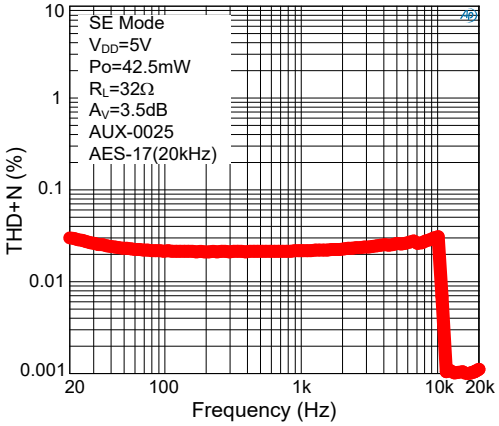
THD+N vs. Frequency



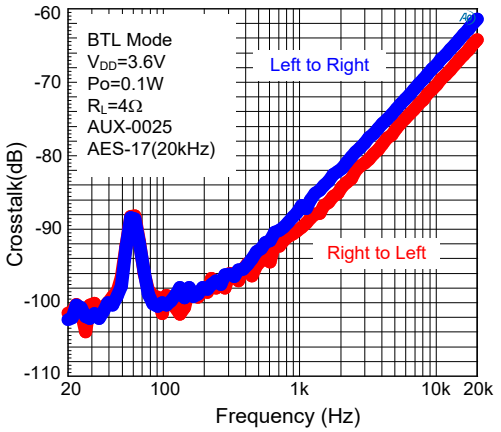
THD+N vs. Frequency



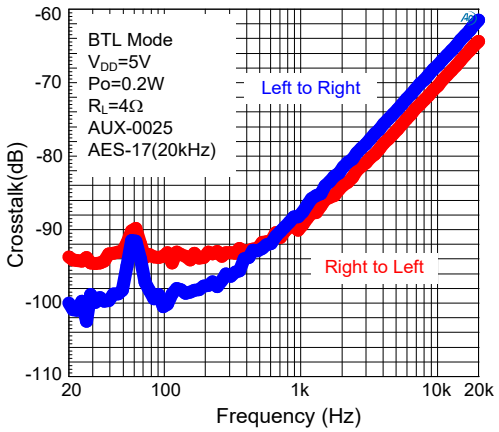
THD+N vs. Frequency



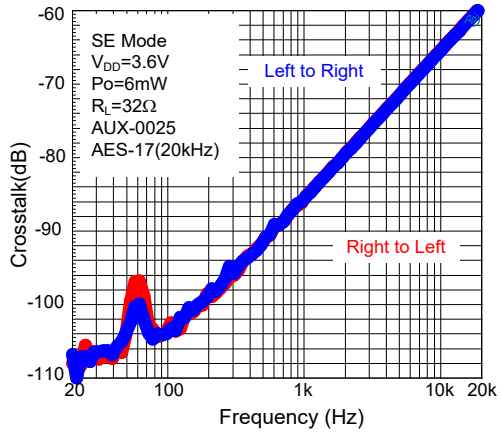
Crosstalk vs. Frequency



Crosstalk vs. Frequency

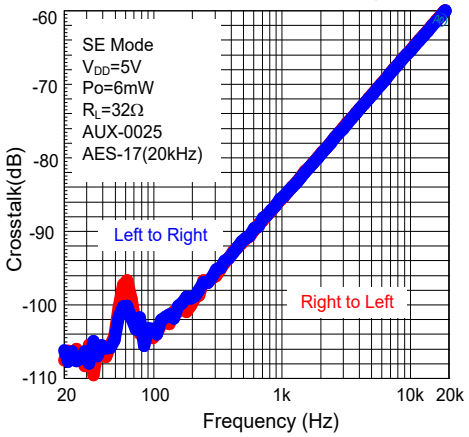


Crosstalk vs. Frequency

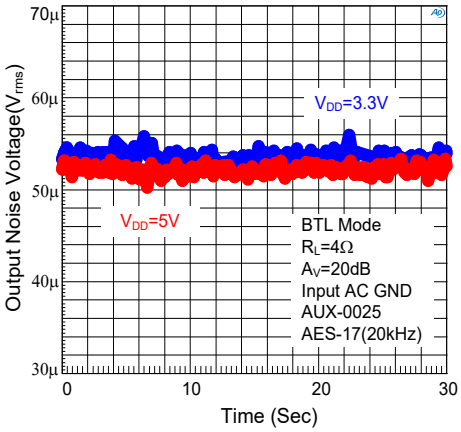


Typical Operating Characteristics

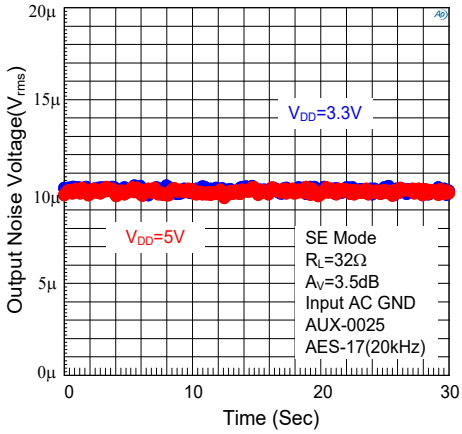
Crosstalk vs. Frequency



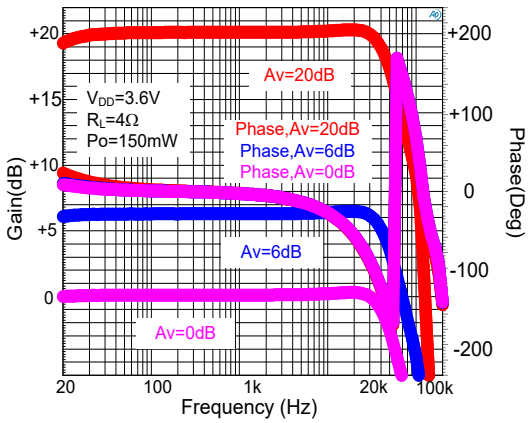
Output Noise Voltage vs. Time



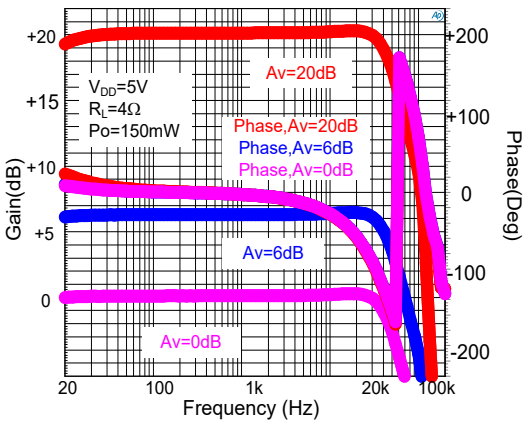
Output Noise Voltage vs. Time



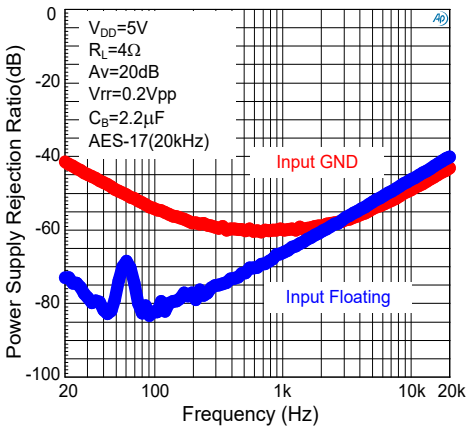
Frequence Response



Frequence Response

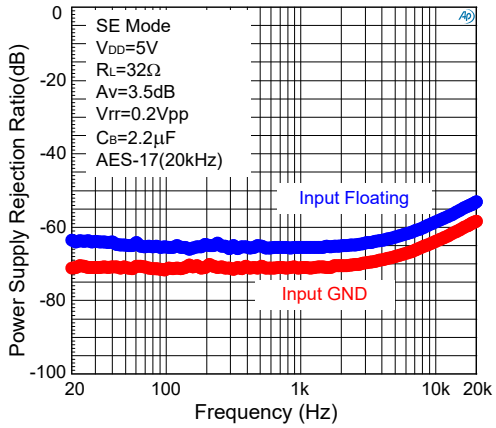


PSRR vs. Frequency

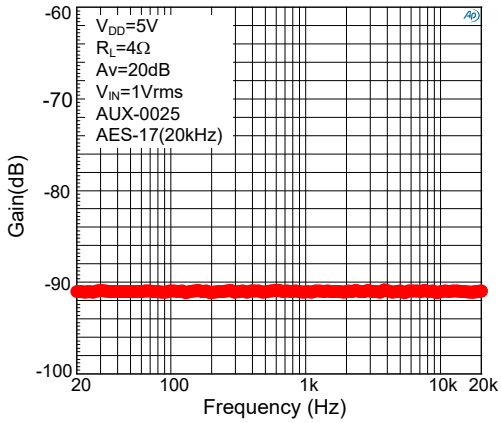


Typical Operating Characteristics

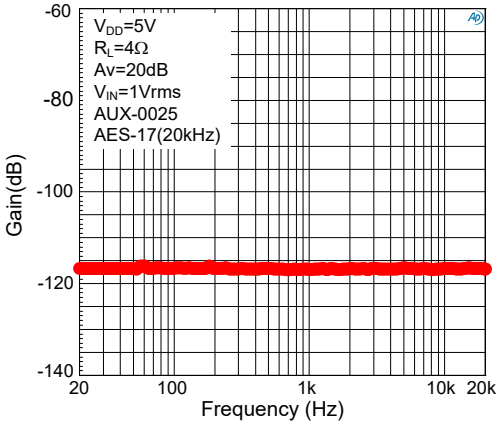
PSRR vs. Frequency



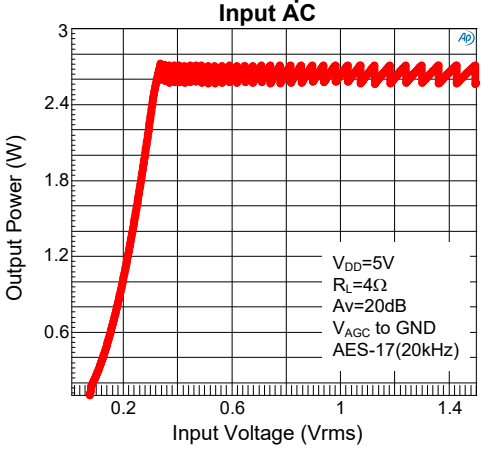
Mute Attenuation vs. Frequence



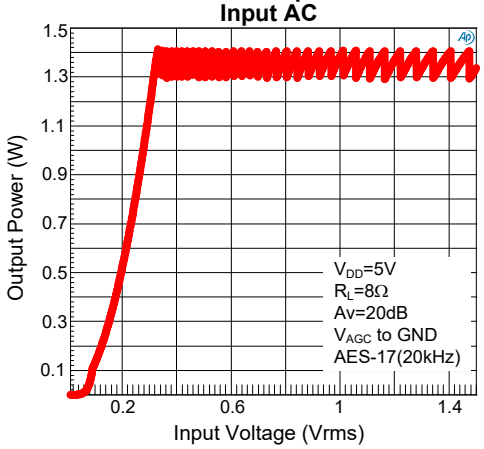
Shutdown Attenuation vs. Frequence



AGC Function Output Power vs. Input AC

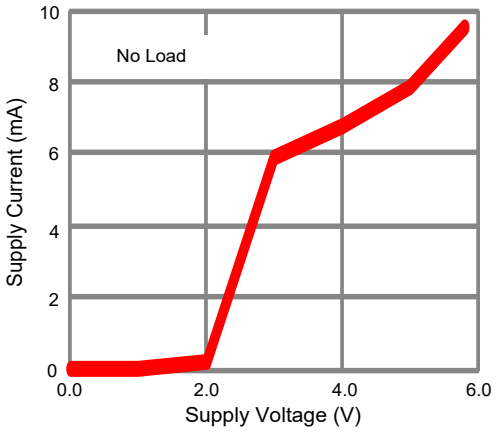


AGC Function Output Power vs. Input AC

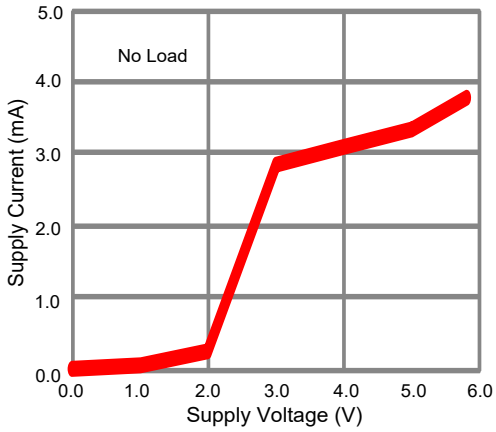


Typical Operating Characteristics

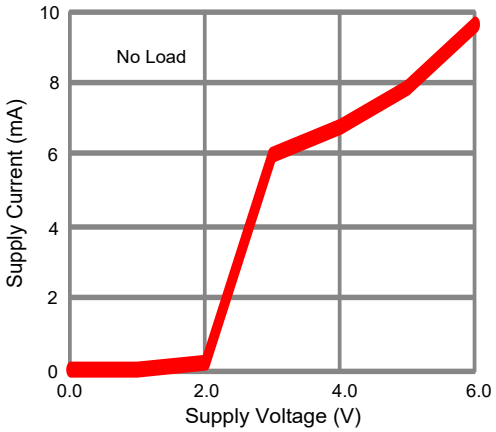
Supply Current vs. Supply Voltage(BTL)



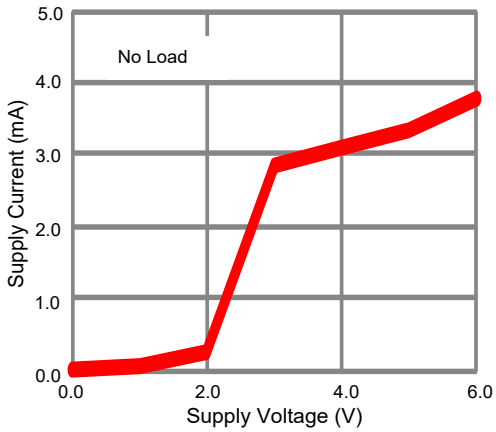
Supply Current vs. Supply Voltage(SE)



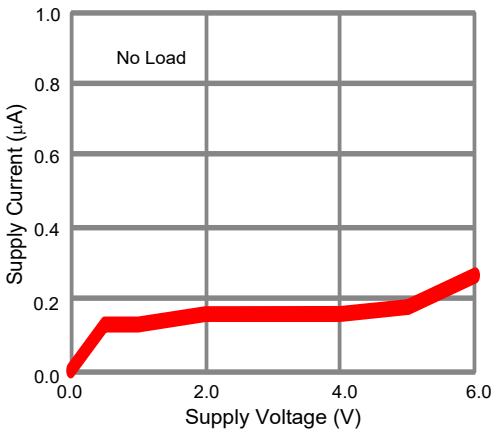
Mute Current vs. Supply Voltage(BTL)



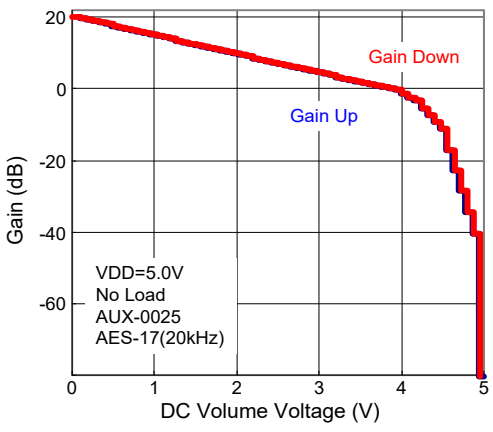
Mute Current vs. Supply Voltage(SE)



Shutdown Current vs. Supply Voltage

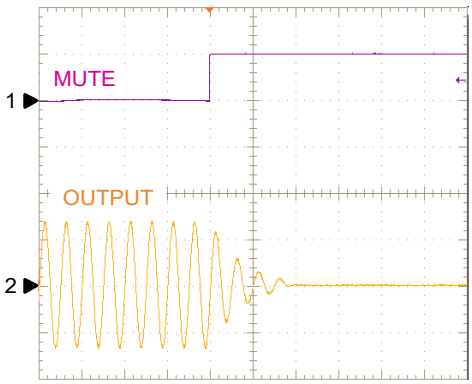


Gain vs. Volume Voltage



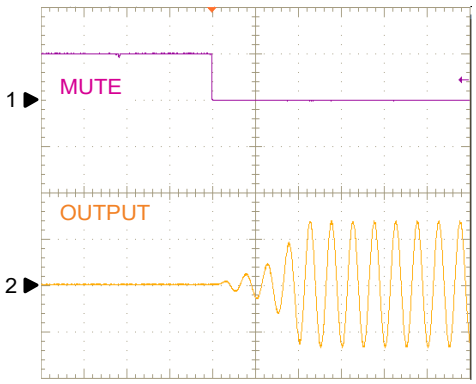
Typical Operating Characteristics

Mute



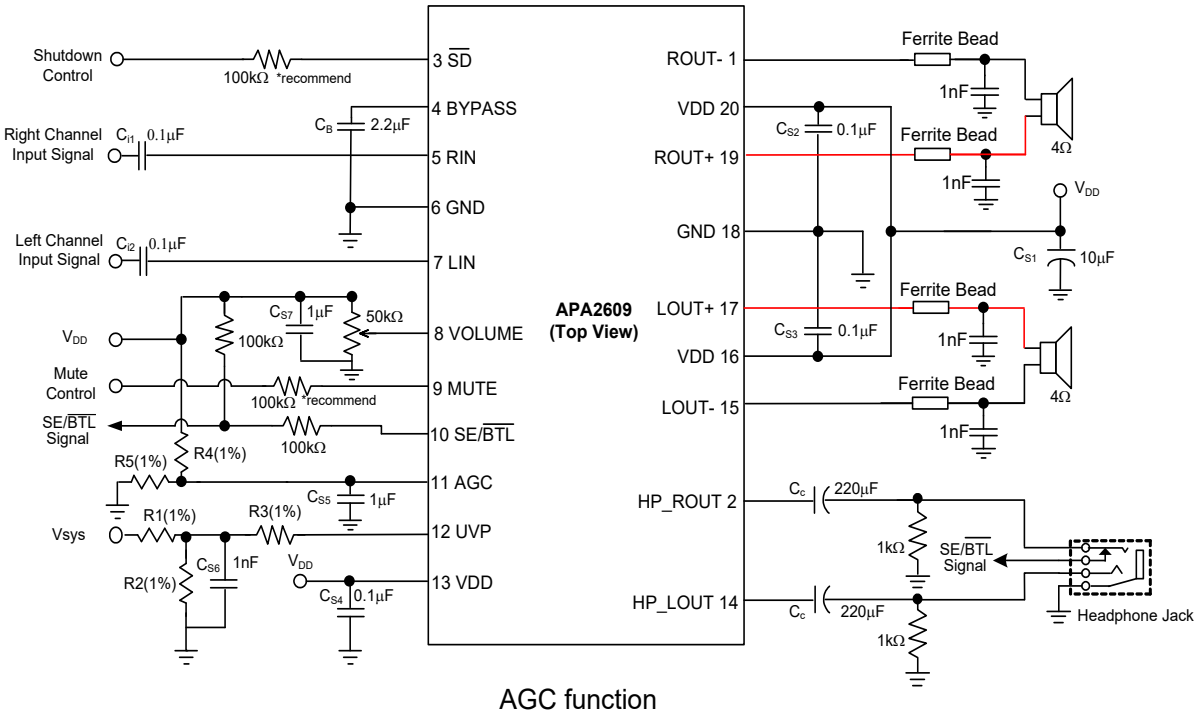
CH1:MUTE,5V/Div, DC
CH2:OUTPUT,2V/Div, DC
TIME:2mS/Div

Mute Release

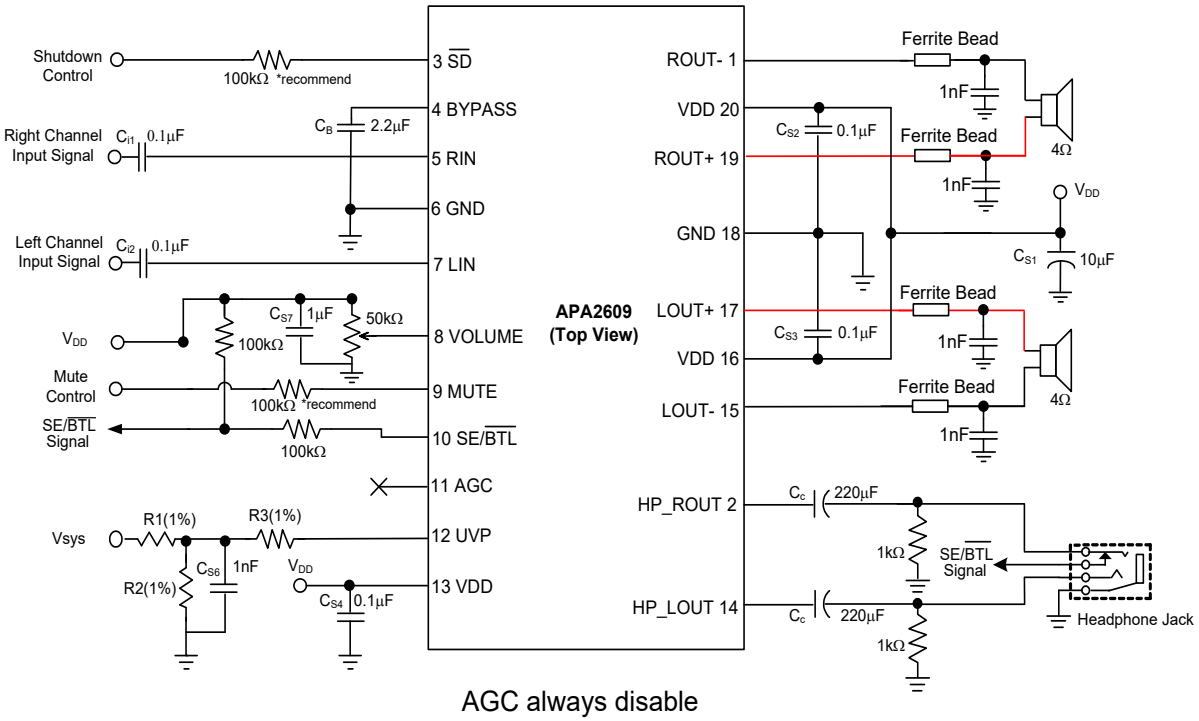


CH1:MUTE,5V/Div, DC
CH2:OUTPUT,2V/Div, DC
TIME:2mS/Div

Typical Application Circuit



AGC function



AGC always disable

DC Volume Control Table

V_{DD}=5V, V_{GND}=0V, No Load, T_A=25°C

Step	BTL Gain(dB)	SE Gain(dB)	Down (%)	Down (V)	Up (%)	Up (V)	Recom(%)	Recom (V)
			Volume H to L		Volume L to H			
1	20.0	3.5	1.70	0.09	0.00	0.00	0.00	0.00
2	19.6	3.2	3.25	0.16	2.20	0.11	2.73	0.14
3	19.2	2.9	4.80	0.24	3.75	0.19	4.28	0.21
4	18.8	2.6	6.35	0.32	5.30	0.27	5.83	0.29
5	18.4	2.3	7.90	0.40	6.85	0.34	7.38	0.37
6	18.0	1.7	9.45	0.47	8.40	0.42	8.93	0.45
7	17.6	1.4	11.00	0.55	9.95	0.50	10.48	0.52
8	17.2	1.1	12.55	0.63	11.50	0.58	12.03	0.60
9	16.8	0.8	14.10	0.71	13.05	0.65	13.58	0.68
10	16.4	0.5	15.65	0.78	14.60	0.73	15.13	0.76
11	16.0	0.2	17.20	0.86	16.15	0.81	16.68	0.83
12	15.6	-0.2	18.75	0.94	17.70	0.89	18.23	0.91
13	15.2	-0.5	20.30	1.02	19.25	0.96	19.78	0.99
14	14.8	-0.8	21.85	1.09	20.80	1.04	21.33	1.07
15	14.4	-1.2	23.40	1.17	22.35	1.12	22.88	1.14
16	14.0	-1.5	24.95	1.25	23.90	1.20	24.43	1.22
17	13.6	-1.5	26.50	1.33	25.45	1.27	25.98	1.30
18	13.2	-1.8	28.05	1.40	27.00	1.35	27.53	1.38
19	12.8	-2.2	29.60	1.48	28.55	1.43	29.08	1.45
20	12.4	-2.5	31.15	1.56	30.10	1.51	30.63	1.53
21	12.0	-2.9	32.70	1.64	31.65	1.58	32.18	1.61
22	11.6	-3.2	34.25	1.71	33.20	1.66	33.73	1.69
23	11.2	-3.6	35.80	1.79	34.75	1.74	35.28	1.76
24	10.8	-3.9	37.35	1.87	36.30	1.82	36.83	1.84
25	10.4	-4.3	38.90	1.95	37.85	1.89	38.38	1.92
26	10.0	-4.6	40.45	2.02	39.40	1.97	39.93	2.00
27	9.6	-5.0	42.00	2.10	40.95	2.05	41.48	2.07
28	9.2	-5.4	43.55	2.18	42.50	2.13	43.03	2.15
29	8.8	-5.7	45.10	2.26	44.05	2.20	44.58	2.23
30	8.4	-6.1	46.65	2.33	45.60	2.28	46.13	2.31
31	8.0	-6.4	48.20	2.41	47.15	2.36	47.68	2.38
32	7.6	-6.8	49.75	2.49	48.70	2.44	49.23	2.46

Copyright©ANPEC Electronic Corp.

DC Volume Control Table (Cont.)

V_{DD}=5V, V_{GND}=0V, No Load, T_A=25°C

Step	BTL Gain(dB)	SE Gain(dB)	Down (%)	Down (V)	Up (%)	Up (V)	Recom(%)	Recom (V)
			Volume H to L		Volume L to H			
33	7.2	-7.2	51.30	2.57	50.25	2.51	50.78	2.54
34	6.8	-7.5	52.85	2.64	51.80	2.59	52.33	2.62
35	6.4	-7.9	54.40	2.72	53.35	2.67	53.88	2.69
36	6.0	-8.3	55.95	2.80	54.90	2.75	55.43	2.77
37	5.6	-8.6	57.50	2.88	56.45	2.82	56.98	2.85
38	5.2	-9	59.05	2.95	58.00	2.90	58.53	2.93
39	4.8	-9.4	60.60	3.03	59.55	2.98	60.08	3.00
40	4.4	-9.8	62.15	3.11	61.10	3.06	61.63	3.08
41	4.0	-10.1	63.70	3.19	62.65	3.13	63.18	3.16
42	3.6	-10.5	65.25	3.26	64.20	3.21	64.73	3.24
43	3.2	-10.9	66.80	3.34	65.75	3.29	66.28	3.31
44	2.8	-11.3	68.35	3.42	67.30	3.37	67.83	3.39
45	2.4	-11.6	69.90	3.50	68.85	3.44	69.38	3.47
46	2.0	-12	71.45	3.57	70.40	3.52	70.93	3.55
47	1.6	-12.4	73.00	3.65	71.95	3.60	72.47	3.62
48	1.2	-12.8	74.55	3.73	73.50	3.68	74.02	3.70
49	0.8	-13.1	76.10	3.81	75.05	3.75	75.57	3.78
50	0.4	-13.5	77.65	3.88	76.60	3.83	77.12	3.86
51	0.0	-13.9	79.20	3.96	78.15	3.91	78.67	3.93
52	-1.0	-14.9	80.75	4.04	79.70	3.99	80.22	4.01
53	-2.0	-15.8	82.30	4.12	81.25	4.06	81.77	4.09
54	-3.0	-16.8	83.85	4.19	82.80	4.14	83.32	4.17
55	-5.0	-18.8	85.40	4.27	84.35	4.22	84.87	4.24
56	-7.0	-20.7	86.95	4.35	85.90	4.30	86.42	4.32
57	-9.0	-22.7	88.50	4.43	87.45	4.37	87.97	4.40
58	-11.0	-24.7	90.05	4.50	89.00	4.45	89.52	4.48
59	-17.0	-30.7	91.60	4.58	90.55	4.53	91.07	4.55
60	-23.0	-36.9	93.15	4.66	92.10	4.61	92.62	4.63
61	-29.0	-43	94.70	4.74	93.65	4.68	94.17	4.71
62	-35.0	-49.3	96.25	4.81	95.20	4.76	95.72	4.79
63	-41.0	-55.3	97.80	4.89	96.75	4.84	97.27	4.86
64	-80.0	-80	100.00	5.00	98.30	4.92	100.00	5.00

Copyright©ANPEC Electronic Corp.

Function Descriptions

Class D Operation

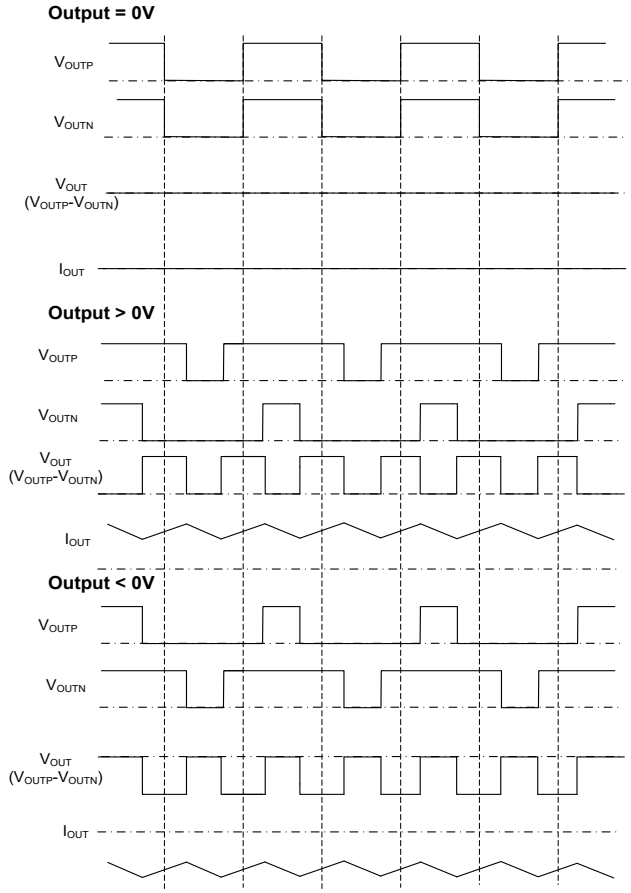
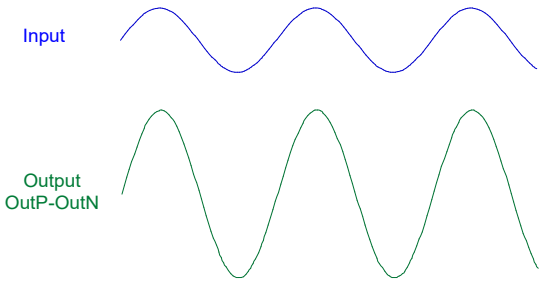


Figure1. The APA2609 Output Waveform (Voltage& Current)



Input vs. Output Waveform

The APA2609 power amplifier modulation scheme is shown in figure 1; the outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals.When output > 0V, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when Output <0V, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load, and reduces the I^2R losses in the load that improve the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminate in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Bypass Voltage

The bypass voltage is about $V_{DD}/2$. It is the common reference voltage of internal circuits.

The external capacitor (C_B) for this reference is a critical component and should be close to BYPASS pin as possible.

DCVolume Control Function

The APA2609 has an internal stereo volume control whose setting is the function of the DC voltage applied to the VOLUME input pin. The APA2609 volume control consists of 64 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps controlled by the DC voltage, are from +20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in the table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the "DC Volume Control Graph".

For the highest accuracy, the voltage shown in the "recommended voltage" column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions.

The gain step is 0.4dB/step from 20dB to 0dB , 1dB/step from 0dB to -3dB, 2dB/step from -3dB to -11dB, and 6dB/step from -11dB to -41db.

The last gain setting is actually the same as MUTE MODE

AGC(Non-Clipping)Function

The APA2609 provides the 64 steps non-clipping control, and the range is from 20dB to -80dB. When the output reaches the maximum power setting value, the internal Programmable Gain Amplifier (PGA) will decrease the gain to prevent the output waveform clipping. This feature prevents speaker damage from being overstressed. Using the AGC pin to set the non-clipping function and limit the output power.

Table 1: AGC Setting Threshold v.s Output Power

AGC Function	Output Power
VDD~0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$P_O = \frac{8(½VDD-V_{AGC})^2}{RL}$ x0.95
0.27VDD~GND	(Max Output Power 4Ω) Po=2.7W (Max Output Power 8Ω) Po=1.4W

MUTE Operation

When place the logic high on MUTE pin, the APA2609's outputs runs at a constant 50% duty cycle, and the APA2609 is at mute state. Place the logic low on MUTE pin enables the outputs, and the output changes the duty cycle with the input signal. This pin could be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. The MUTE pin must not be floating.

It features smooth mute function when activation or deactivation mute mode to minimize pop noise.

Copyright©ANPEC Electronic Corp.

Function Descriptions (Cont.)

Shutdown Operation

In order to reduce power consumption while not in use, the APA2609 contains a shutdown function. By switching the $\overline{SD}$ pin to GND level, the amplifier enters a low-consumption-current state. On normal operating, APA2609's $\overline{SD}$ pin should pull to VDD level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Over Current Protection

The APA2609 monitors the output current, and when the current exceeds the current-limit threshold, the APA2609 turn-off the output stage to prevent the output device from damages in over-current or short-circuit condition. The IC will turn-on the output buffer after 200ms, but if the overcurrent or short-circuits condition is still remain, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has be removed.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA2609. When the junction temperature exceeds $T_{J=}$+140°C, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about 110°C. The thermal protection is designed with a 30 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Under Voltage Protection

External under voltage detection can be used to Shutdown the APA2609 before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.25V.
The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application.
The thresholds can be determined as below:

With the condition: R3 >> R1//R2
V_{UVP}=[1.25-(IHys+initial)xR3]x(R1+R2)/R2
Hysteresis=IHys x R3 x (R1+R2)/R2
I_{Hys}=5uA(typ)
initial=1uA(typ)

For example, to obtain VUVP=3.325V and 1V hysteresis, R1=3kΩ, R2=1.2kΩ and R3=50kΩ. Only if external voltage V_{system} is lower than the shutdown thershold VUVP, the APA2609 is in shutdown mode.
On the other hand, V_{system} could be pulled higher than V_{Hys} (VUVP + hysteresis=4.2V(typ)) to keep the IC out of shutdown mode.

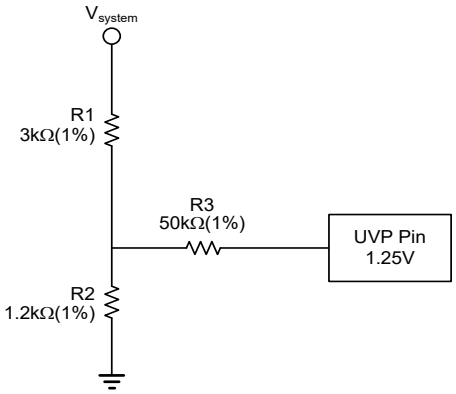


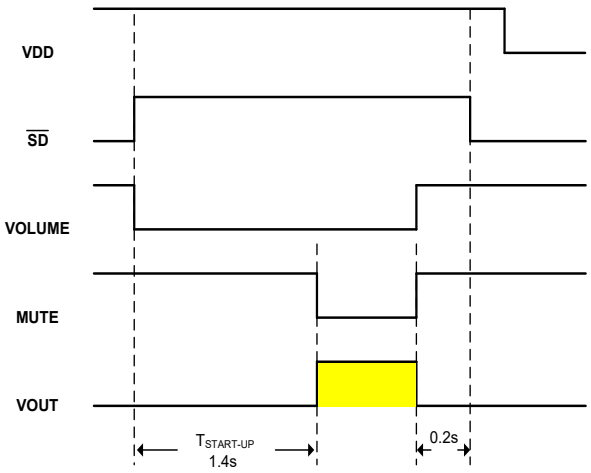
Figure 2. Under-Voltage Protection

DC Detect

If one of the differential output is 100% duty (i.e. always High state), and the other is 0% duty (i.e. always Low state) for 125msec, it will trigger DC protection to force output driver into Hi-Z state from damaging speaker. To restore from DCP fault, reset IC or fix the root cause which make output saturate at full duty.

Power Sequence

This sequence is used to prevent power on/off POP situation.
After VDD is ready, pulling high the SD pin and set the VOLUME to desired level.
Then Un-Mute it after Tstartup. To shut down APA2609, MUTE it or force VOLUME to VDD first. After a period of time (0.2sec for example), shut down IC before ramps VDD down.

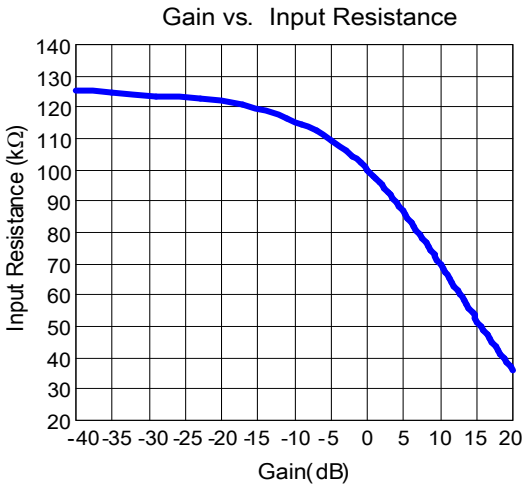


Application Information

Square Wave into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jumping out the air gap and defacing the voice coil. However, this depends on the amplitude and frequency of the square wave. For 500kHz switching frequency, this is an issue for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor, R_i



For achieving the 64 steps gain setting, it varies the input resistance network (R_i & R_f) of amplifier. The input resistor's range form smallest to maximum is about 3.5 times. Therefore, the input high-pass filter's low cutoff frequency will change 3.5 times from low to high. The cutoff frequency can be calculated by equation 1.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 36kΩ (minimum) and the specification calls for a flat bass response down to 50Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.08μF, so a 0.1uF is chosen. To avoid start-up pop noise, Ci should be under 0.1*Cb. A further consideration for this capacitor is its leakage. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' inputs are held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

The bypass capacitance affects the startup time. It is determined in the following equation:

$$T_{START-UP}=0.56(sec/\mu F) \times C_B + 0.2(sec) \quad (3)$$

The Cb is places close to BYPASS pin as possible to avoid external noise coupling.
Large Cb improves PSRR especially in lower bandwidth (<1kHz), but increases Tstartup.

Ferrite Bead Selection

If the traces form APA2609 to speaker are short, the ferrite bead filters as shown in Figure 3 might be adequate to meet the FCC & CE required.
A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output Low-Pass Filter

If the traces form APA2609 to speaker are short, it doesn't require output filter for FCC & CE standard.
A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The Figure 3 is the sample for added ferrite bead; the ferrite shows choosing high impedance in high frequency.

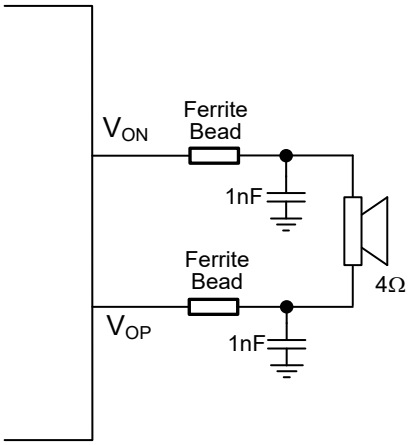


Figure 3. Ferrite bead output filter

Application Information (Cont.)

Output Low-Pass Filter (Cont.)

Figure 4 and 5 are examples of LC filter configurations. It's recommended for the situation that the trace form amplifier to speaker is too long and needs to eliminate the radiated emission or EMI.

Filters should be placed closely to OUT pins for minimized EMI.

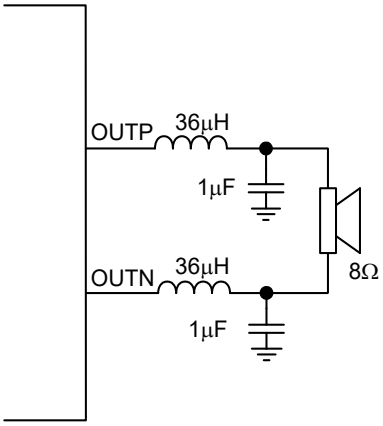


Figure 4. LC output filter for 8Ω speaker

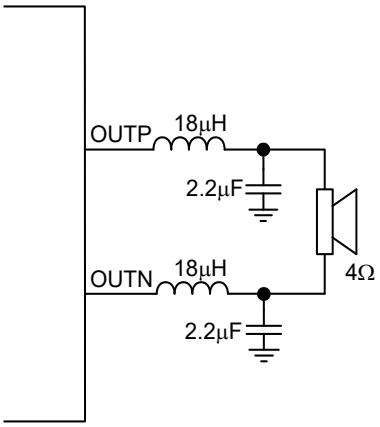


Figure 5. LC output filter for 4Ω speaker

Figure 4 and 5's low pass filter cut-off frequency are 25kHz (F_C).

$$f_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

Power-Supply Decoupling Capacitor, C_S

The APA2609 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure low THD. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the VDD pin. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

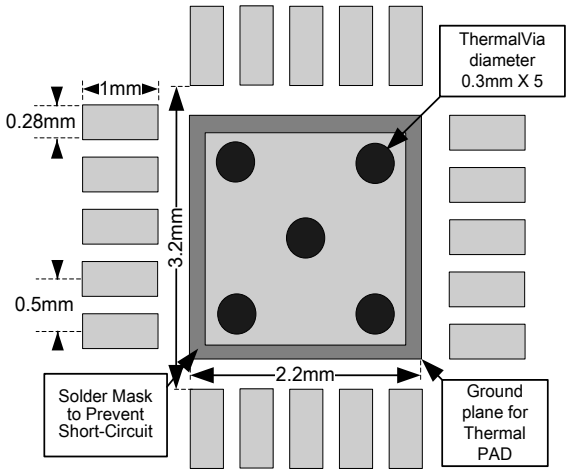


Figure 6. QFN4x4-20A Land Pattern Recommendation

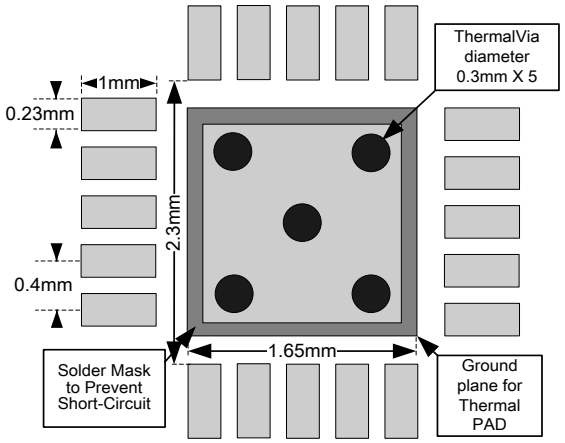
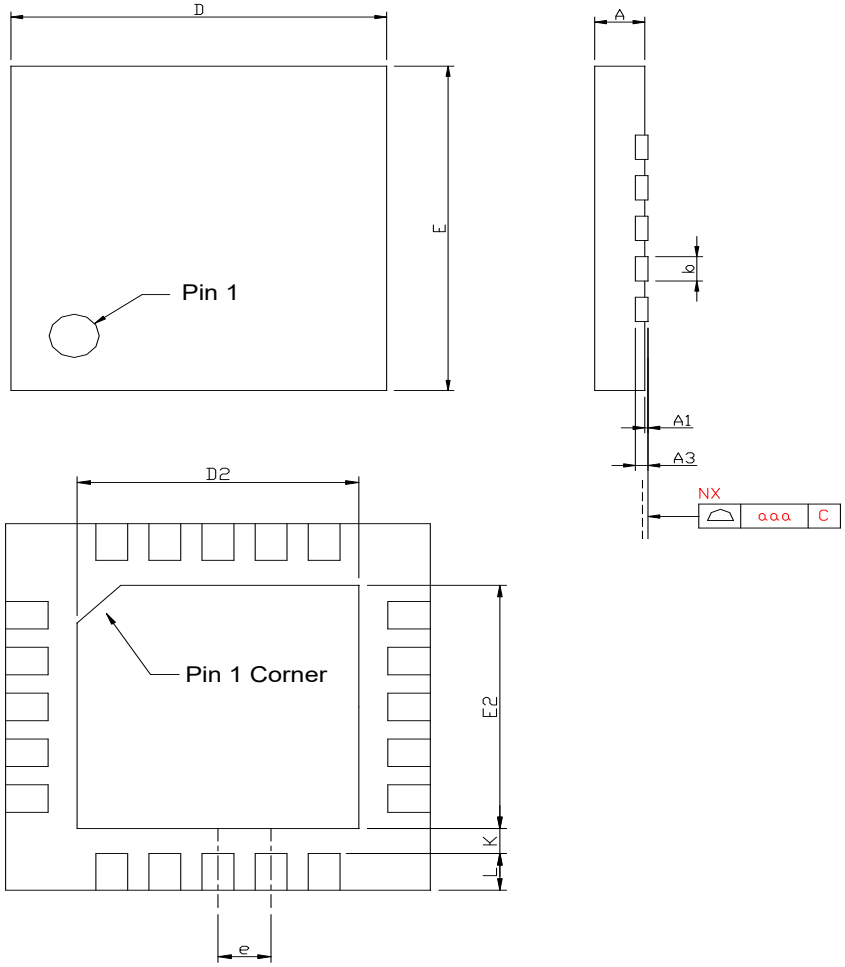


Figure7. QFN3x3-20 Land Pattern Recommendation

1. All components should be placed close to the APA2609. For example, the input capacitor (C_i) should be close to APA2609's input pins to avoid causing noise coupling to APA2609's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2609's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The QFN4X4-20A Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short-circuit) except the Thermal PAD area.

Package Information

QFN4x4-20A

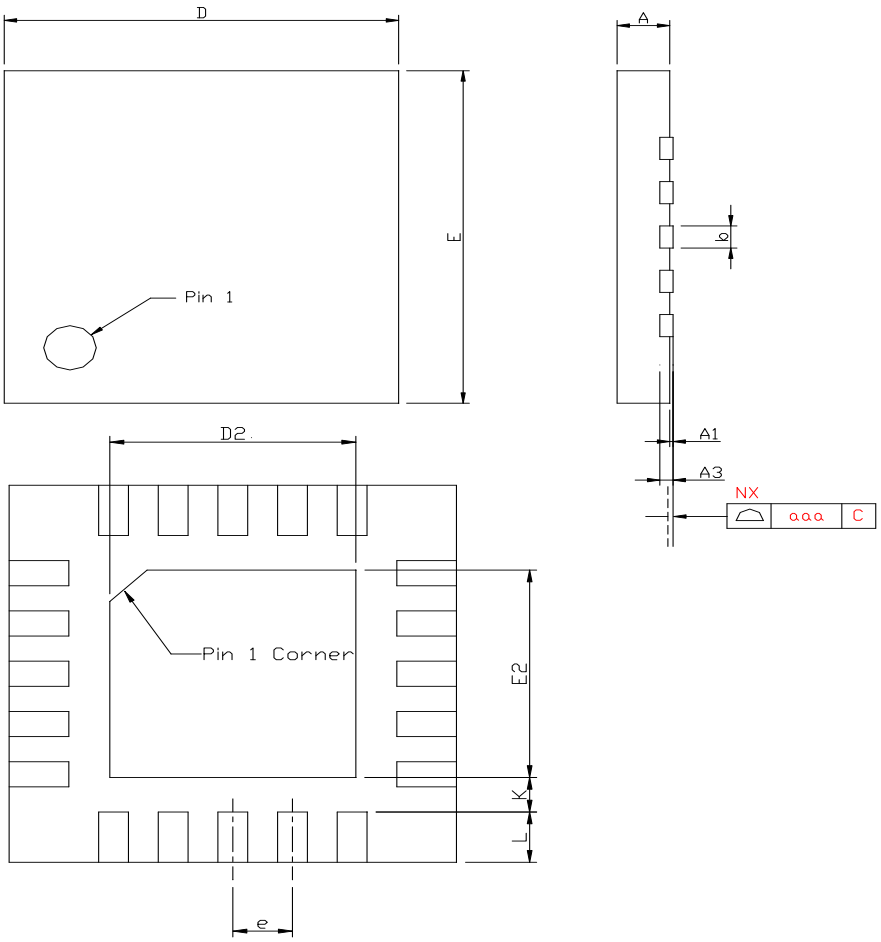


SYMBOL	QFN4*4-20A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.50	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.50	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 VGGD-5.

Package Information

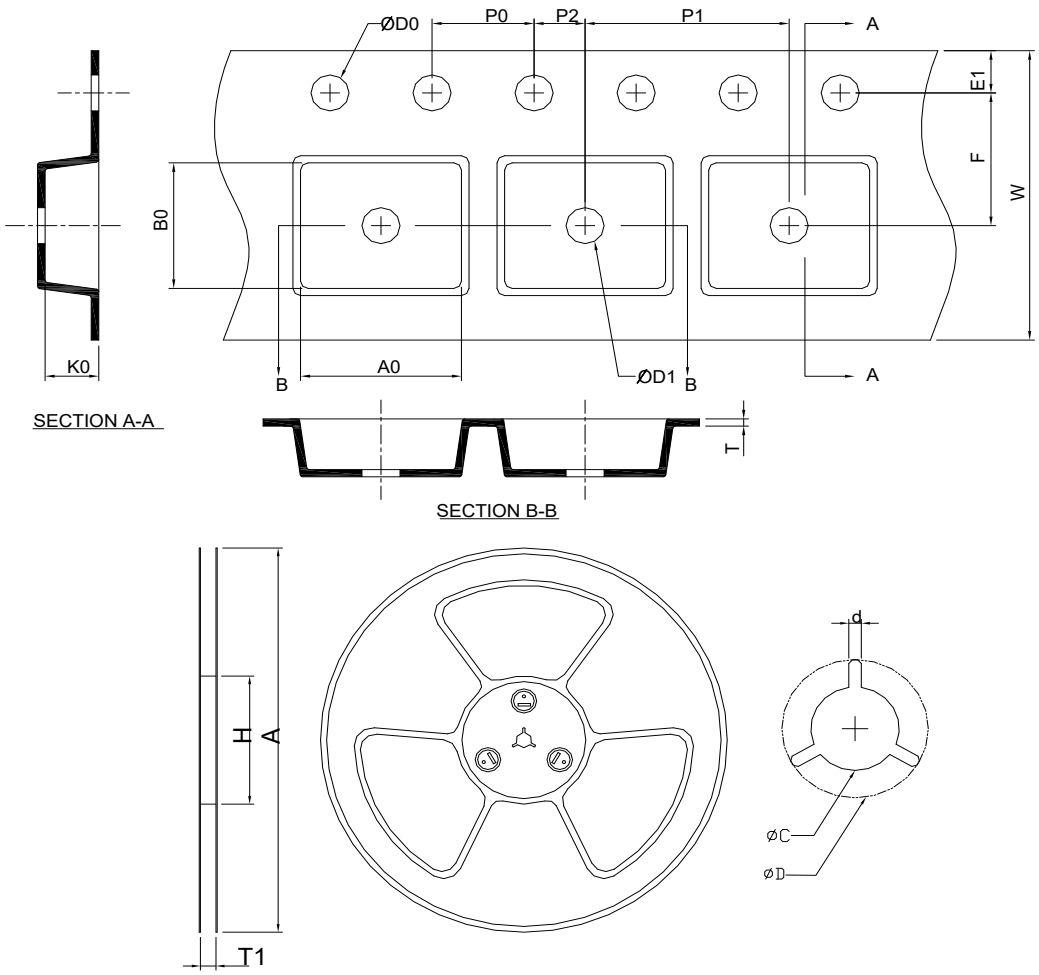
QFN3x3-20



SYMBOL	QFN3*3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN 4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QFN 3x3	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

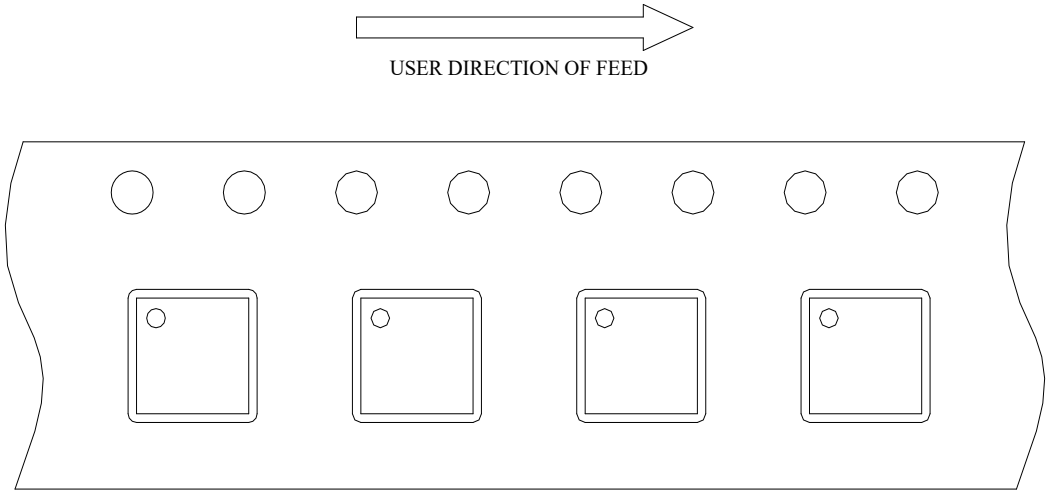
(mm)

Devices Per Unit

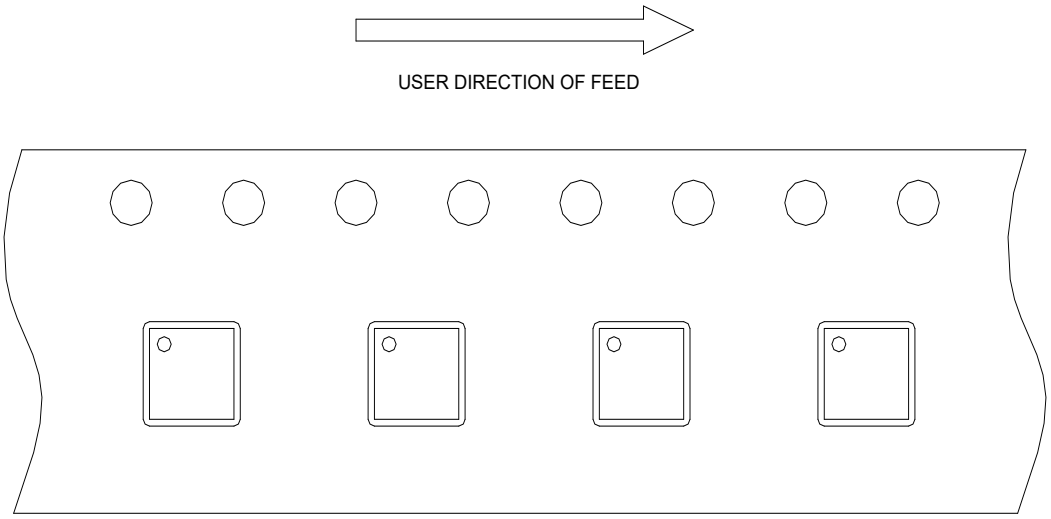
Package type	Packing	Quantity
QFN 4x4	Tape & Reel	3000
QFN 3x3	Tape & Reel	3000

Taping Direction Information

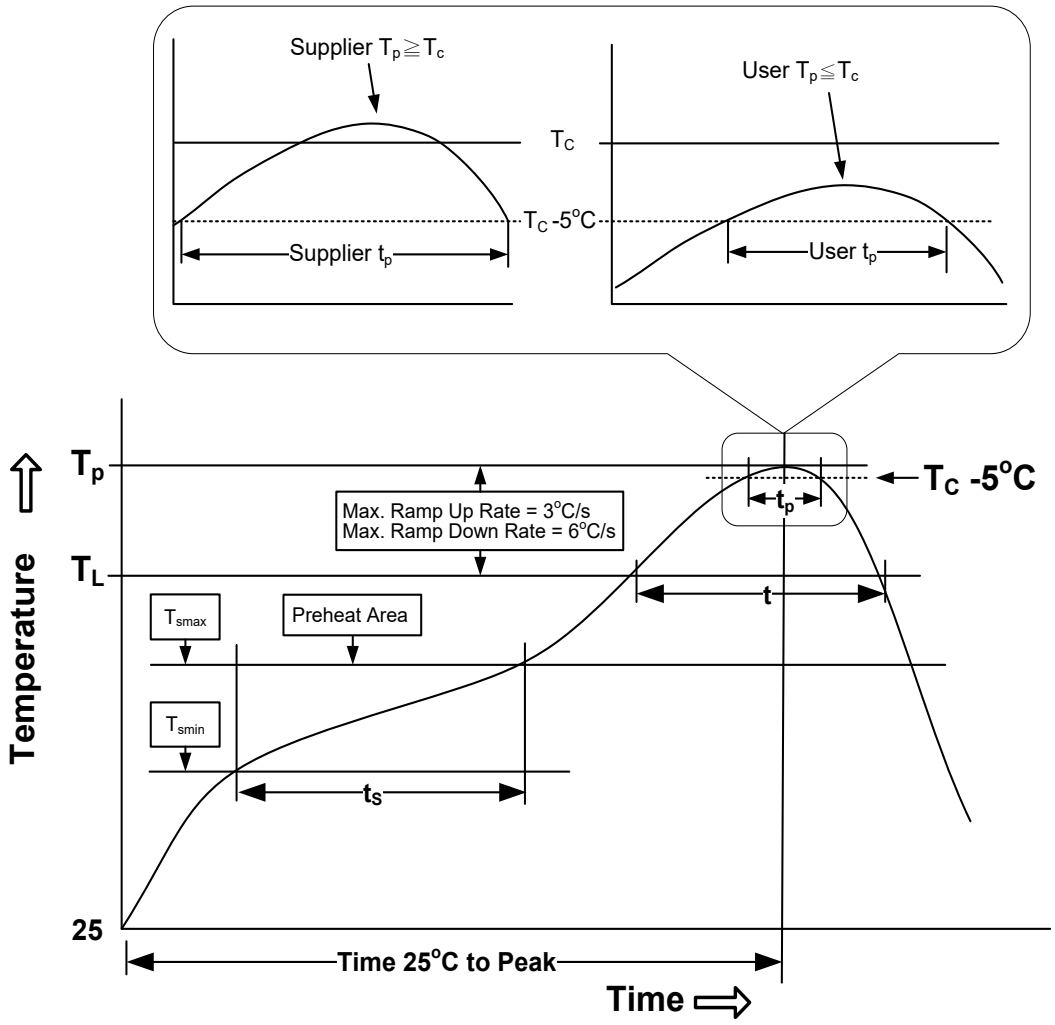
QFN4x4-20A



QFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

Copyright©ANPEC Electronic Corp.

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Duxing 1st Rd., East Dist.,
Hsinchu City 300096, Taiwan (R.O.C.)
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No.11, Ln. 218, Sec. 2, Zhongxing Rd., Xindian Dist.,
New Taipei City 231037, Taiwan (R.O.C.)
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838