

Features

- **62mΩ Power Switch On Resistance**
- **Wide Supply Voltage Range: 2.7V to 5.5V**
- **Fix Current Limit Protection**
- **Fast Over current Response: 2us (typ.)**
- **Over-Temperature Protection**
- **Fault Indication Output**
- **Enable Input**
- **Built-in Soft-Start**
- **Reverse Input-Output Voltage Protection: 25mV (typ.)**
- **UL Approved-File No. E328191**
- **UL-CB Scheme IEC/EN62368-1 Certified**
- **TUV IEC/EN62368-1 Certified**

Applications

- **Notebook and Desktop Computers**
- **USB Ports**
- **High-Side Power Protection Switches**
- **MHL Ports**

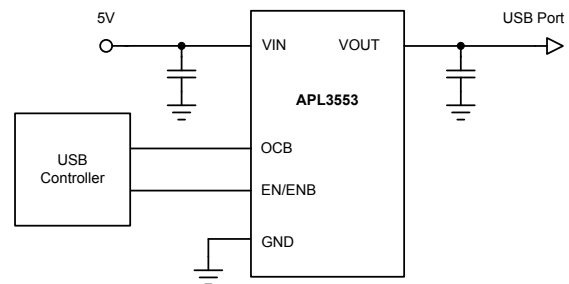
General Description

The APL3553I/J series of power switches are designed for USB applications. The 62mΩ N-channel MOSFET power switch satisfies the voltage drop requirements of USB specification.

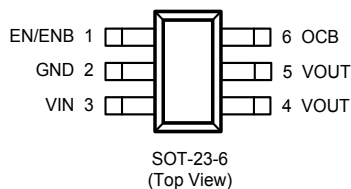
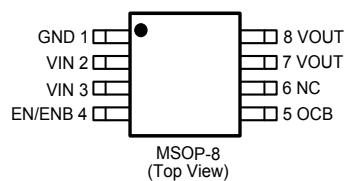
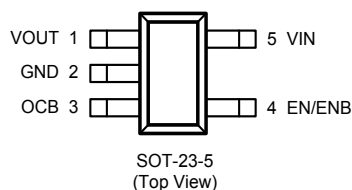
The protection features include current-limit protection, short-circuit protection, and over-temperature protection. The device limits the output current at current limit threshold level. When V_{OUT} drops below $V_{IN}-1V$, the devices limit the current to a lower and safe level. The over-temperature protection limits the junction temperature below 140°C in case of short circuit or over load conditions.

Other features include a deglitched OCB output to indicate the fault condition and an enable input to enable or disable the device.

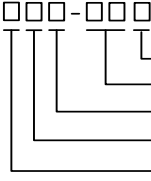
Simplified Application Circuit



Pin Configurations



Ordering and Marking Information

APL3553  Assembly Material Handling Code Temperature Range Package Code EN Function	Package Code B: SOT-23-5 C: SOT-23-6 X:MSOP-8 Operating Ambient Temperature Range I: -40 to 85°C Handling Code TR: Tape & Reel EN Function I: Active High J: Active Low Assembly Material G: Halogen and Lead Free Device
APL3553 B: 53OX	X - Date Code O - EN Function Code
APL3553 C: 53OX	X - Date Code O - EN Function Code
APL3553 X: L553O XXX XX	X - Date Code O - EN Function Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	-0.3 ~ 7	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 7	V
V_{ENB}, V_{EN}	EN, ENB to GND Voltage	-0.3 ~ 7	V
V_{OCB}	OCB to GND Voltage	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	SOT-23-5	°C/W
		SOT-23-6	
		MSOP-8	
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 2)	SOT-23-5	°C/W
		SOT-23-6	
		MSOP-8	

Note 2 : θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 5.5	V
I_{OUT}	OUT Output Current (APL3553I/J)	0 ~ 2	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

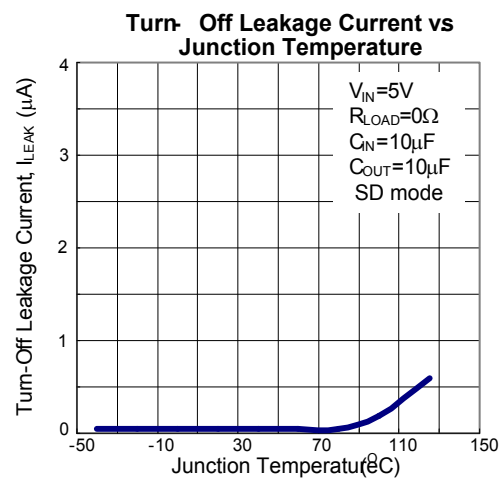
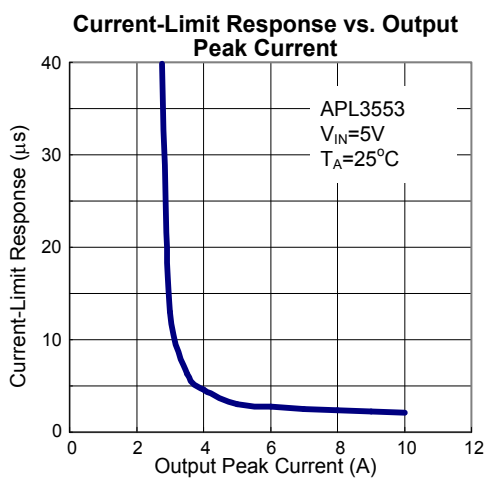
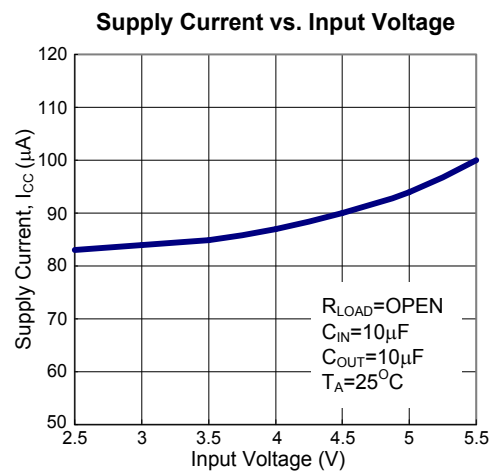
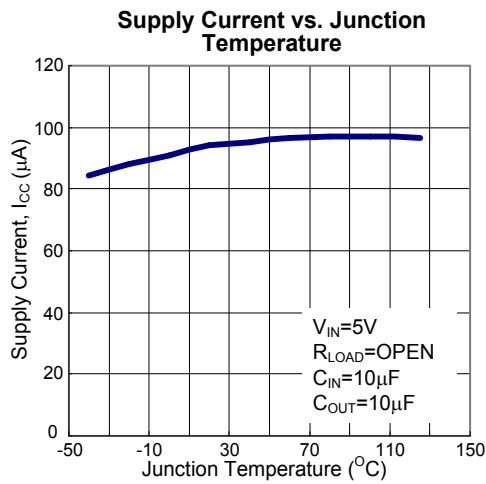
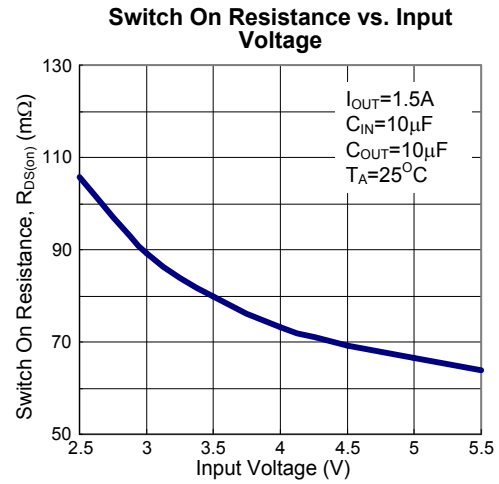
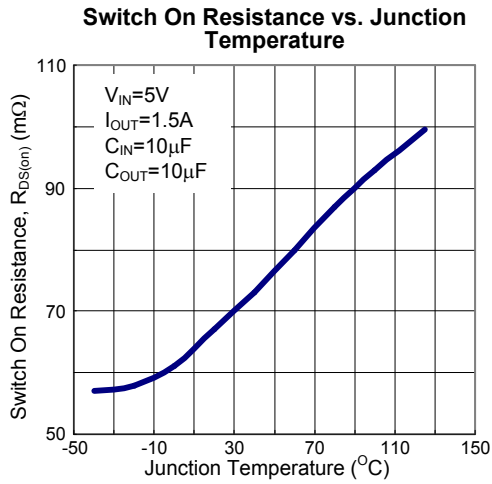
Note 3 : Refer to the typical application circuit

Electrical Characteristics

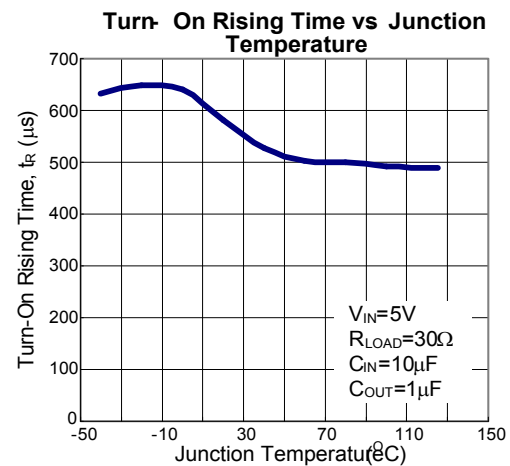
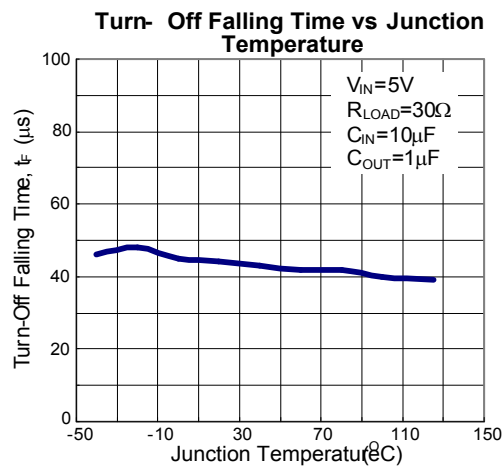
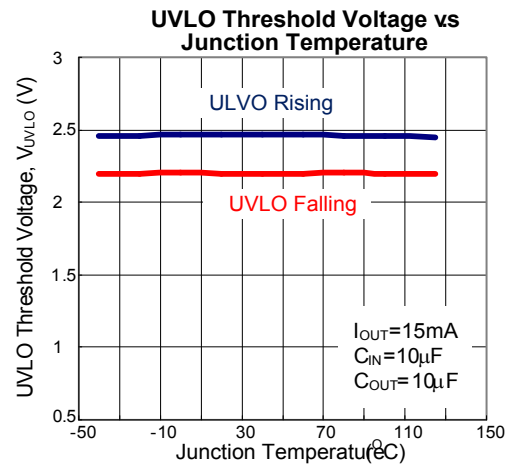
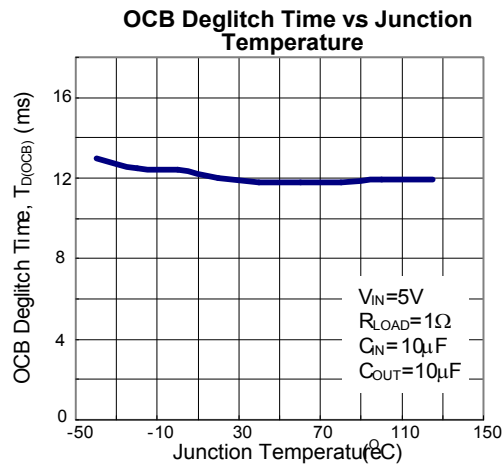
Unless otherwise specified, these specifications apply over $V_{IN}=5V$, $V_{EN}=5V$ or $V_{ENB}=0V$ and $T_A=-40 \sim 85^\circ C$. Typical values are at $T_A=25^\circ C$.

Symbol	Parameter	Test Conditions	APL3553I/J			Unit	
			Min.	Typ.	Max.		
SUPPLY CURRENT							
	VIN Supply Current	No load, V _{EN} =0V or V _{ENB} =5V	-	-	1	μA	
		No load, V _{EN} =5V or V _{ENB} =0V	-	65	-	μA	
	Leakage Current	VOUT=GND, V _{EN} =0V or V _{ENB} =5V	-	-	1	μA	
	Reverse Leakage Current	VIN=GND, V _{OUT} =5V, V _{EN} =0V or V _{ENB} =5V	-	-	1	μA	
POWER SWITCH							
R _{DS(ON)}	Power Switch On Resistance	I _{OUT} =1.5A, T _A = 25 °C	SOT-23-5 Package	-	62	78	mΩ
UNDER-VOLTAGE LOCKOUT (UVLO)							
	VIN UVLO Threshold Voltage	V _{IN} rising, T _A = -40 ~ 85 °C	1.7	-	2.65	V	
	VIN UVLO Hysteresis		-	0.2	-	V	
CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTIONS							
I _{LIM}	Current Limit Threshold	APL3553I/J V _{IN} =5V, T _A = 25 °C	2.7	3.2	3.9	A	
I _{SHORT}	Short-Circuit Output Current	APL3553I/J V _{IN} =5V, T _A = 25 °C	-	2.2	-	A	
OCB OUTPUT PIN							
	OCB Output Low Voltage	I _{OCB} =5mA	-	0.2	0.4	V	
	OCB Leakage Current	V _{OCB} =5V	-	-	1	μA	
t _{D(OCB)}	OCB Deglitch Time	OCB assertion, T _A = -40 ~ 85 °C	5	12	20	ms	
EN OR ENB INPUT PIN							
V _{IH}	Input Logic HIGH	V _{IN} =5V	1.4	-	-	V	
V _{IL}	Input Logic LOW	V _{IN} =5V	-	-	0.6	V	
	Input Current		-	-	1	μA	
	VOUT Discharge Resistance	V _{EN} =0V or V _{ENB} =5V	-	150	-	Ω	
t _{D(ON)}	Turn On Delay Time		-	80	-	μs	
t _{D(OFF)}	Turn Off Delay Time		-	5	-	μs	
t _{SS}	Soft-Start Time	No load, C _{OUT} =1μF, V _{IN} =5V	500	-	2000	μs	
OVER-TEMPERATURE PROTECTION (OTP)							
T _{OTP}	Over-Temperature Threshold	T _J rising	-	140	-	°C	
	Over-Temperature Hysteresis		-	20	-	°C	
REVERSE VOLTAGE PROTECT							
I _{REV}	Reverse current trip point	Enable reverse current protection	-	100	-	mA	
V _{REV}	Reverse voltage comparator trip point	V _{IN} -V _{OUT} , disable reverse current protection	-	25	-	mV	
T _{REV}	Time from reverse current condition to MOSFET turn off	V _{IN} =5V	3	5	7	ms	

Typical Operating Characteristics

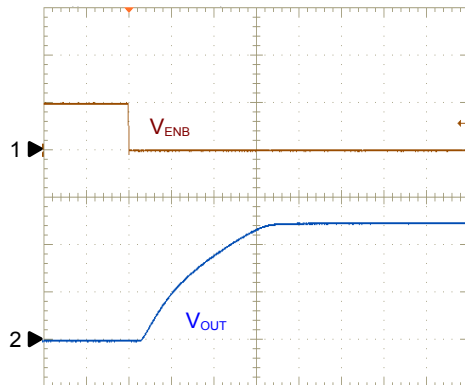


Typical Operating Characteristics (Cont.)



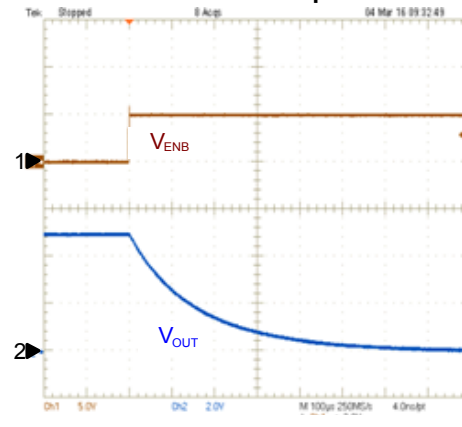
Operating Waveforms

Turn On Response



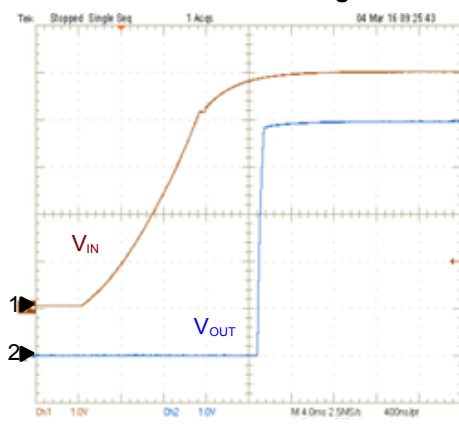
$V_{IN}=5V, C_{OUT}=10\mu F/\text{Electrolytic},$
 $C_{IN}=10\mu F/\text{Electrolytic}, R_{LOAD}=30\Omega$
 CH1: $V_{ENB}, 5V/\text{Div}, \text{DC}$
 CH2: $V_{OUT}, 2V/\text{Div}, \text{DC}$
 TIME: $200\mu s/\text{Div}$

Turn Off Response



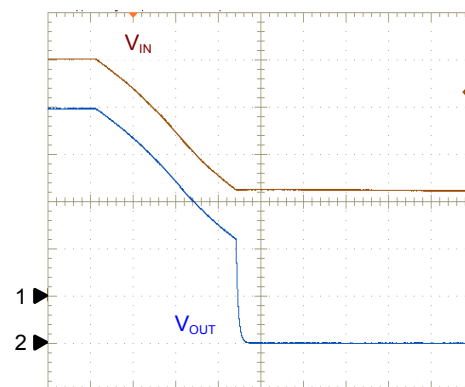
$V_{IN}=5V, C_{OUT}=10\mu F/\text{Electrolytic},$
 $C_{IN}=10\mu F/\text{Electrolytic}, R_{LOAD}=30\Omega$
 CH1: $V_{ENB}, 5V/\text{Div}, \text{DC}$
 CH2: $V_{OUT}, 2V/\text{Div}, \text{DC}$
 TIME: $100\mu s/\text{Div}$

UVLO at Rising



$V_{IN}=5V, C_{OUT}=10\mu F/\text{Electrolytic},$
 $C_{IN}=10\mu F/\text{Electrolytic}, R_{LOAD}=30\Omega$
 CH1: $V_{IN}, 1V/\text{Div}, \text{DC}$
 CH2: $V_{OUT}, 1V/\text{Div}, \text{DC}$
 TIME: $4ms/\text{Div}$

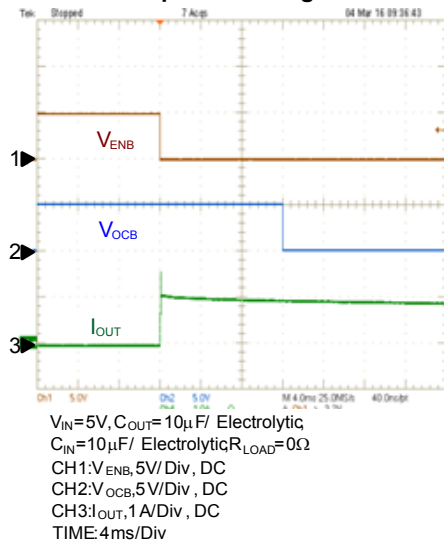
UVLO at Falling



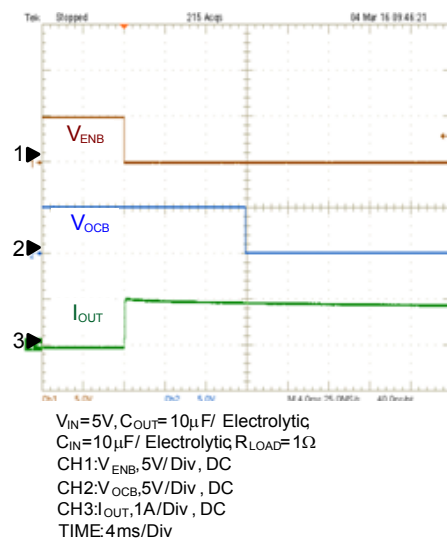
$V_{IN}=5V, C_{OUT}=10\mu F/\text{Electrolytic},$
 $C_{IN}=10\mu F/\text{Electrolytic}, R_{LOAD}=30\Omega$
 CH1: $V_{IN}, 1V/\text{Div}, \text{DC}$
 CH2: $V_{OUT}, 1V/\text{Div}, \text{DC}$
 TIME: $4ms/\text{Div}$

Operating Waveforms (Cont.)

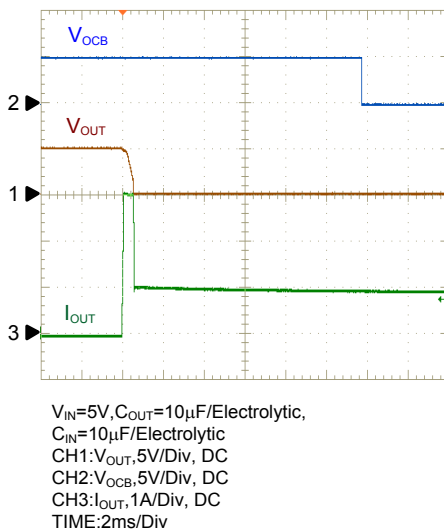
OCB Response During Short Circuit



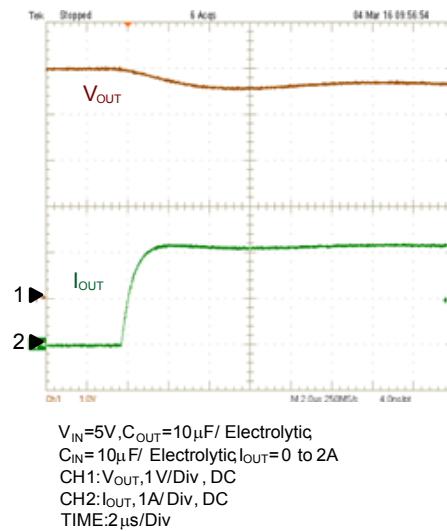
OCB Response During Over Load



OCB Response with Ramped Load



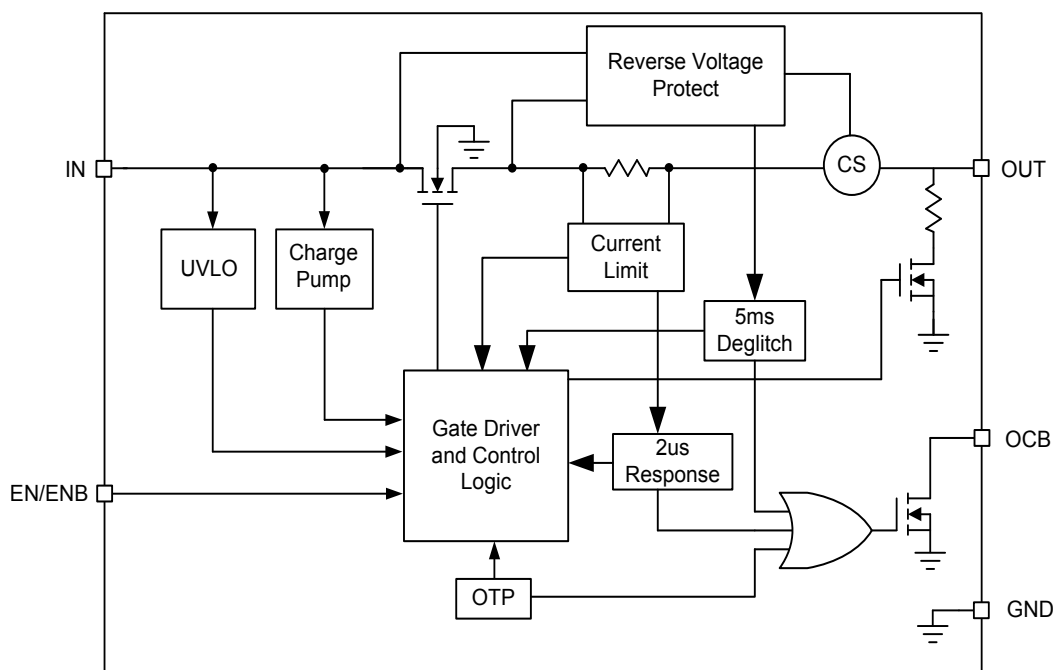
Load-Transient Response



Pin Description

PIN				FUNCTION
SOT-23-5	SOT-23-6	MSOP-8	NAME	
2	2	1	GND	Ground.
5	3	2,3	VIN	Power Supply Input. Connect this pin to external DC supply.
4	1	4	EN(53I)	Enable Input. Pulling this pin to high will enable the device and pulling this pin to low will disable device. The EN pin cannot be left floating.
			ENB(53J)	Enable Input. Pulling this pin to high will disable the device and pulling this pin to low will enable device. The ENB pin cannot be left floating.
3	6	5	OCB	Fault Indication Pin. This pin goes low when a current limit or an over-temperature condition is detected after a 12ms deglitch time.
1	4,5	7,8	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When ENB is high or EN is low, the output voltage is discharged by an internal resistor.
-	-	6	NC	No connection.

Block Diagram



The timing diagram illustrates the operational characteristics of the TPS22901. It shows the relationship between the input voltage (V_{IN}), enable signal (EN), output voltage (V_{OUT}), output current (I_{OUT}), and overcurrent block signal (OCB).

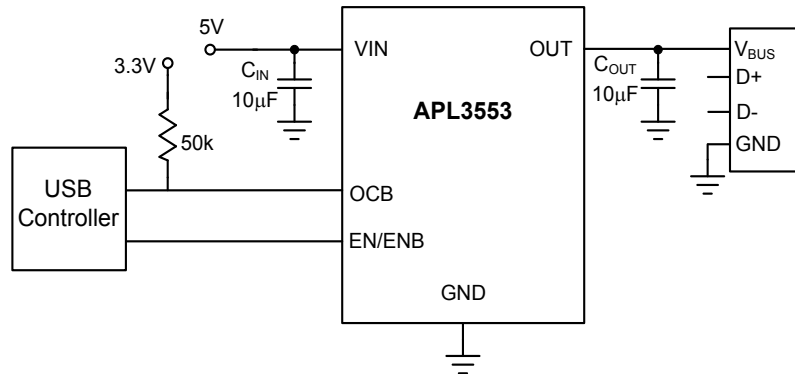
- Enable Transition:** When EN transitions from low to high, the output voltage V_{OUT} ramps up. The time to reach 10% of V_{OUT} is $T_{DI(ON)} = 80\mu s$. The time to reach 90% of V_{OUT} is $T_{SS} = 400\mu s$.
- Overcurrent Event:** When I_{OUT} exceeds the current limit, OCB transitions from high to low. The output voltage V_{OUT} drops to 0V. The time for V_{OUT} to drop to 0V is $T_{DI(OCB)} = 12ms$. The time for V_{OUT} to recover to 1.5V after OCB transitions back to high is $T_{IOS} = 2\mu s$.
- Standby Mode:** When EN transitions from high to low, the output voltage V_{OUT} ramps down. The time for V_{OUT} to reach 10% of V_{OUT} is $T_{ON} = 10ms$.

Timing diagram for the RCP release sequence. The diagram shows three signals: VIN-VOUT, IOU_T, and OCB. VIN-VOUT starts high, then drops to a level labeled $<-6\text{mV}$ for a duration of $<5\text{ms}$. It then rises to a level labeled $>-6\text{mV}$. IOU_T starts high, then drops to a level labeled 0A (Reverse Current trip point -100mA). It then rises to a level labeled Reverse Current trip point -100mA. The duration of the low state is labeled $T_{\text{REV}} >5\text{ms}$. OCB is high. Other labels include RCP release trip point 25mV and MOS Turn off.

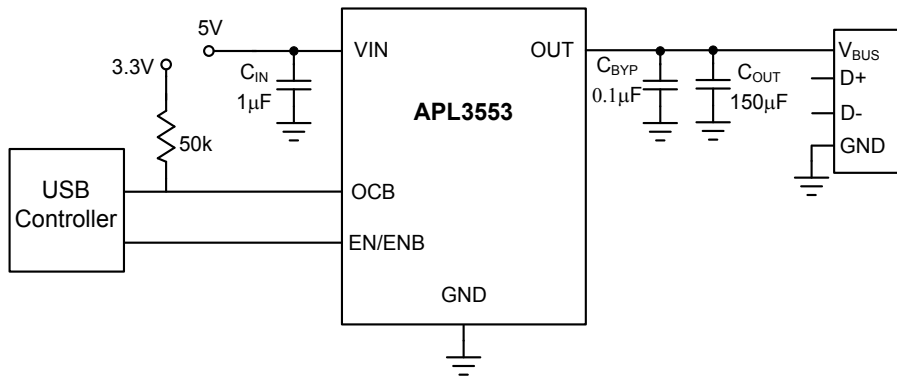
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Typical Application Circuit

Circuit 1.



Circuit 2.



Note: The C_{IN} is typically $1\mu F$. However, the parasitic inductance before VIN pin could cause voltage spike to damage internal circuitry. If voltage spike, especially during short circuit or hot plug-in of large capacitance load, on VIN exceeds VIN's absolute maximum rating, adding at least $10\mu F$ /MLCC capacitor at VIN is strongly recommended.

Function Description

VIN Under-Voltage Lockout (UVLO)

The APL3553I/J series of power switches have a built-in under-voltage lockout circuit to keep the output shutting off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current-Limit Protection

The APL3553I/J series of power switches provide the current-limit protection function. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period.

Short-Circuit Protection

When the output voltage drops below $V_{IN}-1V$, which is caused by an over-load or a short-circuit, the devices limit the output current down to a safe level. The short-circuit current limit is used to reduce the power dissipation during short-circuit conditions. If the junction temperature reaches over-temperature threshold, the device will enter the thermal shutdown.

OCB Output

The APL3553I/J series of power switches provide an open-drain output to indicate that a fault has occurred. When any of current-limit or over-temperature protection occurs for a deglitch time of $t_{D(OCB)}$, the OCB goes low. If fault condition release, OCB will goes high when $V_{OUT} > 1.5V$ (see Figure 1). Since the OCB pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Disable

Pull the ENB above 1.4V or EN below 0.6V will disable the device, and pull ENB pin below 0.6V or EN above 1.4V will enable the device. When the IC is disabled, the supply current is reduced to less than $1\mu A$. The enable input is compatible with both TTL and CMOS logic levels. The EN/ENB pin cannot be left floating.

Over-Temperature Protection

When the junction temperature exceeds $140^{\circ}C$, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by $20^{\circ}C$, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed $T_J=+125^{\circ}C$.

Reverse-Voltage Protection

The reverse voltage protection feature turns off the Nchannel MOSFET when a reverse current of $(V_{OUT} - V_{IN})/R_{DS(on)}$ over 100mA(typ.) for 5ms (typ) deglitch time(see Figure 2). The APL3553I/J device allows theN-channel MOSFET immediately turn on once the output voltage goes lower than the input voltage by 25 mV (typ) (see Figure 2). This prevents damage to devices on the input side of the APL3553I/J by preventing significant current from sinking into the input capacitance.

Application Information

Input Capacitor

10 μ F or higher ceramic bypass capacitor from VIN to GND, located near the APL3553I/J, is strongly recommended to suppress the ringing during short circuit fault event.

When the load current trips the SCP threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause VIN ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry.

Input capacitor is especially important to prevent V_{IN} from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

Output Capacitor

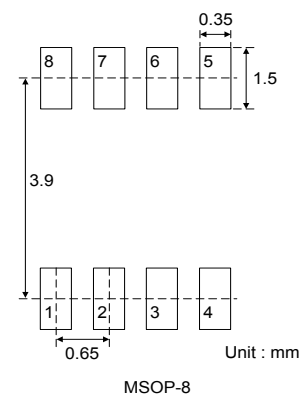
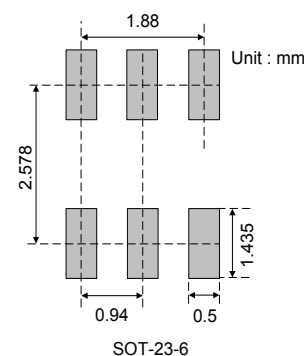
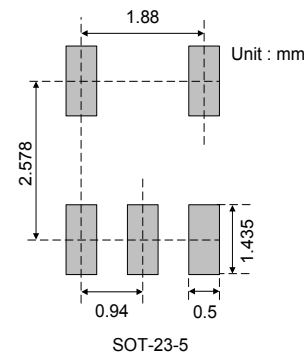
A low-ESR 150 μ F aluminum electrolytic between OUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1 μ F ceramic capacitor improves the immunity of the device to short-circuit transients.

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

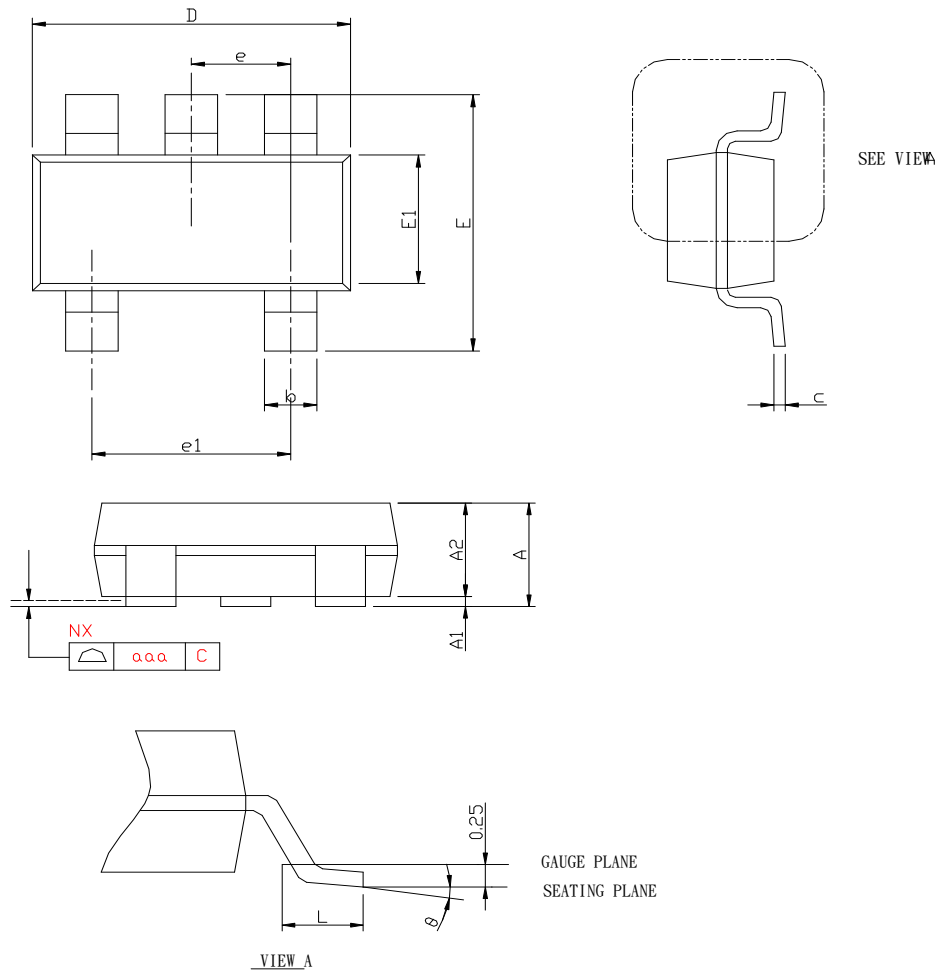
1. Please place the input capacitors near the IN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3553I/J and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep IN and OUT traces as wide and short as possible.
6. The traces routing the R_{ILIM} resistor to the APL3553I/J should be as short as possible to reduce parasitic effects on the current limit accuracy.

Recommended Minimum Footprint



Package Information

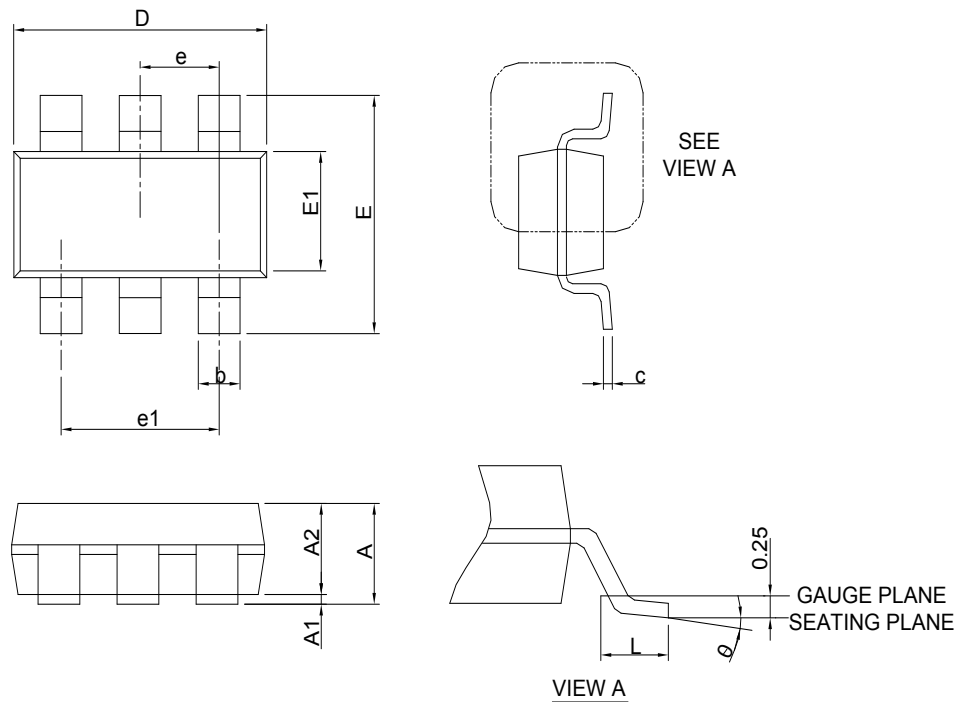
SOT-23-5



SYMBOL	SOT-23-5					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP	MAX.
A	1.00	1.16	1.45	0.039	0.046	0.057
A1	0.00	0.05	0.15	0.000	0.002	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.38	0.50	0.012	0.015	0.020
c	0.08	0.17	0.22	0.003	0.007	0.009
D	2.70	2.93	3.10	0.106	0.115	0.122
E	2.60	2.83	3.00	0.102	0.111	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0°	4°	8°	0°	4°	8°
aaa	0.10			0.004		

Package Information

SOT-23-6



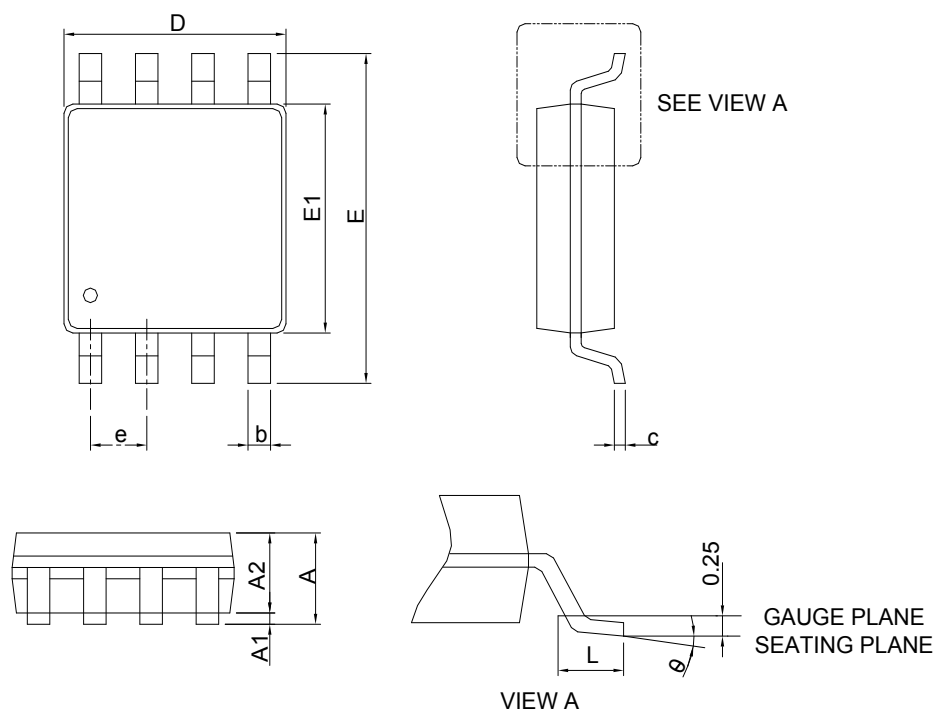
SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

MSOP-8



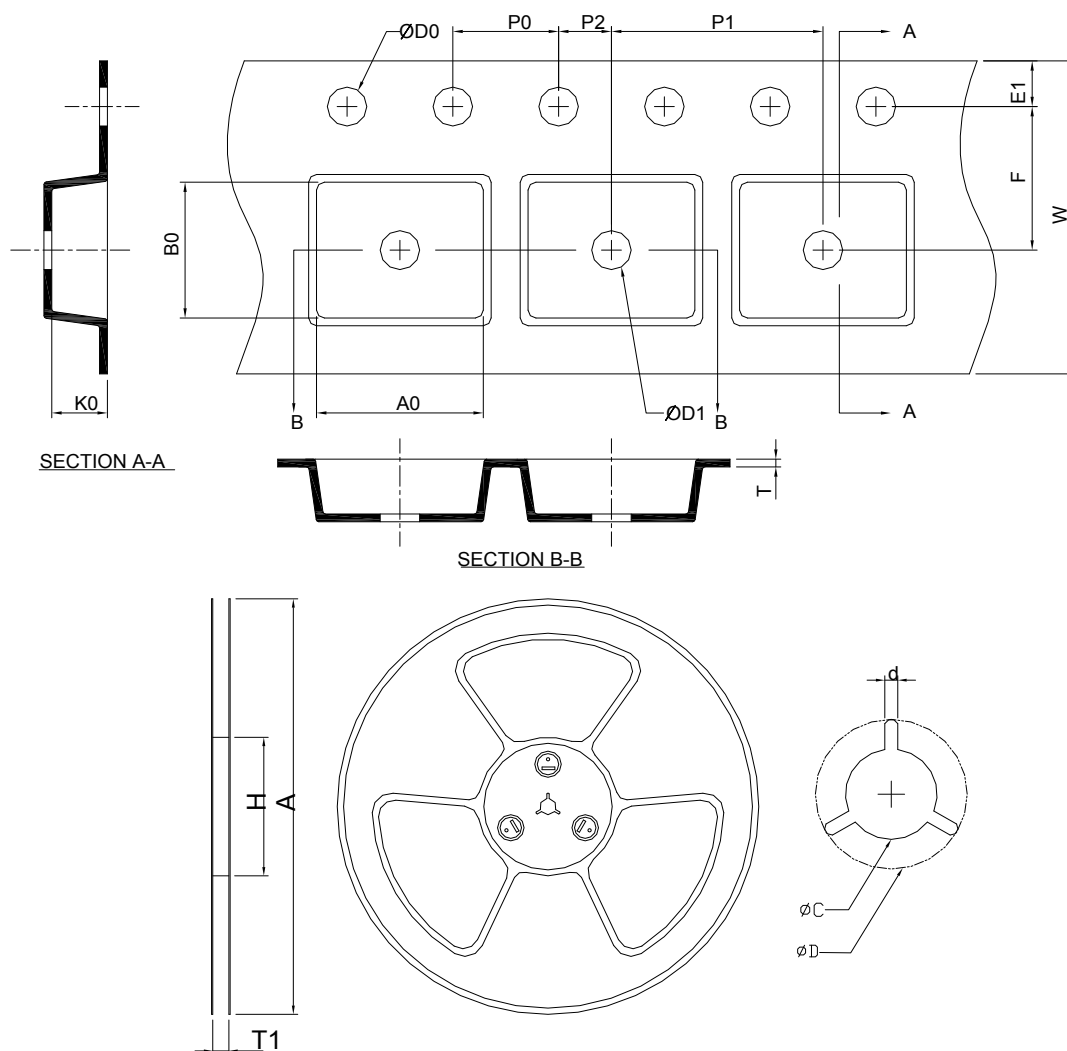
SYMBOL	MSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 5 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	A	H	T1	C	d	D	W	E1	F
MSOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20

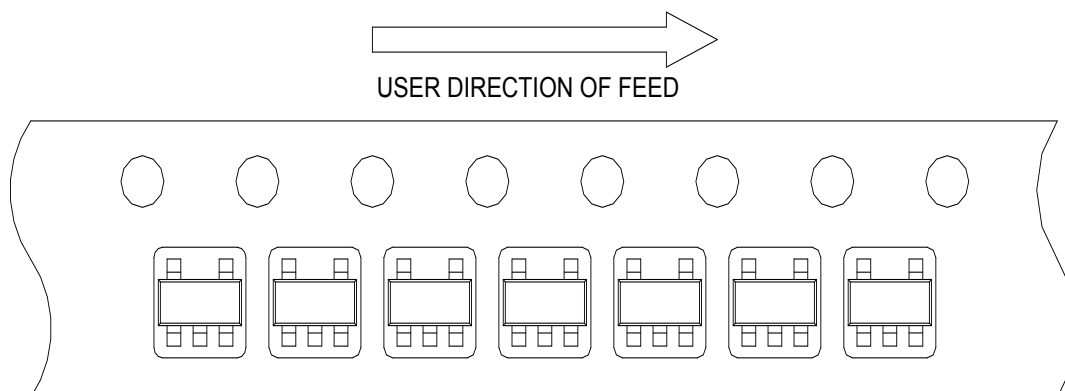
(mm)

Devices Per Unit

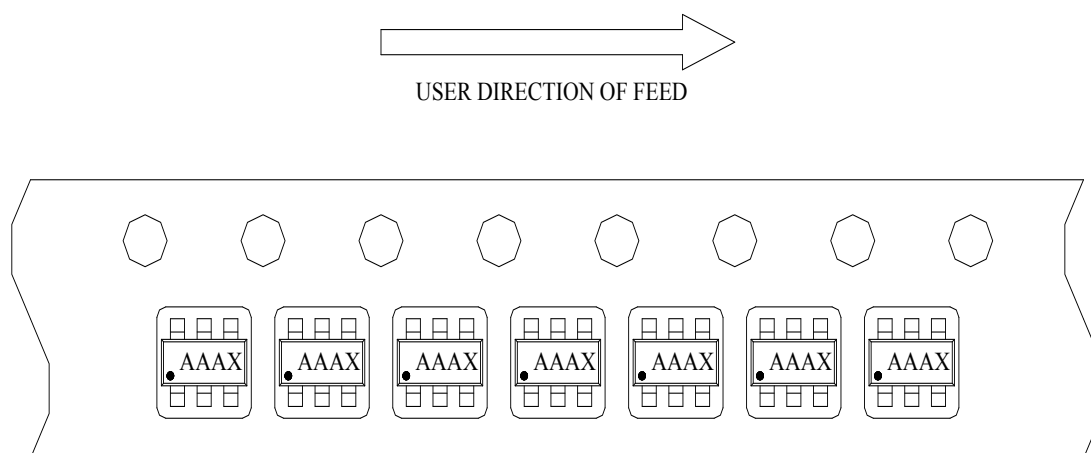
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SOT-23-6	Tape & Reel	3000
MSOP-8	Tape & Reel	3000

Taping Direction Information

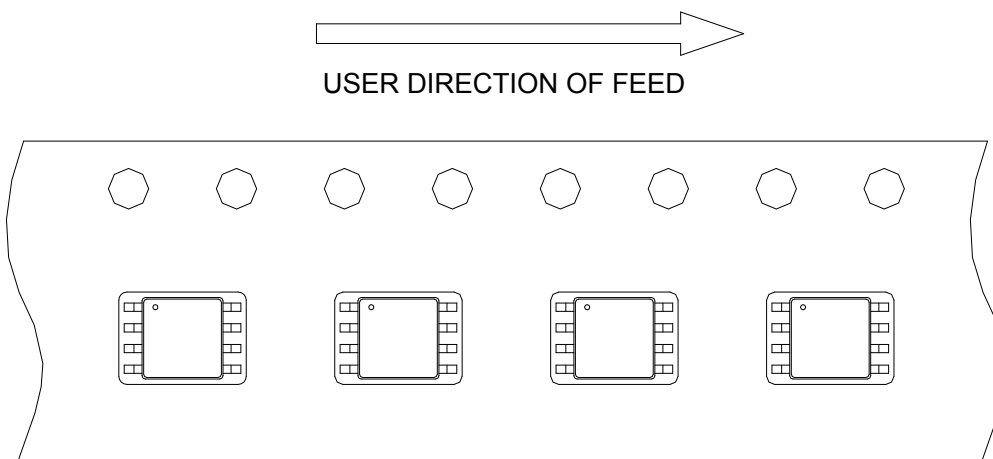
SOT-23-5



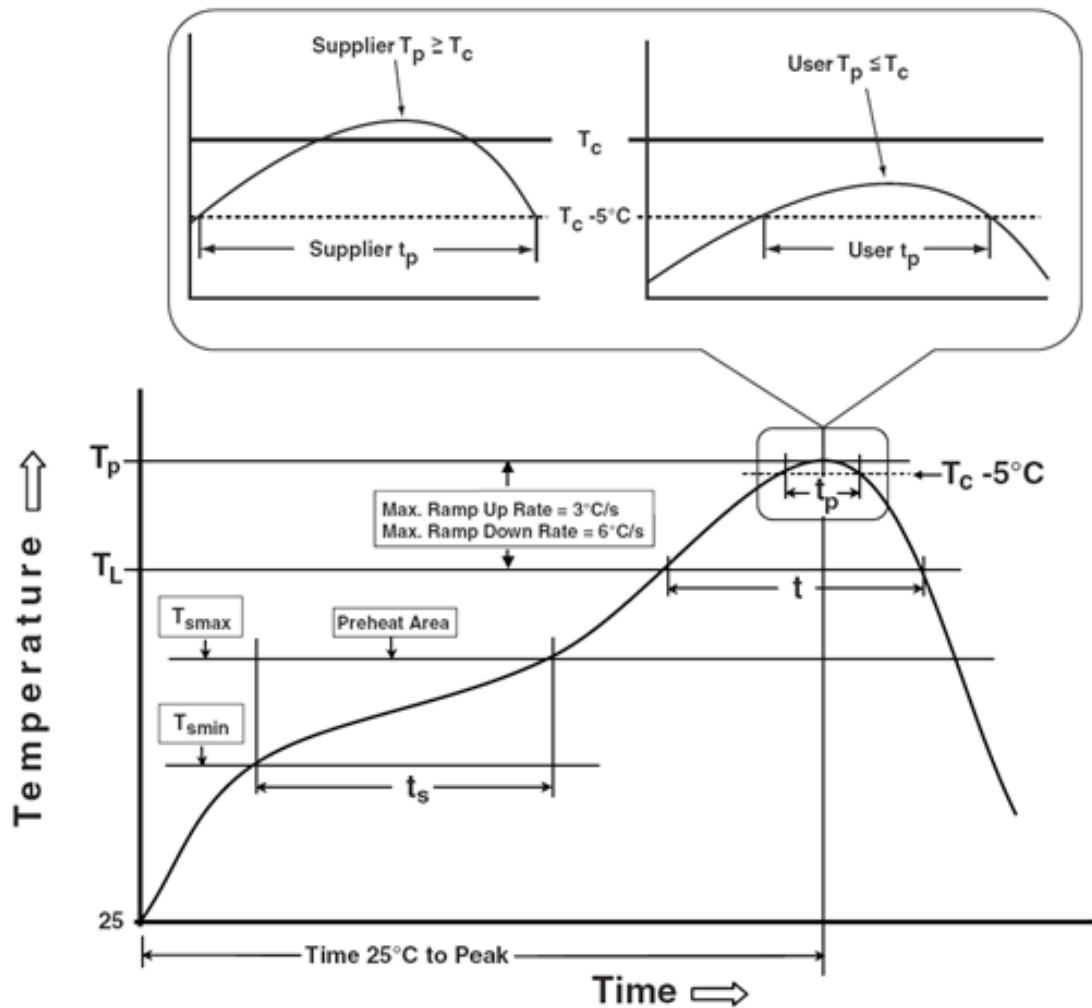
SOT-23-6



MSOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ >350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, I_{tr} ≥ 100mA

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