

3A, Ultra Low Dropout (0.23V Typical) Linear Regulator

Features

- **Ultra Low Dropout**
- 0.23V (typical) at 3A Output Current
- **Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable**
- **0.8V Reference Voltage**
- **High Output Accuracy**
- $\pm 1.5\%$ over Line, Load, and Temperature Range
- **Fast Transient Response**
- **Adjustable Output Voltage**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Current-Limit and Short Current-Limit Protections**
- **Thermal Shutdown with Hysteresis**
- **Open-Drain VOUT Voltage Indicator (POK)**
- **Low Shutdown Quiescent Current**
- **Shutdown/Enable Control Function**
- **Simple SOP-8P and TDFN3x3-10 Packages with Exposed Pad**

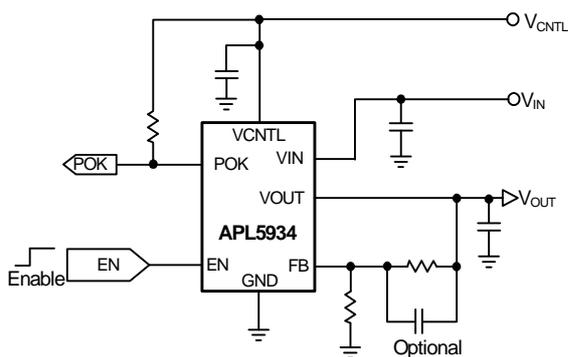
General Description

The APL5934 is a 3A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (V_{CNTL}) for the control circuitry, the other is a main supply voltage (V_{IN}) for power conversion, to reduce power dissipation and provide extremely low dropout voltage.

The APL5934/B integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5934/B can be enabled by other power systems. Pulling and holding the EN/ENB voltage below 0.4V shut/enable off the output.

The APL5934 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

Simplified Application Circuit

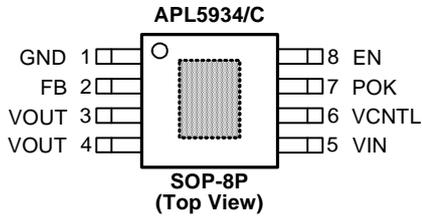


Applications

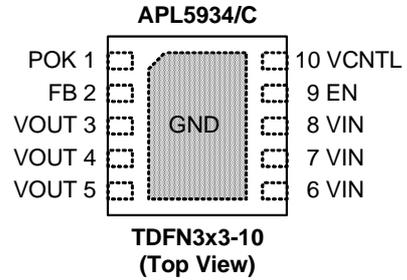
- **Front Side Bus VTT (1.2V/3A)**
- **Note Book PC Applications**
- **Motherboard Applications**

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

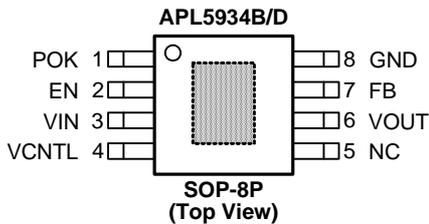
Pin Configuration



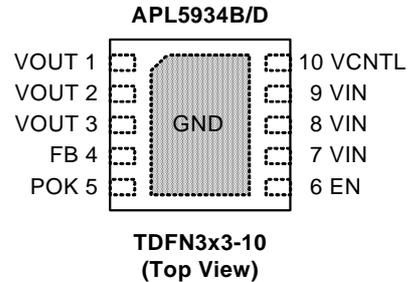
 = Exposed Pad
(connected to VIN or ground plane for better heat dissipation)



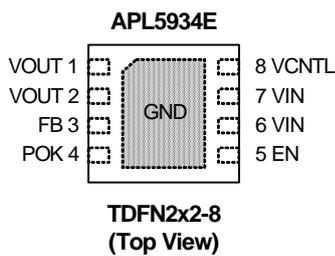
 = Exposed Pad
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(connected to ground plane for better heat dissipation)

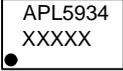


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(connected to ground plane for better heat dissipation)



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Ordering and Marking Information

<p>APL5934</p> <p> □□□□-□□□□ └─ EN Function └─ Package Code └─ Temperature Range └─ Handling Code └─ Assembly Material </p>	<p>Product Code (Enable Function) Blank : Avtive High/Initial On B : Active High / Intitial On C : Active High/Initial Off D : Active High / Initial Off E: Active High / Initial Off Package Code KA : SOP-8P QB : TDFN3x3-10 QB : TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G: Halogen and Lead Free Device</p>
<p>APL5934 KA:  XXXXX - Date Code</p>	<p>APL5934 QB:  XXXXX - Date Code</p>
<p>APL5934B KA:  XXXXX - Date Code</p>	<p>APL5934B QB:  XXXXX - Date Code</p>
<p>APL5934C KA:  XXXXX - Date Code</p>	<p>APL5934C QB:  XXXXX - Date Code</p>
<p>APL5934D KA:  XXXXX - Date Code</p>	<p>APL5934D QB:  XXXXX - Date Code</p>
<p>APL5934E QB:  X - Date Code</p>	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6	V
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ $V_{IN} + 0.3$	V
	POK to GND Voltage	-0.3 ~ 6	V
	EN, FB to GND Voltage	-0.3 ~ $V_{CNTL} + 0.3$	V
P_D	Power Dissipation, $T_A=25^{\circ}C$	for SOP-8P/TDFN3x3-10	1.8
		for TDFN2x2-8	1.2
$I_{OUT(PK)}$	VOUT Peak Current (< 30 μ s)	9	A
T_J	Maximum Junction Temperature	150	$^{\circ}C$
T_{STG}	Storage Temperature	-65 ~ 150	$^{\circ}C$
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	$^{\circ}C$
V_{ESD}	(CDM Model) JESD22-C101F	± 1	kV

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air <small>(Note 2)</small>	SOP-8P	50
		TDFN3x3-10	50
		TDFN2x2-8	75
θ_{JC}	Junction-to-Case Resistance in Free Air <small>(Note 2)</small>	SOP-8P	8
		TDFN3x3-10	8
		TDFN2x2-8	13

Note 2: θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P/ TDFN3x3-10/TDFN2x2-8 is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage	3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage	1.2 ~ 5.5	V
V_{OUT}	VOUT Output Voltage (when $V_{CNTL} - V_{OUT} > 1.2V$)	0.8 ~ $V_{IN} - V_{DROP}$	V
I_{OUT}	VOUT Output Current	Continuous Current	0 ~ 3
		Peak Current	0 ~ 4
C_{OUT}	VOUT Output Capacitance	$I_{OUT}=3A$ at 25% nominal V_{OUT}	8 ~ 1100
		$I_{OUT}=2A$ at 25% nominal V_{OUT}	8 ~ 1700
		$I_{OUT}=1A$ at 25% nominal V_{OUT}	8 ~ 2400
ESR_{COUT}	ESR of VOUT Output Capacitor	0 ~ 200	m Ω
T_A	Ambient Temperature	-40 ~ 85	$^{\circ}C$
T_J	Junction Temperature	-40 ~ 125	$^{\circ}C$

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{CNTL}=5V$, $V_{IN}=1.8V$, $V_{OUT}=1.2V$ and $T_A = -40 \sim 85^\circ C$. Typical values are at $T_A=25^\circ C$.

Symbol	Parameter	Test Conditions	APL5934			Unit		
			Min.	Typ.	Max.			
SUPPLY CURRENT								
I_{VCNTL}	VCNTL Supply Current	EN = High or ENB=Low, $I_{OUT}=0A$	-	100	120	μA		
I_{SD}	VCNTL Supply Current at Shutdown	EN = Low, or ENB=High	-	-	3	μA		
	VIN Supply Current at Shutdown	EN = Low, or ENB=High	-	-	1	μA		
POWER-ON-RESET (POR)								
	Rising VCNTL POR Threshold		2.5	2.7	2.9	V		
	VCNTL POR Hysteresis		-	0.4	-	V		
	Rising VIN POR Threshold		0.8	0.9	1.0	V		
	VIN POR Hysteresis		-	0.5	-	V		
OUTPUT VOLTAGE								
V_{REF}	Reference Voltage	FB=VOUT	-	0.8	-	V		
	Output Voltage Accuracy	$V_{CNTL}=3.0 \sim 5.5V$, $I_{OUT}=0 \sim 3A$, $T_J = -40 \sim 125^\circ C$	-1.5	-	+1.5	%		
	Load Regulation	$I_{OUT}=0A \sim 3A$	-	0.06	0.25	%		
	Line Regulation	$I_{OUT}=10mA$, $V_{CNTL}=3.0 \sim 5.5V$	-0.15	-	+0.15	%/V		
	VOUT Pull-low Resistance	$V_{CNTL}=5V$, $V_{EN}=0V$, $V_{OUT} < 0.8V$	-	85	-	Ω		
	FB Input Current	$V_{FB}=0.8V$	-100	-	100	nA		
DROPOUT VOLTAGE								
V_{DROD}	VIN-to-VOUT Dropout Voltage	$V_{CNTL}=5.0V$, $I_{OUT}=3A$	$V_{OUT}=2.5V$	$T_J=25^\circ C$	-	0.26	0.31	V
				$T_J = -40 \sim 125^\circ C$	-	-	0.42	
			$V_{OUT}=1.8V$	$T_J=25^\circ C$	-	0.24	0.29	
				$T_J = -40 \sim 125^\circ C$	-	-	0.40	
			$V_{OUT}=1.2V$	$T_J=25^\circ C$	-	0.23	0.28	
				$T_J = -40 \sim 125^\circ C$	-	-	0.38	
I_{LIM}	Current-Limit Level		$T_J=25^\circ C$	4.7	5.7	6.7	A	
			$T_J = -40 \sim 125^\circ C$	4.2	-	-		
PROTECTIONS								
I_{SHORT}	Short Current-Limit Level	$V_{FB} < 0.2V$	-	1.1	-	A		
	Short Current-Limit Blanking Time	From beginning of soft-start	0.6	1.5	-	ms		
T_{SD}	Thermal Shutdown Temperature	T_J rising	145	150	-	$^\circ C$		
	Thermal Shutdown Hysteresis		-	50	-	$^\circ C$		

Electrical Characteristics (Cont.)

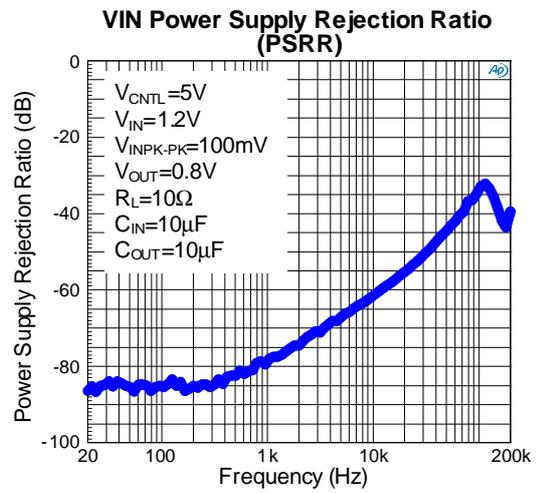
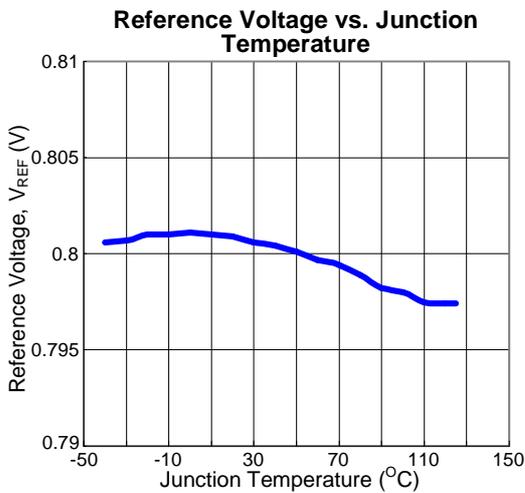
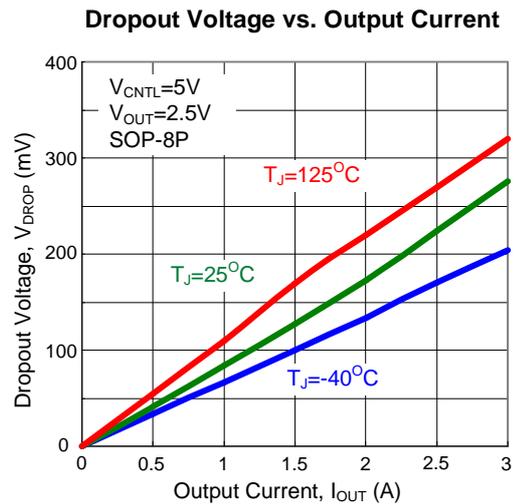
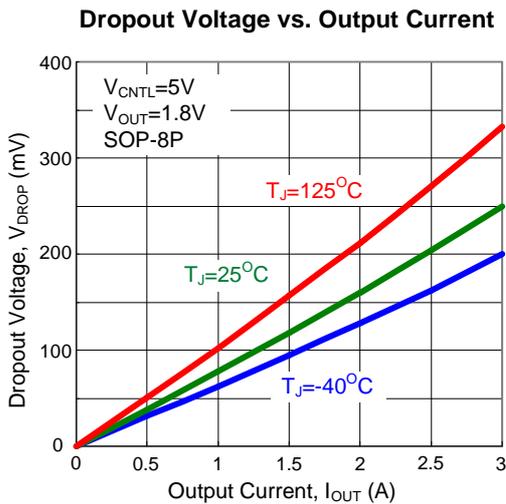
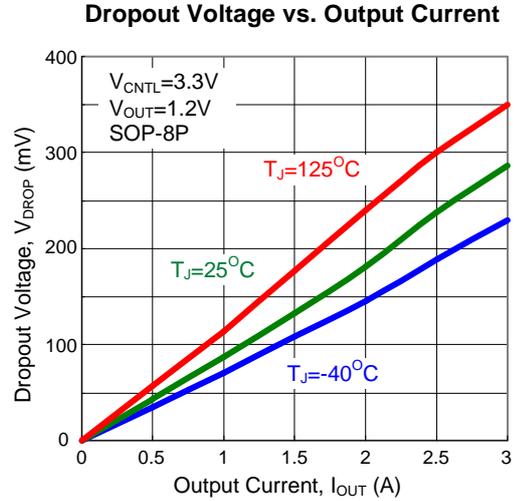
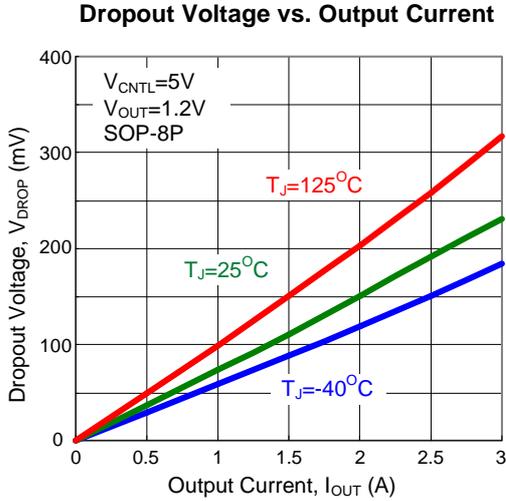
Unless otherwise specified, these specifications apply over $V_{\text{CNTL}}=5\text{V}$, $V_{\text{IN}}=1.8\text{V}$, $V_{\text{OUT}}=1.2\text{V}$ and $T_{\text{A}}= -40 \sim 85^{\circ}\text{C}$. Typical values are at $T_{\text{A}}=25^{\circ}\text{C}$.

Symbol	Parameter	Test Conditions	APL5934			Unit
			Min.	Typ.	Max.	
ENABLE AND SOFT-START						
$V_{\text{EN}}/V_{\text{ENB}}$	EN Logic High Threshold Voltage	V_{EN} rising or V_{ENB} rising	0.5	0.8	1.1	V
	ENB Logic Low Threshold Voltage					
	EN/ENB Hysteresis		-	0.1	-	V
	EN/ENB Pull-High Current	EN=GND or ENB=GND	-	3	-	μA
	EN/ENB Pull-Low Current	EN=VCNTL or ENB=VCNTL				
t_{SS}	Soft-Start Interval	$V_{\text{OUT}}=10\%$ to 90% (APL5934/B/C)	0.3	0.6	0.9	ms
		$V_{\text{OUT}}=10\%$ to 90% (APL5934D/E)	1	2	3	
t_{ON}	Turn On Delay	From being enabled to V_{OUT} rising 10% (APL5934/C)	60	120	230	μs
		From being enabled to V_{OUT} rising 10% (APL5934B/D/E)	1	2.5	4	ms
POWER-OK AND DELAY						
V_{THPOK}	Rising POK Threshold Voltage	V_{FB} rising	90	92	94	%
	POK Threshold Hysteresis		-	8	-	%
	POK Pull-low Voltage	POK sinks 5mA	-	0.25	0.4	V
	POK Debounce Interval	$V_{\text{FB}} <$ falling POK voltage threshold	-	10	-	μs
	POK Delay Time	From $V_{\text{FB}}=V_{\text{THPOK}}$ to rising edge of the V_{POK}	1	2	3	ms

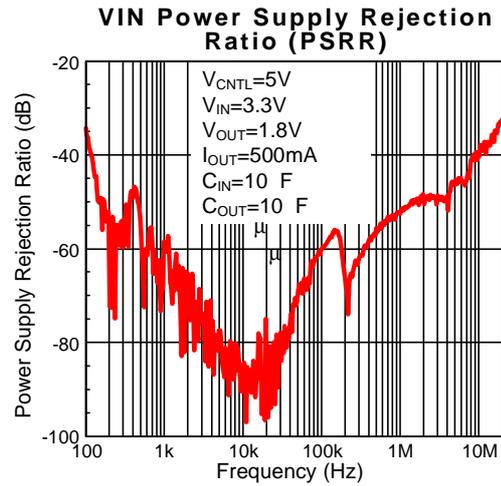
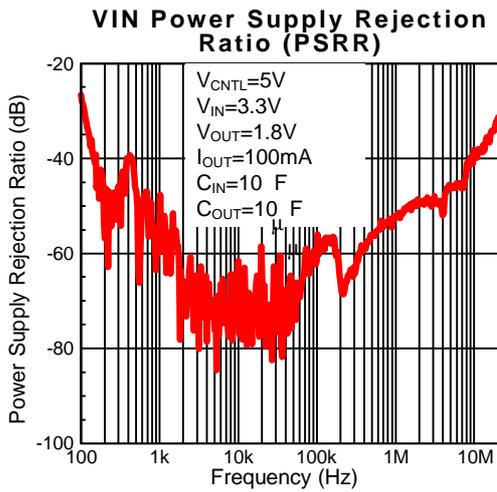
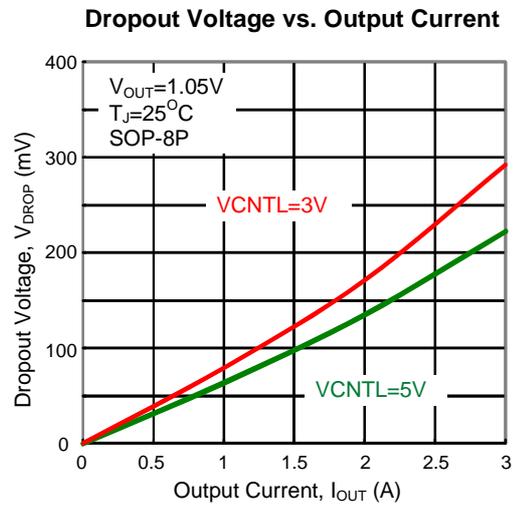
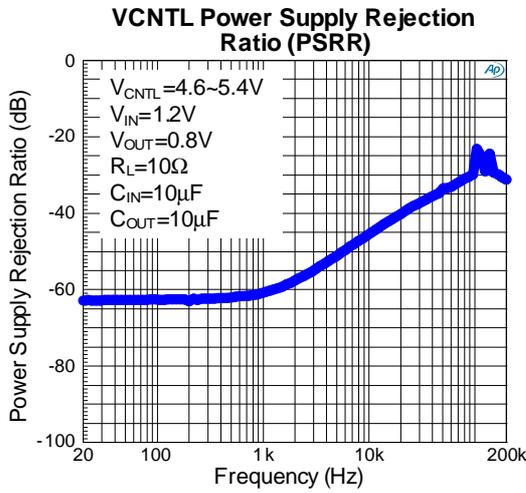
Pin Description

PIN					NAME	FUNCTION
NO.						
SOP-8P		TDFN3x3-10		TDFN2x2-8		
APL5934B/D	APL5934/C	APL5934B/D	APL5934/C	APL5934E		
8	1	-	-	-	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
7	2	4	2	3	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.
6	3,4	1,2,3	3,4,5	1,2	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10 μ F at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 3A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
3	5	7,8,9	6,7,8	6,7	VIN	Main supply input pin for voltage conversions. A decoupling capacitor ($\geq 10\mu$ F recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose.
4	6	10	10	8	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (0.1 μ F typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
1	7	5	1	4	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	8	6	9	5	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When leave this pin open, an internal pull-up/low current (3 μ A typical) pulls the EN voltage and enables/shuts down the regulator.
5	-	-	-	-	NC	No Connection.
Exposed Pad	-	Exposed Pad	Exposed Pad	Exposed Pad	GND	Ground pin of the circuitry. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.
-	Exposed Pad	-	-	-	-	Connect this pad to system VIN or ground plane for good thermal conductivity.

Typical Operating Characteristics

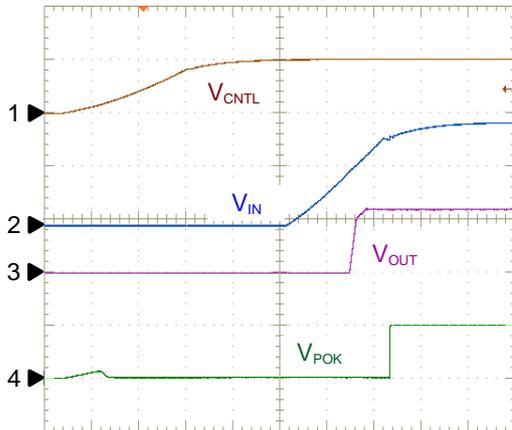


Typical Operating Characteristics (Cont.)



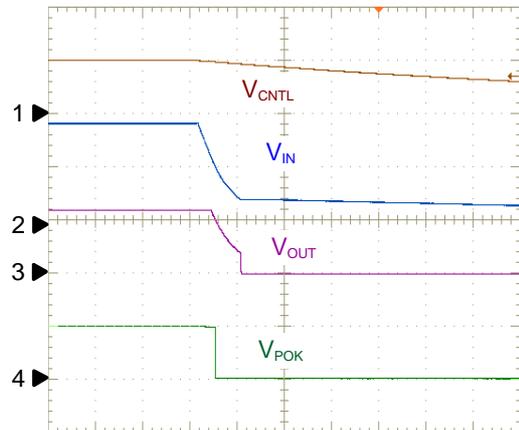
Operating Waveforms

Power On



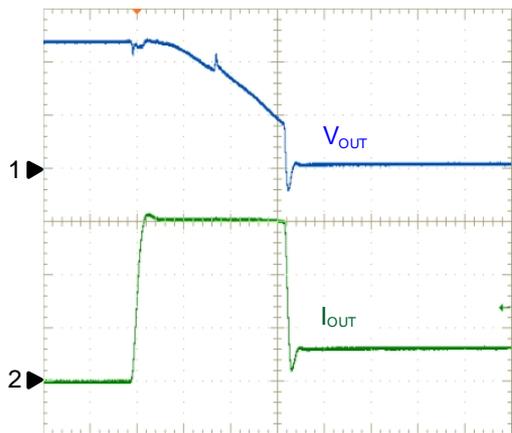
$C_{OUT}=10\mu F, C_{IN}=10\mu F$
 CH1: V_{CNTL} , 5V/Div, DC
 CH2: V_{IN} , 1V/Div, DC
 CH3: V_{OUT} , 1V/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 4ms/Div

Power Off



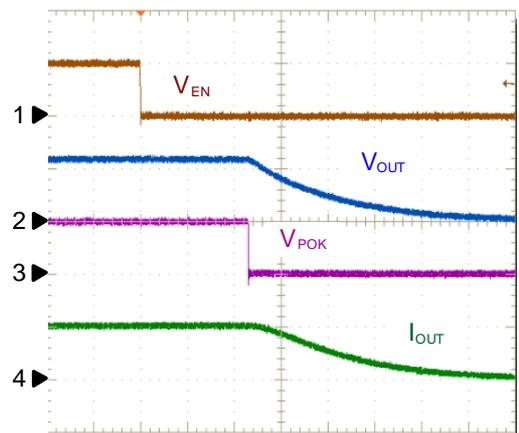
$C_{OUT}=10\mu F, C_{IN}=10\mu F$
 CH1: V_{CNTL} , 5V/Div, DC
 CH2: V_{IN} , 1V/Div, DC
 CH3: V_{OUT} , 1V/Div, DC
 CH4: V_{POK} , 5V/Div, DC
 TIME: 40ms/Div

Over Current Protection



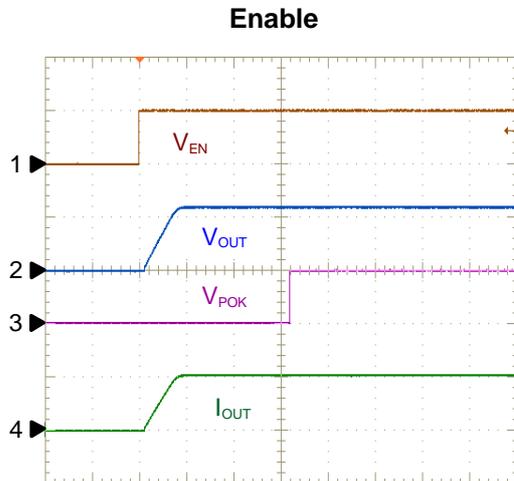
$C_{OUT}=10\mu F, C_{IN}=10\mu F$
 CH1: V_{OUT} , 500mV/Div, DC
 CH2: I_{OUT} , 2A/Div, DC
 TIME: 100μs/Div

Shutdown



$C_{OUT}=10\mu F, C_{IN}=10\mu F$
 CH1: V_{EN} , 5V/Div, DC
 CH2: V_{OUT} , 1V/Div, DC
 CH3: V_{POK} , 5V/Div, DC
 CH4: I_{OUT} , 2A/Div, DC
 TIME: 2μs/Div

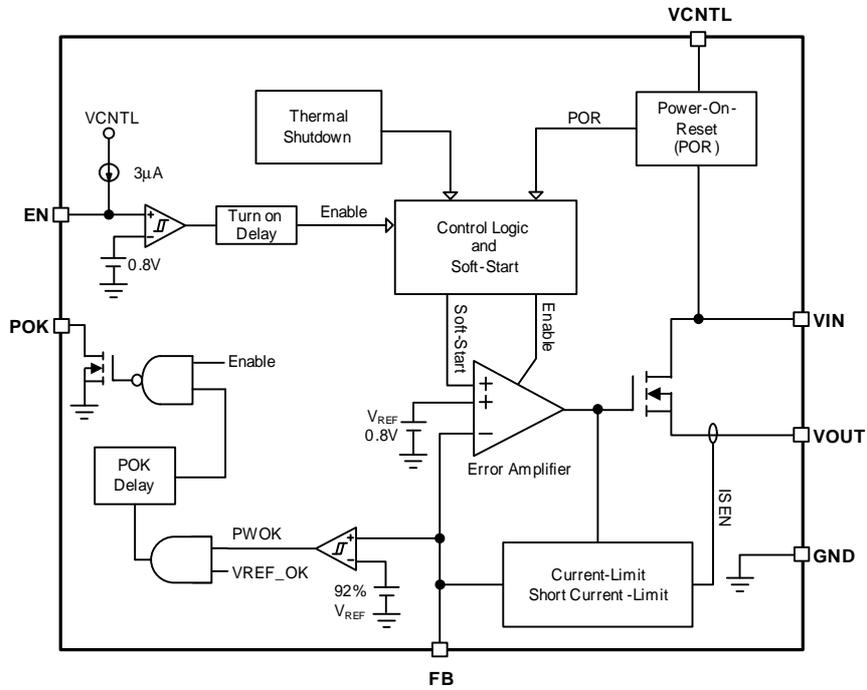
Operating Waveforms (Cont.)



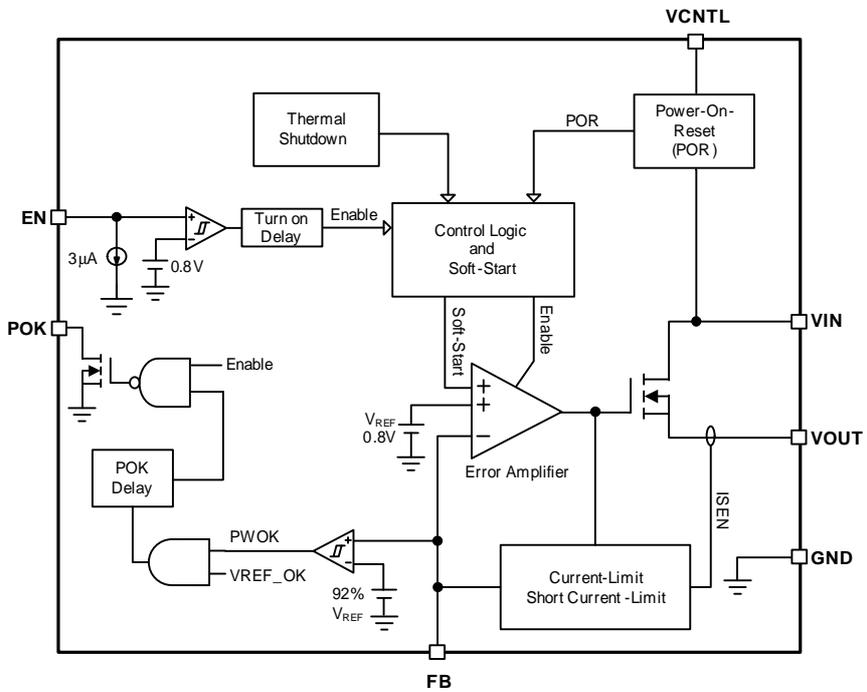
$C_{OUT}=10\mu F, C_{IN}=10\mu F$
 CH1: V_{EN}, 5V/Div, DC
 CH2: V_{OUT}, 1V/Div, DC
 CH3: V_{POK}, 5V/Div, DC
 CH4: I_{OUT}, 2A/Div, DC
 TIME: 1ms/Div

Block Diagram

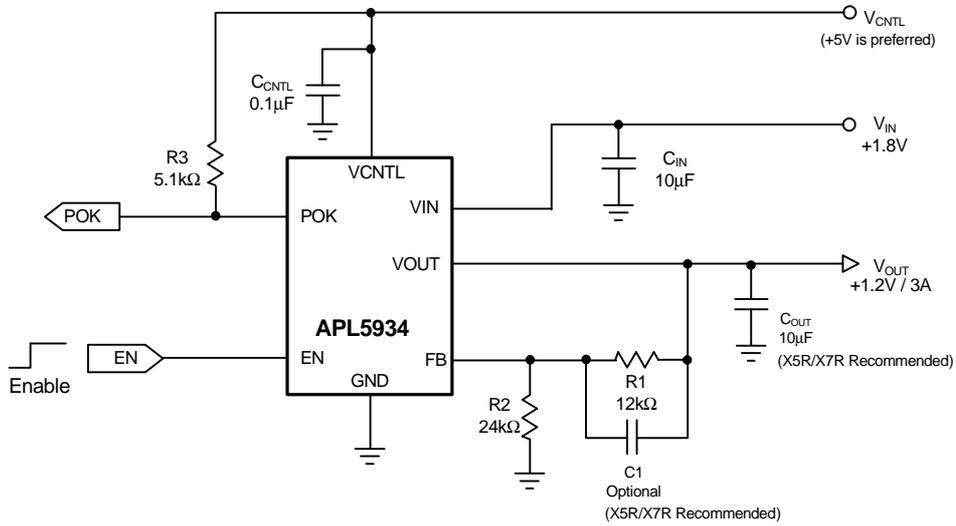
APL5934/B



APL5934C/D/E



Typical Application Circuit



10µF: GRM31MR60J106KE19 Murata

Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless the output status when one of the supply voltages falls below its falling POR voltage threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge during start-up. The typical soft-start interval is about 0.6 ms.

Output Voltage Regulation

An error amplifier works with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

Current-Limit Protection

The APL5934 monitors the current flowing through the output NMOS and limits the maximum current to prevent load and APL5934 from damages during current overload conditions.

Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 1.1A (typical) when the voltage on FB pin falls below 0.2V (typical) during current overload or short-circuit conditions.

The short current-limit function is disabled for successful start-up during soft-start interval.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5934. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start process after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 50°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

For normal operation, the device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Enable Control

The APL5934 has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up/low by an internal current source (3μA typical) to enable/shutdown normal operation. It's not necessary to use an external transistor to save cost.

Power-OK and Delay

The APL5934 indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK voltage threshold (V_{THPOK}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate that the output is ok. As the V_{FB} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 10μs typical).

Application Information

Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage.

Output Capacitor

The APL5934 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as output capacitors.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the APL5934 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

Input Capacitor

The APL5934 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance. Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10µF at least.

However, if the drop of the input voltage is not cared, the input capacitance can be less than 10µF. More capacitance reduces the variations of the supply voltage on VIN pin.

Setting Output Voltage

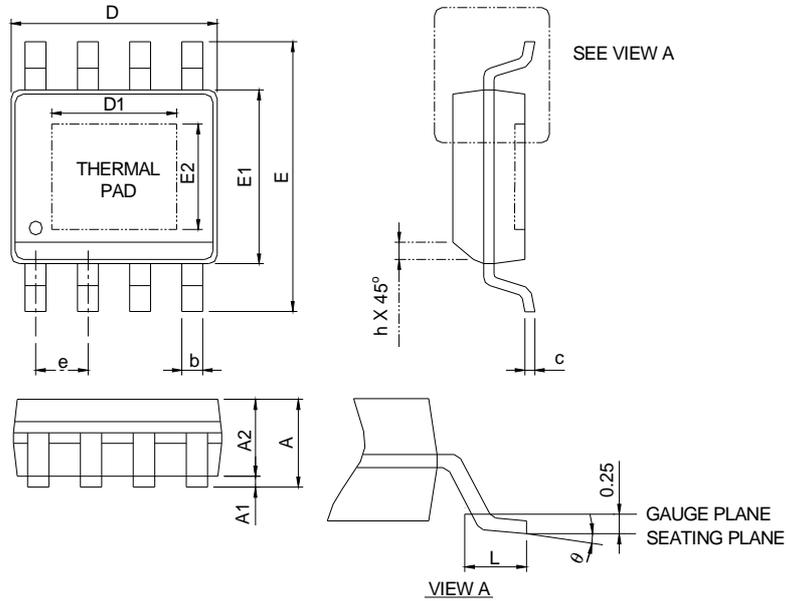
The output voltage is programmed by the resistor divider connected to FB pin. The preset output voltage is calculated by the following equation :

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2} \right) \dots\dots\dots (V)$$

Where R1 is the resistor connected from VOUT to FB with Kelvin sensing connection and R2 is the resistor connected from FB to GND. A bypass capacitor(C1) may be connected with R1 in parallel to improve load transient response and stability.

Package Information

SOP-8P

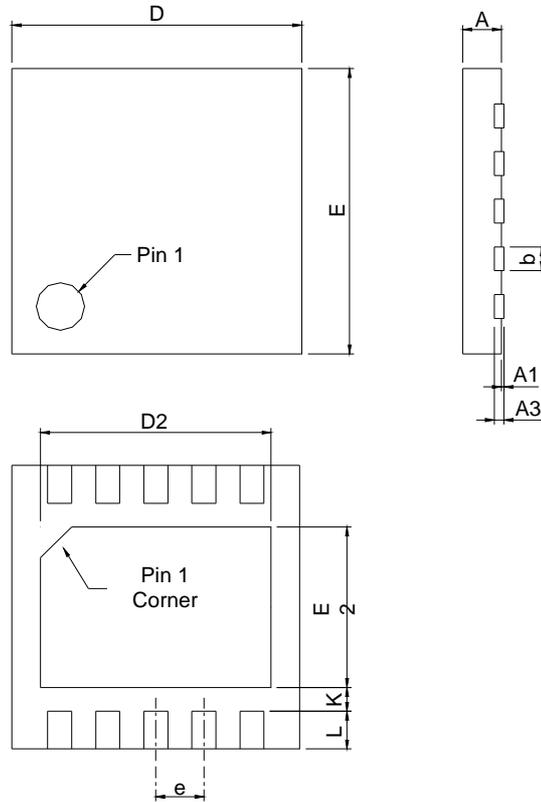


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.30	1.60	0.051	0.063
A1	0.00	0.10	0.000	0.006
A2	1.25	1.45	0.049	0.057
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
Q.Q.Q	0.10		0.004	

- Note: 1. Followed from JEDEC MS-012 BA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information (Cont.)

TDFN3x3-10

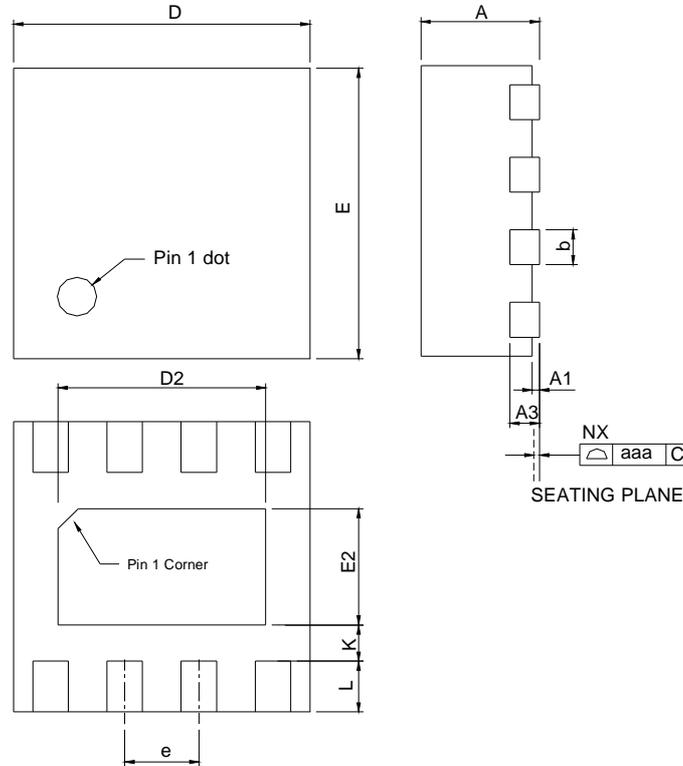


SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note: Followed from JEDEC MO-229 VEED-5.

Package Information (Cont.)

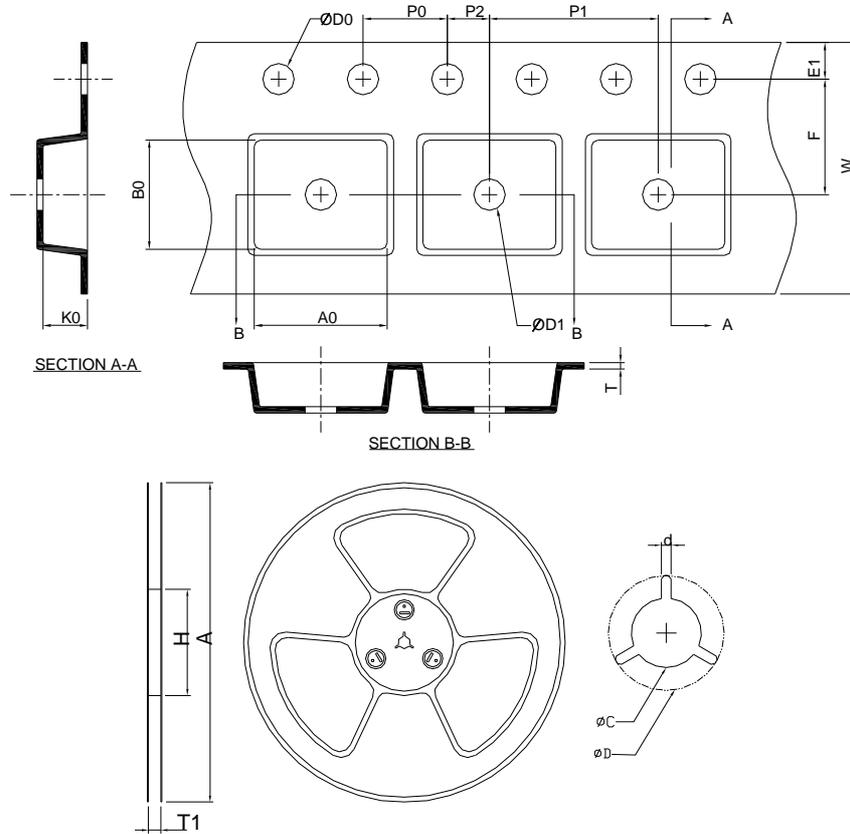
TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note: Followed from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN 3x3	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN 2x2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20

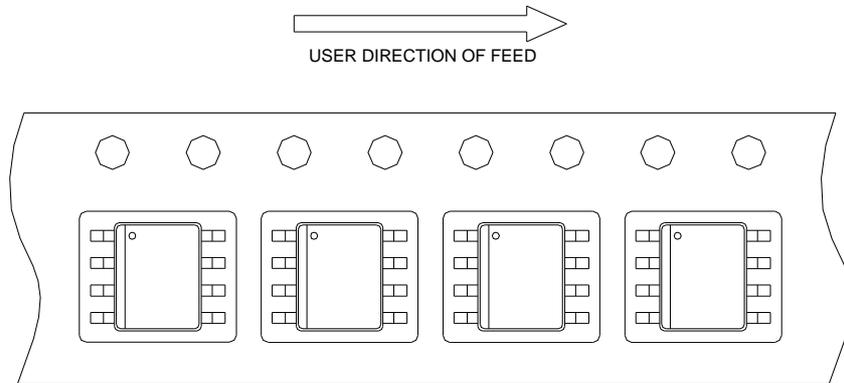
(mm)

Devices Per Unit

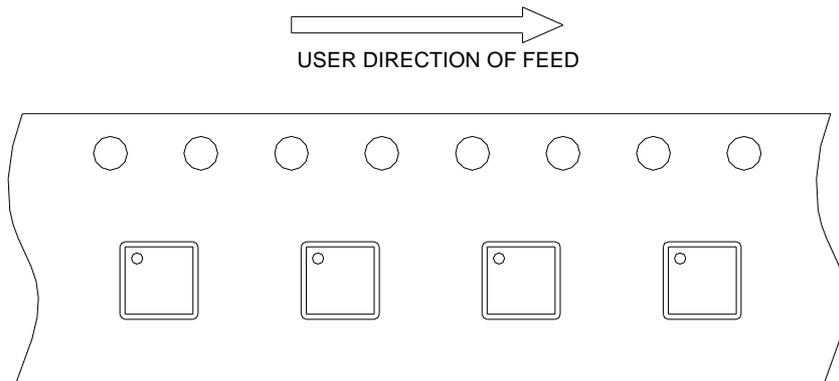
Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500
TDFN3x3	Tape & Reel	3000
TDFN2x2	Tape & Reel	3000

Taping Direction Information

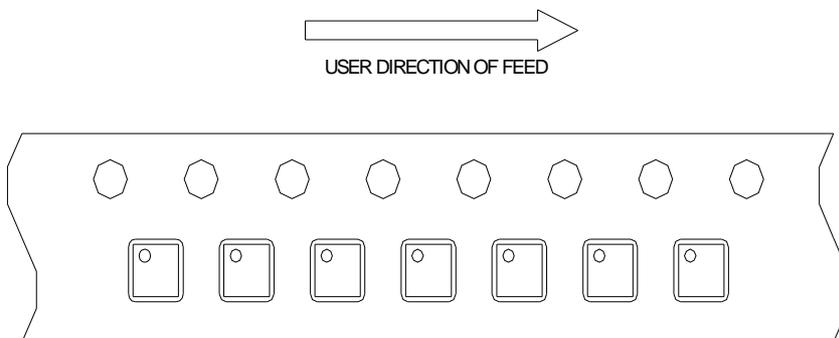
SOP-8P



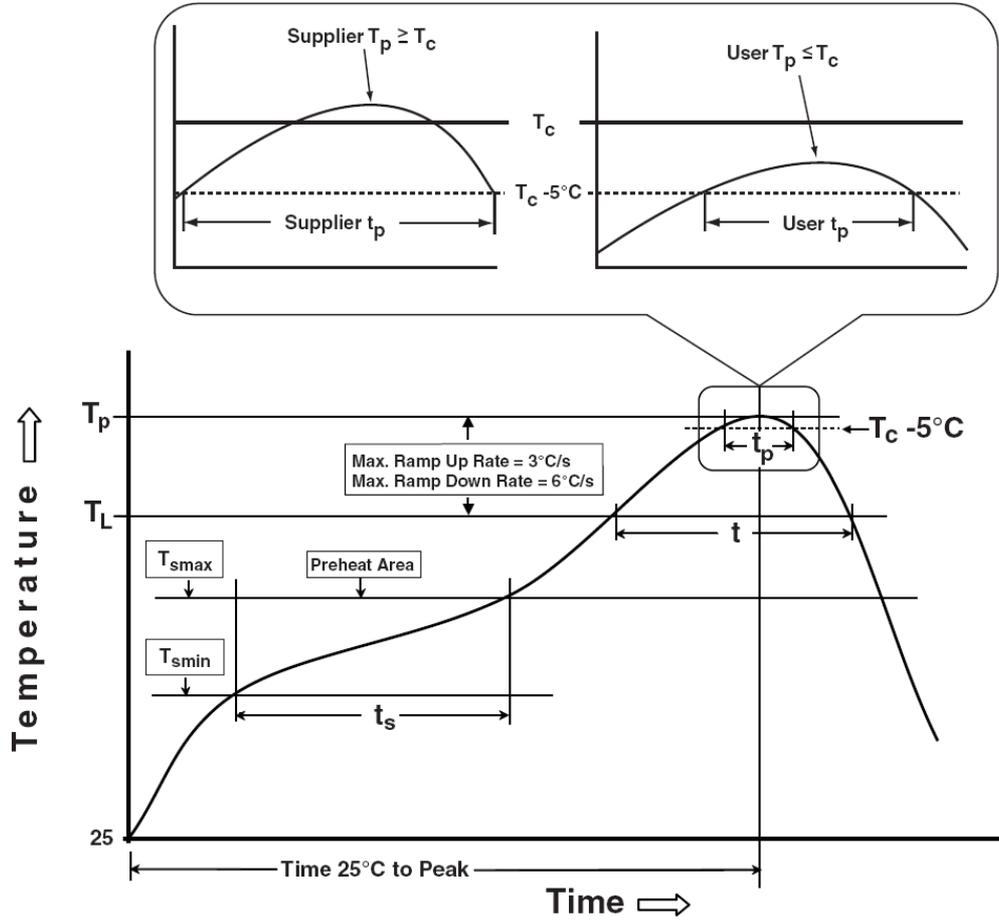
TDFN3x3-10



TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD-78	10ms, $I_{tr} \geq 100\text{mA}$

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