APW6016E

5 Buck Converters and 1 Termination LDO PMIC with I2C interface

Features

- **High Input Voltages Range from 4.5V to 16V**
- **Built in Input Voltage UVLO threshold**
- **Built in VIN OVP**
- **Programmable power sequence control by I2C for all channel**
- **Provide 5 Single-Buck PWM Converter and 1 Termination LDO Regulator**
- **Channel 1 Synchronous Buck for VCORE**
- **(Default 1V)**
  - 0.4V ~ 1.975V programmable with 25mV step
  - 1.5A output current capability
  - 750KHz / 1.5MHz switching frequency
- **Channel 2 Synchronous Buck for Memory**
  (Default 1.2V)
  - 0.4V ~ 1.975V programmable with 25mV step
  - 1.5A output current capability
  - 750KHz / 1.5MHz switching frequency
- **Channel 3 Synchronous Buck for I/O**
  (Default 1.8V)
  - 0.8V ~ 3.95V programmable with 50mV step
  - 1.0A output current capability
  - 750KHz / 1.5MHz switching frequency
- **Channel 4 Synchronous Buck for I/O**
  (Default 2.5V)
  - 0.8V ~ 3.95V programmable with 50mV step
  - 1.0A output current capability
  - 750KHz / 1.5MHz switching frequency
- **Channel 5 Synchronous Buck for I/O**
  (Default 3.3V)
  - 0.8V ~ 3.95V programmable with 50mV step
  - 1.0A output current capability
  - 750KHz / 1.5MHz switching frequency
- **Channel 6 VTT Termination LDO Regulator**
  - 0.5A output current capability
- **Built-in EN function**
- **Built-in RST to monitor output voltage status**
- **Built-in Current Limit/SCP/OVP/OTP**
- **VTQFN-32 4mmx4mm Thin package**
- **Lead Free Available (RoHS Compliant)**

General Description

The APW6016E is designed for server management processor power system, which integrates 5 buck converters and one 0.5A sink/source VTT LDO into one single package. The PWM converters and VTT LDO output voltage can support VCORE, memory, memory bus termination and 1.8V/2.5V/3.3V I/O. Each VR voltage are programmable with high resolution via I2C interface. Moreover, the power-on and power-off sequences as well as soft-start time of these VR are controlled and programmable via I2C interface, providing versatility for system designers.

The APW6016E provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Modulation mode (PFM), the APW6016E provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. On VTQFN-32 Package, the Forced PWM Mode works nearly at constant frequency for low-noise requirements.

The APW6016E features sufficient protections against over-current, over-voltage, short circuit and over temperature to prevent catastrophic failure. A Power-On- Reset function monitors the voltage on SVIN prevents wrong operation during power on.

The output voltage of VTT automatically tracks the voltage of half V_{OUT2}. The VTT output voltage is only requiring 10μF of ceramic output capacitance for stability and fast transient response.

Applications

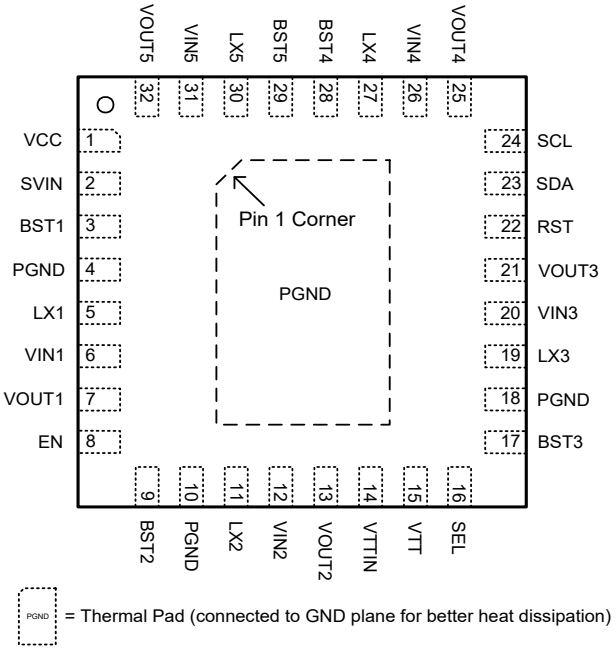
- **Server**

Ordering and Marking Information

APW6016E □□ – □□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF : VTQFN4x4-32 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device G : Halogen and Lead Free Device
APW6016E QF : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter		Rating	Unit
V_{INx}	Supply Voltages (VIN/SVIN/EN/RST to GND)		-0.3 ~ 18	V
V_{BSTX}	BOOT Supply Voltages (BST1/BST2/BST3/BST4/BST5 to LX)		-0.3 ~ 7	V
	Other Pins (VCC/SCL/SDA/VOUTx/VTT/VTTIN/SEL to GND)		-0.3 ~ 7	V
V_{LXX}	LX Voltages (LX1/LX2/LX3/LX4/LX5 to GND)	<100ns pulse width	-5 ~ 21	V
		>100ns pulse width	-0.3 ~ VIN+0.3	
T_j	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds		260	°C
V_{ESD}	Minimum ESD Rating	(Human Body Mode) (MM mode)	±2 0.2	kV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter	Range	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient	52	°C/W
θ_{JC}	Thermal Resistance - Junction to Case	7	°C/W

Note 3: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	4.5 ~ 16	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{SVIN}=12V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
SVIN SUPPLY CURRENT							
$I_{SVINSTB}$	SVIN Standby Current	T_A=25°C, LX not switching		-	600	-	μA
$I_{SVINSDN}$	SVIN Shutdown Current	T_A=25°C, EN=low		-	65	100	μA
SVIN POWER-ON-RESET AND OVER VOLTAGE PROTECTION							
V_{POR_R}	SVIN POR Rising Threshold	V_{SVIN} Rising, R_{SEL}=400kΩ		10.2	10.5	10.8	V
		V_{SVIN} Rising, R_{SEL}=200kΩ		4.0	4.2	4.4	V
V_{POR_F}	SVIN POR Falling Threshold	V_{SVIN} Falling, R_{SEL}=400kΩ		9.5	9.8	10.1	V
		V_{SVIN} Falling, R_{SEL}=200kΩ		3.8	4	4.2	V
	SVIN Pre-POR Rising Threshold (Note 4)	V_{SVIN} Rising, I2C active		-	2.75	-	V
	SVIN Pre-POR Rising Threshold Hysteresis (Note 4)	V_{SVIN} Falling		-	200	-	mV
V_{OVP_SVIN}	SVIN Over Voltage Threshold	V_{SVIN} Rising		-	18	-	V
		Hysteresis		-	1	-	V
VTT OUTPUT							
V_{VTT}	VTT Output Voltage	V_{OUT2}=1.2V		-	0.6	-	V
V_{VTT}	VTT Output Tolerance	V_{OUT2}=1.2V, V_{OUT2}/2 - V_{VTT}, I_{VTT}=0A		-20	-	20	mV
		V_{OUT2}=1.2V, V_{OUT2}/2 - V_{VTT}, I_{VTT}=0.5A		-30	-	30	
I_{LIM}	Current-Limit	Sourcing Current (V_{OUT2}=1.2V)	T_J=25°C	0.6	0.8	-	A
		Sinking Current (V_{OUT2}=1.2V)	T_J=25°C	0.6	0.8	-	
I_{VTTLK}	VTT Leakage Current	V_{VTT}=5V, V_{EN}=0V, T_A=25°C, without Discharge function		-4	-	4	mA
$I_{VTTINLK}$	VTTIN Leakage Current	V_{VTTIN}=5V, V_{EN}=0V, T_A=25°C		-1	-	1	mA
I_{VTTDIS}	VTT Discharge Current	V_{VTT}=0.3V, V_{EN}=0V, T_A=25°C		15	25	35	mA
PWM CONVERTER OUTPUTS							
V_{OUT1}	VOUT1 Regulation Voltage	T_A=25°C, Reg0x02[5:0] = 011000		0.99	1	1.01	V
	VOUT1 Programmable Range	25mV/step		0.4	-	1.975	V
V_{OUT2}	VOUT2 Regulation Voltage	T_A=25°C, default, RSEL=400kΩ or SEL=GND		1.188	1.2	1.212	V
		T_A=25°C, default, RSEL=200kΩ or SEL=floating		1.336	1.35	1.364	
	VOUT2 Programmable Range	25mV/step		0.4	-	1.975	V
V_{OUT3}	VOUT3 Regulation Voltage	T_A=25°C, Reg0x04[5:0] = 010100		1.782	1.8	1.818	V
	VOUT3 Programmable Range	50mV/step		0.8	-	3.95	V
V_{OUT4}	VOUT4 Regulation Voltage	T_A=25°C, Reg0x05[5:0] = 100010		2.475	2.5	2.525	V
	VOUT4 Programmable Range	50mV/step		0.8	-	3.95	V
V_{OUT5}	VOUT5 Regulation Voltage	T_A=25°C, Reg0x06[5:0] = 110010		3.267	3.3	3.333	V
	VOUT4 Programmable Range	50mV/step		0.8	-	3.95	V
	VOUTx Discharge Resistance	EN=low, V_{OUTx}=0.5V		-	20	-	Ω

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{SVIN}=12V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PWM CONTROLLERS						
F_{SW}	Operating Frequency	SEL=GND or RSEL=200kΩ	-20%	1500	+20%	kHz
		SEL=floating or RSEL=400kΩ	-20%	750	+20%	kHz
T_{SS}	Internal Soft Start Time	V_{OUTX} 5% ~ 95%, default	-	1	-	ms
	Soft Start Time Programmable Range	0.5ms/step, Reg0x0B[1:0], Reg0x0C[1:0], Reg0x0D[1:0], Reg0x0E[1:0], Reg0x0F[1:0]	0.5	-	2	ms
$T_{OFF(MIN)}$	Minimum Off Time		-	100	-	ns
$T_{ON(MIN)}$	Minimum On Time		-	60	-	ns
	Zero-Crossing Threshold	PGND-LX	-	5	-	mV
$R_{ON(H)}$	High Side N-MOSFET RDS(ON)	T_A=25°C	-	90	100	mΩ
$R_{ON(L)}$	Low Side N-MOSFET RDS(ON)	T_A=25°C	-	50	60	mΩ
T_D	Dead Time	(Note 4)	-	10	-	ns
PWM CONVERTER PROTECTIONS						
	Low-Side Current Limit	LX1, 2	3	3.5	4	A
	Low-Side Current Limit	LX3, 4, 5	2	2.5	3	A
	OVP Trip Threshold	V_{OUTx} Rising	115	120	125	%
	OVP Debounce Delay		-	10	-	µs
	SCP Trip Threshold	V_{OUTx} Falling	45	50	55	%
	UVP Debounce		-	10	-	µs
	SCP Enable Delay	Retry time up to 3 cycles	-	10	-	ms
GENERAL						
V_{IH}	EN High Threshold Voltage	Voltage Rising	1.2	-	-	V
V_{IL}	EN Low Threshold Voltage	Voltage Falling	-	-	0.4	V
R_{EN}	EN Internal Pull Low Resistance	V_{SVIN}=12V, V_{EN}=12V	-	1	-	mΩ
V_{RST_LOW}	RST Low Level Voltage	I=10mA	-	-	0.4	V
	RST Rising Threshold Voltage	All Channel 1 ~ 5 I V_{OUT} Rising	87	90	93	%V_{REF}
	RST Falling Threshold Voltage	Any Channel 1 ~ 5 V_{OUT} Falling	-	87	-	%V_{REF}
		Any Channel 1 ~ 5 V_{OUT} Rising	115	120	125	%V_{REF}
	RST Low to High Delay Time		-	10	-	ms
	RST High to Low Debounce Time		-	5	-	µs
	SEL Source Current		4	5	6	µA
V_{SEL_1}	SEL Logic Voltage Range		0	-	0.6	V
V_{SEL_2}			0.6	-	1.5	V
V_{SEL_3}			1.5	-	2.5	V
V_{SEL_4}			2.5	-	3.3	V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	150	-	°C
	Thermal Shutdown Hysteresis		-	30	-	°C

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{SVIN}=12V, and T_A = -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

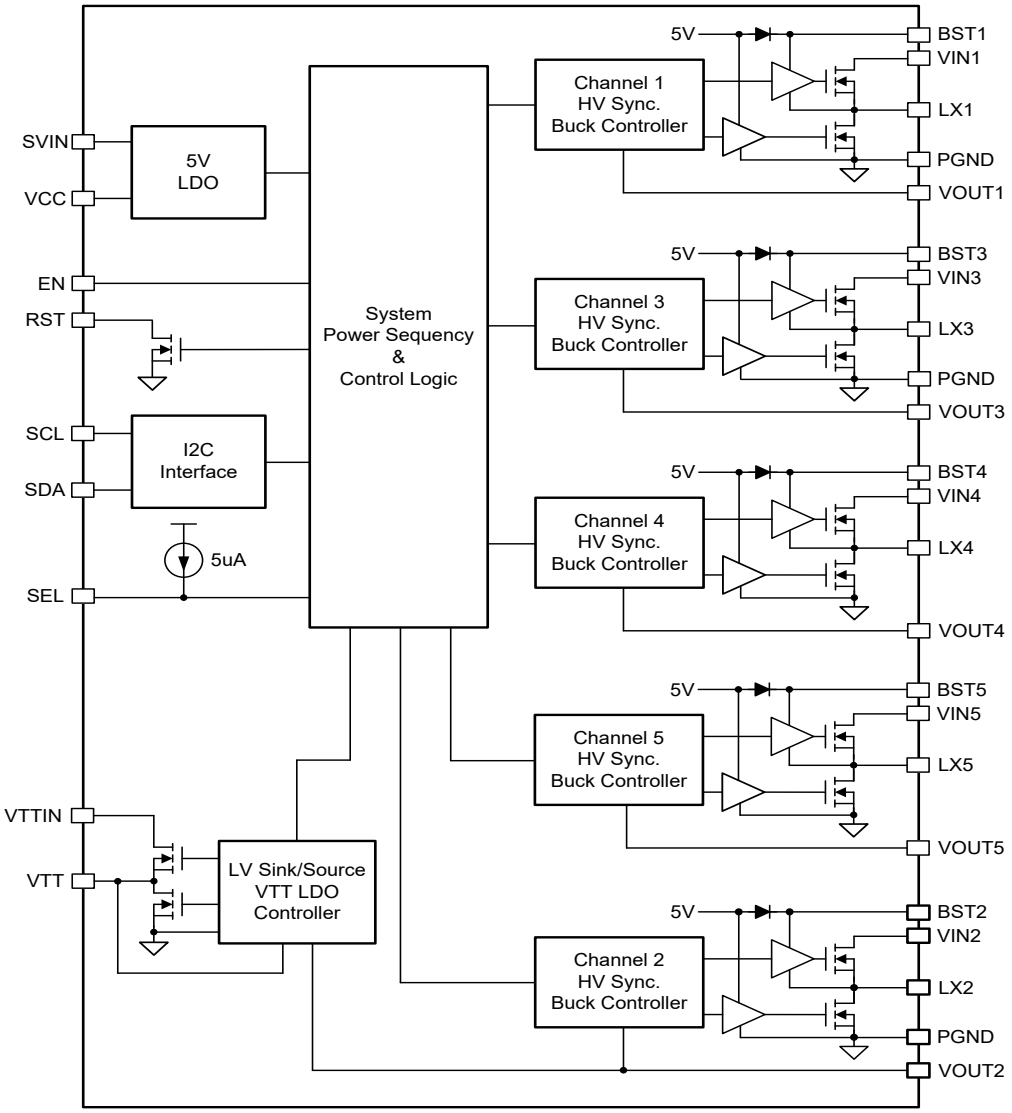
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TIMING						
	Discharge Active Time During Power On		-	1	-	ms
T_{D1}	Buck 1 POK Delay Time	Default, Reg0x0B[4:2] = 001	-	1.7	-	ms
T_{D2}	Buck 2 POK Delay Time	Default, Reg0x0C[4:2] = 001	-	1.7	-	ms
T_{D3}	Buck 3 POK Delay Time	Default, Reg0x0D[4:2] = 001	-	1.7	-	ms
T_{D4}	Buck 4 POK Delay Time	Default, Reg0x0E[4:2] = 001	-	1.7	-	ms
T_{D5}	Buck 5 POK Delay Time	Default, Reg0x0F[4:2] = 001	-	1.7	-	ms
	POK Programmable Range	Reg0x0B[4:2]~Reg0x0F[4:2] = 000	-	1.2	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 010	-	2.7	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 011	-	5.7	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 100	-	10	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 101	-	25	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 110	-	50	-	ms
		Reg0x0B[4:2]~Reg0x0F[4:2] = 111	-	75	-	ms
T_{D_OFF1}	Power Off Delay Time	Reg0x11[1:0] = 00	-	20	-	ms
T_{D_OFF2}		Reg0x11[3:2] = 00	-	20	-	ms
T_{D_OFF3}		Reg0x11[5:4] = 00	-	20	-	ms
T_{D_OFF4}		Reg0x11[7:6] = 00	-	20	-	ms
	Power Off Delay Time Programmable Range		20	-	50	ms
I^2C INTERFACE						
f_{SCL}	Frequency, SCL		-	-	400	kHz
	SDA, SCL Input High Voltage		1.2	-	5	V
	SDA, SCL Input Low Voltage		0	-	0.4	V
	SDA, SCL Leakage Current	V_{SDA}=V_{SCL}=5V	-	-	100	nA
$t_{W(H)}$	Pulse Duration, SCL High		600	-	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low		1300	-	-	ns
t_r	Rise Time, SCL and SDA		20+0.1 C_L(pF)	-	300	ns
tf	Fall Time, SCL and SDA		20+0.1 C_L(pF)	-	300	ns
t_{setup1}	Setup Time, SCL to SDA		100	-	-	ns
t_{hold1}	Hold Time, SCL to SDA		100	-	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition		1300	-	-	ns
t_{setup2}	Setup Time, SCL to Start Condition		600	-	-	ns
t_{hold2}	Hold Time, Start condition to SCL		600	-	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition		600	-	-	ns
C_L	Load Capacitance for Each Bus Line		-	-	400	pF
t_{VD_DATA}	Data Valid Time		-	-	900	ns
t_{VD_ACK}	Data Valid Acknowledge Time		-	-	900	ns

Note 4: Guaranteed by design.

Pin Description

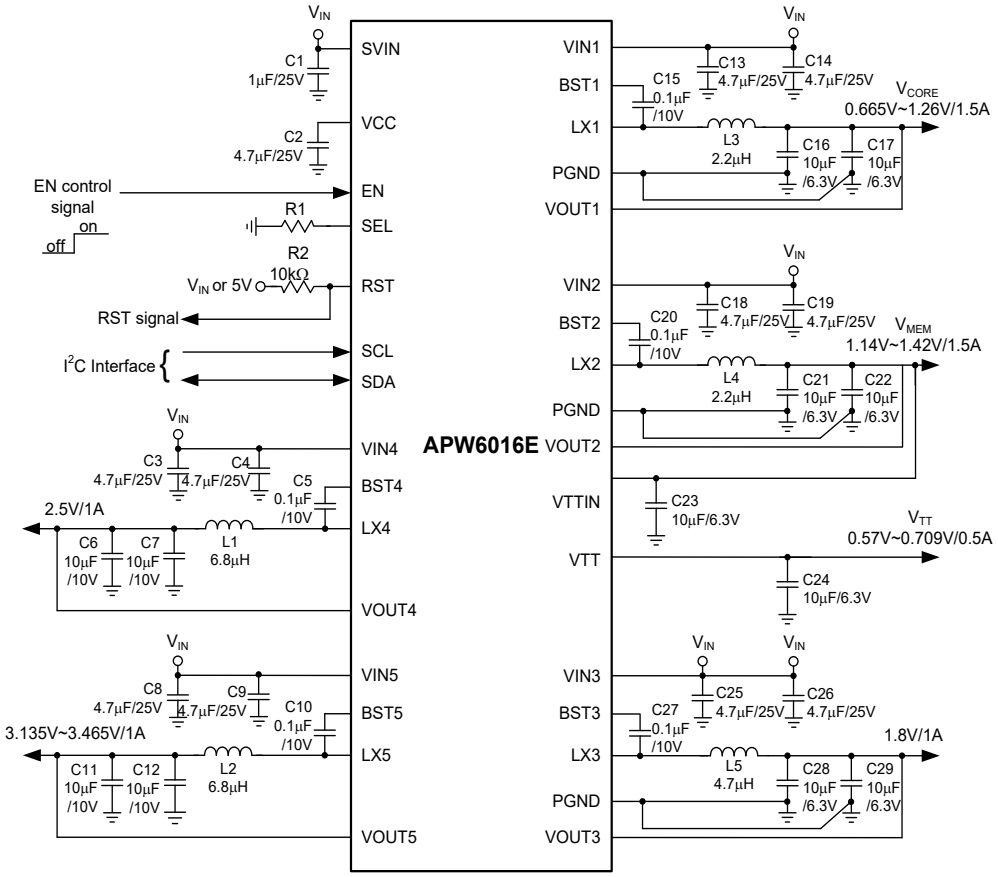
<table>
<tr><th>NO.</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>3, 9, 17,
28, 29</td><td>BSTx</td><td>PWM Converter High-Side Gate Driver Supply Voltage Input Pin.
A 0.1uF X5R ceramic capacitor is connected from this pin to the LX pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.</td></tr>
<tr><td>6, 12, 20,
26, 31</td><td>VINx</td><td>Power Supply Input for Buck Converters. Bypass this pin to PGND with a 10μF ceramic capacitor.</td></tr>
<tr><td>5, 11, 19
27, 30</td><td>LXx</td><td>PWM Converter Power Switching Output.
This pin is the junction of the high side power MOSFET and the low side power MOSFET.
Connect this pin to the output inductor.</td></tr>
<tr><td>7, 13, 21,
25, 32</td><td>VOUTx</td><td>Output voltage Feedback Pin. Connect to VOUTx output voltage.</td></tr>
<tr><td>4, 10, 18</td><td>PGND</td><td>Power Ground.
This pin must be connected directly to the GND plane of the PCB using low inductance vias.</td></tr>
<tr><td>8</td><td>EN</td><td></td></tr>
<tr><td>1</td><td>VCC</td><td>Internal Regulator Output Pin.
The APW6016E provides an internal 5V VCC regulator for the internal control circuitry.
It is recommended to connect a 4.7uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.</td></tr>
<tr><td>2</td><td>SVIN</td><td>Power Supply Input for VCC LDO regulator.</td></tr>
<tr><td>14</td><td>VTTIN</td><td>Power Supply Input for VTT LDO.</td></tr>
<tr><td>15</td><td>VTT</td><td>Power Output for the VTT LDO.</td></tr>
<tr><td>16</td><td>SEL</td><td>Power On Strapping Pin for selecting SVIN POR Threshold, V_{OUT2} and Switching Frequency of Buck Converters.
<table>
<tr><th>SEL pin to ground</th><th>System Application</th><th>V_{POR_R}</th><th>V_{OUT2}</th><th>F_{SW}</th></tr>
<tr><td>Floating</td><td>12V</td><td>10.5V</td><td>1.35V</td><td>750kHz</td></tr>
<tr><td>400kΩ</td><td>12V</td><td>10.5V</td><td>1.2V</td><td>750kHz</td></tr>
<tr><td>200kΩ</td><td>5V</td><td>4.2V</td><td>1.35V</td><td>1.5MHz</td></tr>
<tr><td>GND</td><td>5V</td><td>4.2V</td><td>1.2V</td><td>1.5MHz</td></tr>
</table></td></tr>
<tr><td>23</td><td>SDA</td><td rowspan="2">I^2C Interface.</td></tr>
<tr><td>24</td><td>SCL</td></tr>
<tr><td>22</td><td>RST</td><td>The Open Drain Output for Reset. Connect a resistor in kW value, such as 10~100 kΩ to pull up this pin to a power source. When all buck regulator's and VTT's output voltage are in regulation range, the internal MOSFET turned off and this pin is pulled high by external power.</td></tr>
<tr><td>-</td><td>Thermal Pad</td><td>Ground. Connect the pad to a larger area of ground planes underneath with vias for proper heat dissipation.</td></tr>
</table>

Block Diagram



Typical Application Circuit

For VIN=12V Application Circuit

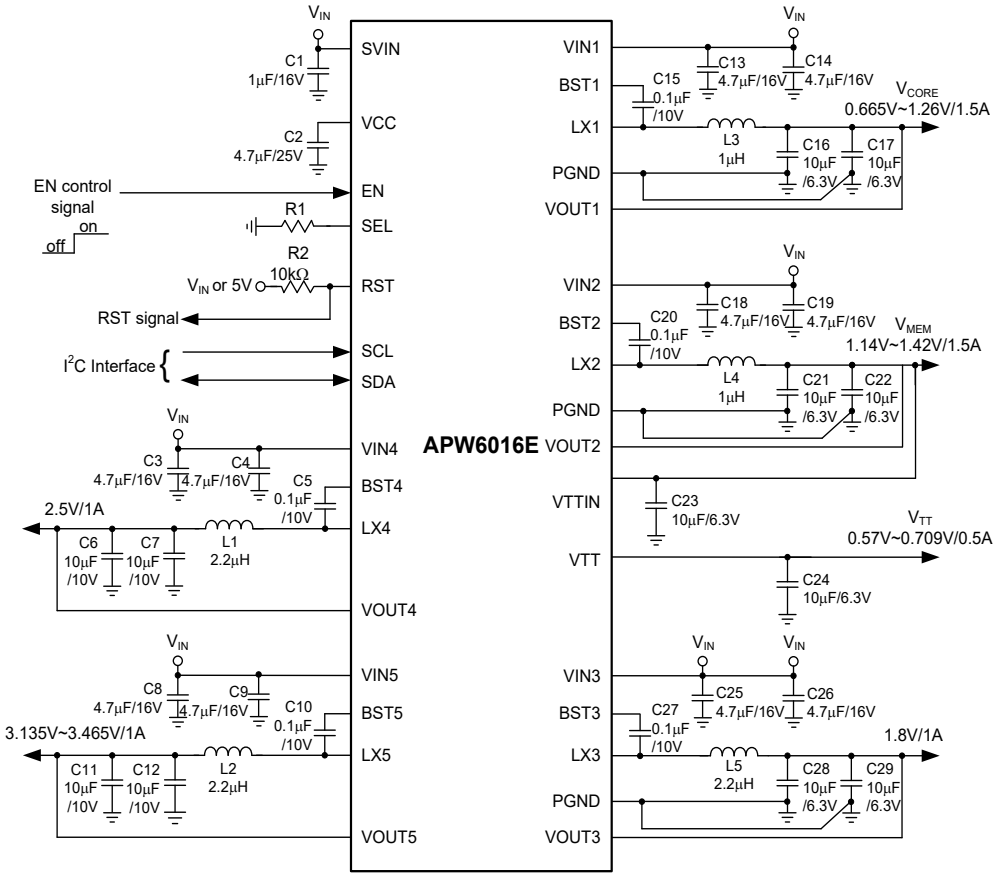


Suggested BOM List

Designation	Manufacturer	Part No.	Description
C1	muRata	GRM188R71E105KA12	1μF, 25V, X7R, 0603
C2	muRata	GRM21BR61E475KA12L	4.7μF, 25V, X5R, 0805
C3, C4, C8, C9, C13, C14, C18, C19, C25, C26	muRata	GRM219C71E475ME21	4.7μF, 25V, X7S, 0805
C5, C10, C15, C20, C27	muRata	GRM155R71A1104MA01	0.1μF, 10V, X7R, 0402
C6, C7, C11, C12	muRata	GRM21BR71A106KA73	10μF, 10V, X7R, 0805
C16, C17, C21, C22, C23, C24, C28, C29	muRata	GRM21BR70J106ME76	10μF, 6.3V, X7R, 0805
L1, L2	Mag Layers	MMD-05AHN6R8M-X2	6.8μH, 5.5mmx5.2mm
L3, L4	Mag Layers	MMD-05AHN2R2M-X2	2.2μH, 5.5mmx5.2mm
L5	Mag Layers	MMD-05AHN4R7M-X2	4.7μH, 5.5mmx5.2mm
R1	Common part		Value depends on application, refer to pin description.
R2	Common part		10kΩ, 0402

Typical Application Circuit (Cont.)

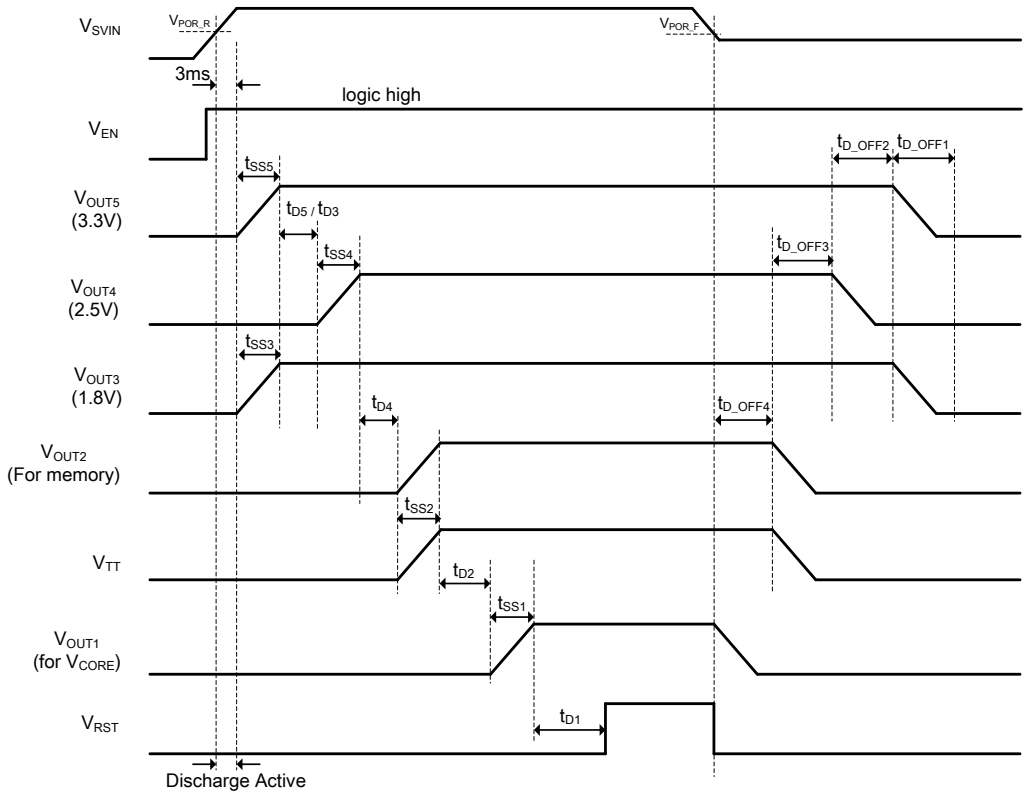
For VIN=5V Application Circuit



Suggested BOM List

Designation	Manufacturer	Part No.	Description
C1	muRata	GRM188R71C105KE15	1μF, 16V, X7R, 0603
C2	muRata	GRM21BR61E475KA12L	4.7μF, 25V, X5R, 0805
C3, C4, C8, C9, C13, C14, C18, C19, C25, C26	muRata	GRM21BR71C475KE51	4.7μF, 16V, X7R, 0805
C5, C10, C15, C20, C27	muRata	GRM155R71A1104MA01	0.1μF, 10V, X7R, 0402
C6, C7, C11, C12	muRata	GRM21BR71A106KA73	10μF, 10V, X7R, 0805
C16, C17, C21, C22, C23, C24, C28, C29	muRata	GRM21BR70J106ME76	10μF, 6.3V, X7R, 0805
L1, L2, L5	Mag Layers	MMD-05AHN2R2M-X2	2.2μH, 5.5mmx5.2mm
L3, L4	Cyntec	SDTR041H-1R0MS	1.0μH, 4.1mmx3.6mm
R1	Common part		Value depends on application, refer to pin description
R2	Common part		10kΩ, 0402

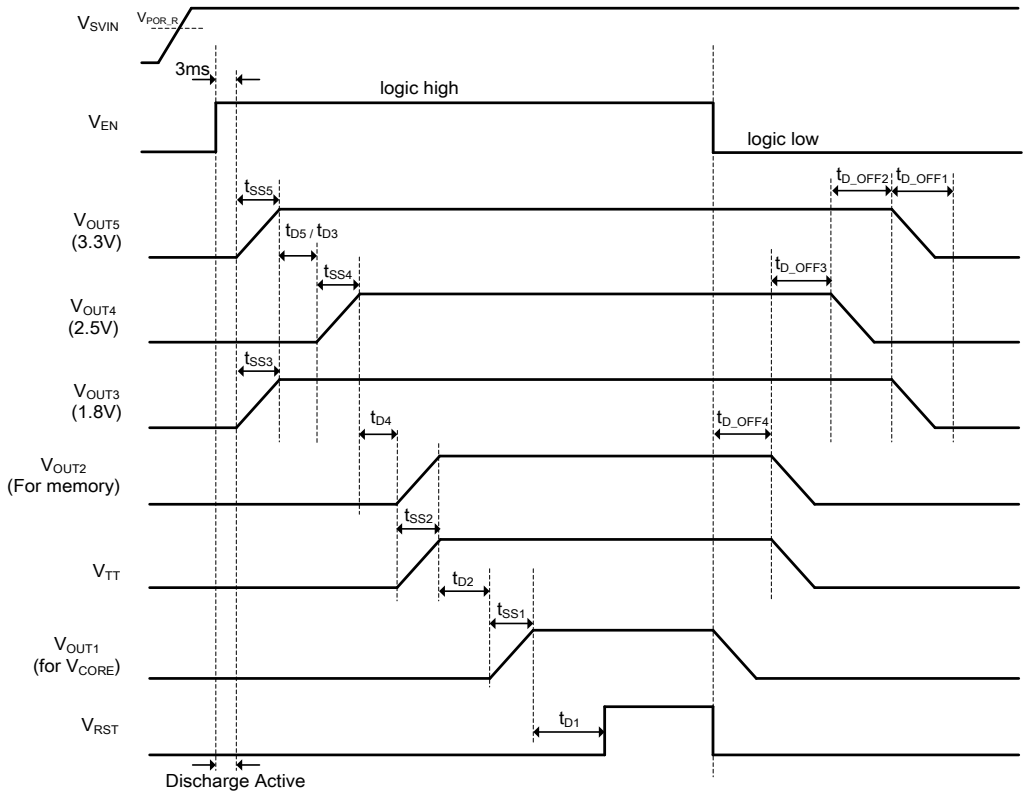
Timing Chart



Parameter	Adjustable Timing Range	Step Value
T_{SS1}	0.5ms ~ 2 ms	0.5ms
T_{D1}	1.2ms ~ 75 ms	Follow Reg.
T_{SS2}	0.5ms ~ 2 ms	0.5ms
T_{D2}	1.2ms ~ 75 ms	Follow Reg.
T_{SS3}	0.5ms ~ 2 ms	0.5ms
T_{D3}	1.2ms ~ 75 ms	Follow Reg.
T_{SS4}	0.5ms ~ 2 ms	0.5ms
T_{D4}	1.2ms ~ 75 ms	Follow Reg.
T_{SS5}	0.5ms ~ 2 ms	0.5ms
T_{D5}	1.2ms ~ 75 ms	Follow Reg.
T_{D_OFF1}	20ms ~ 50ms	10ms
T_{D_OFF2}	20ms ~ 50ms	10ms
T_{D_OFF3}	20ms ~ 50ms	10ms
T_{D_OFF4}	20ms ~ 50ms	10ms

Timing Chart (Cont.)

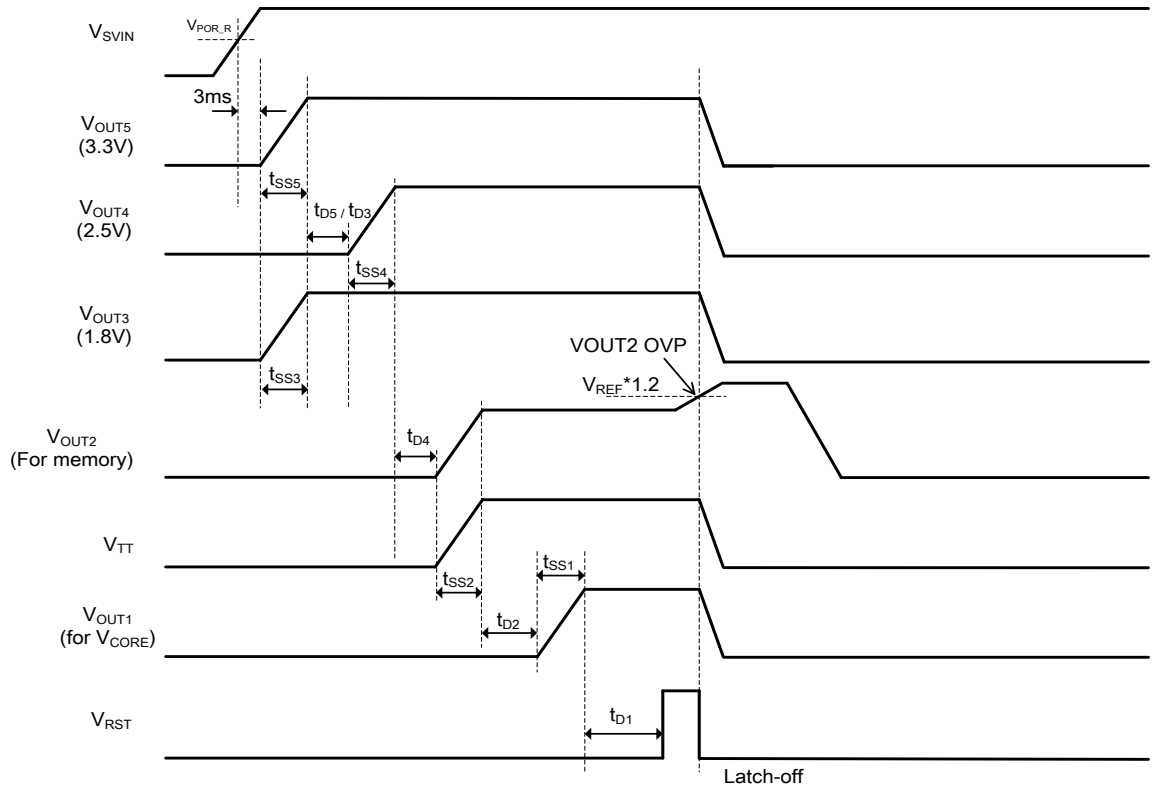
EN on/off



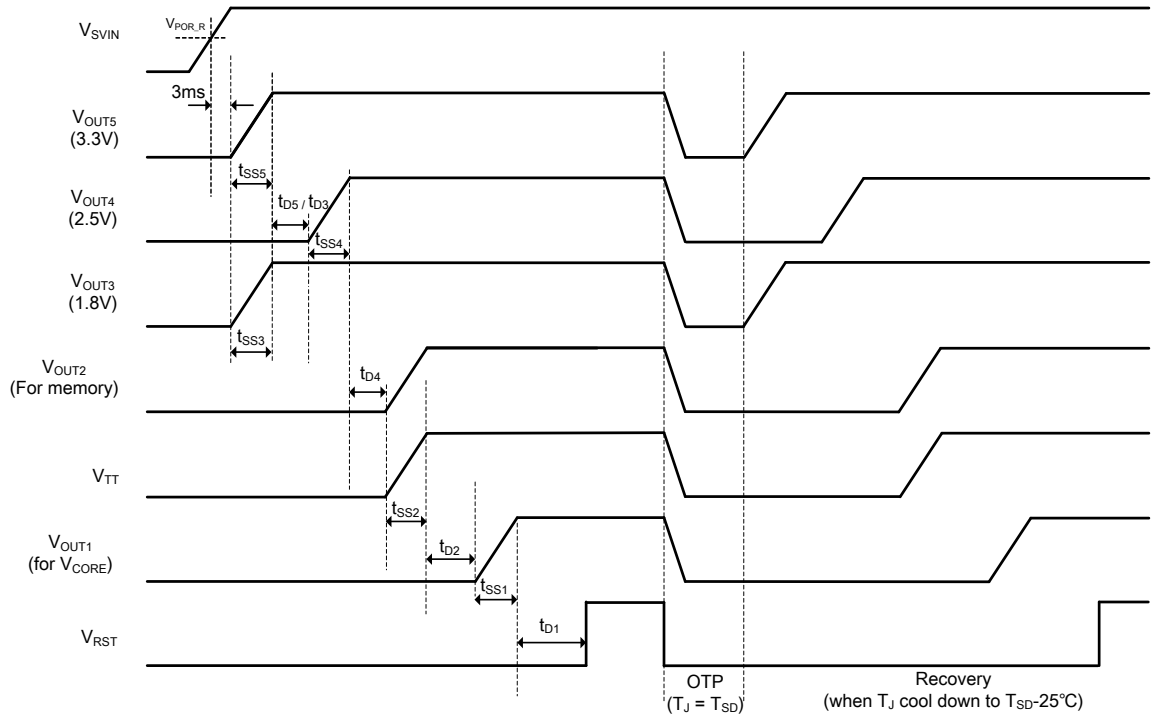
Parameter	Adjustable Timing Range	Step Value
T_{SS1}	0.5ms ~ 2 ms	0.5ms
T_{D1}	1.2ms ~ 75 ms	Follow Reg.
T_{SS2}	0.5ms ~ 2 ms	0.5ms
T_{D2}	1.2ms ~ 75 ms	Follow Reg.
T_{SS3}	0.5ms ~ 2 ms	0.5ms
T_{D3}	1.2ms ~ 75 ms	Follow Reg.
T_{SS4}	0.5ms ~ 2 ms	0.5ms
T_{D4}	1.2ms ~ 75 ms	Follow Reg.
T_{SS5}	0.5ms ~ 2 ms	0.5ms
T_{D5}	1.2ms ~ 75 ms	Follow Reg.
T_{D_OFF1}	20ms ~ 50ms	10ms
T_{D_OFF2}	20ms ~ 50ms	10ms
T_{D_OFF3}	20ms ~ 50ms	10ms
T_{D_OFF4}	20ms ~ 50ms	10ms

Timing Chart (Cont.)

VOUT OVP and Latch-off

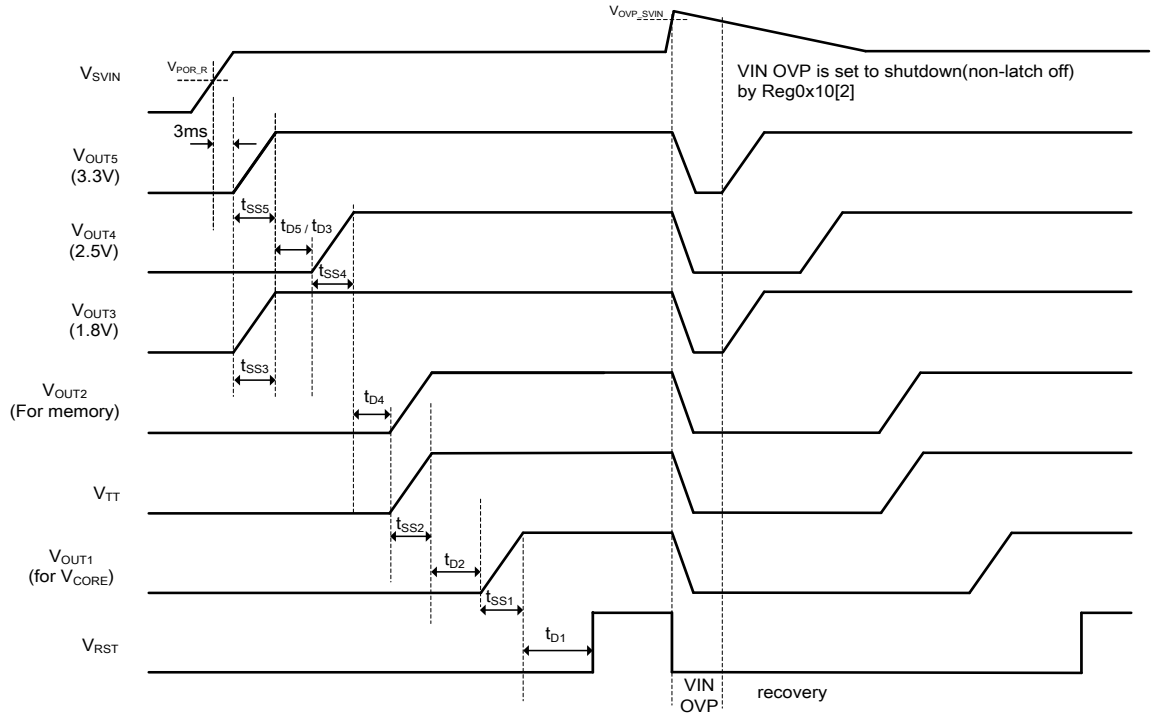


OTP

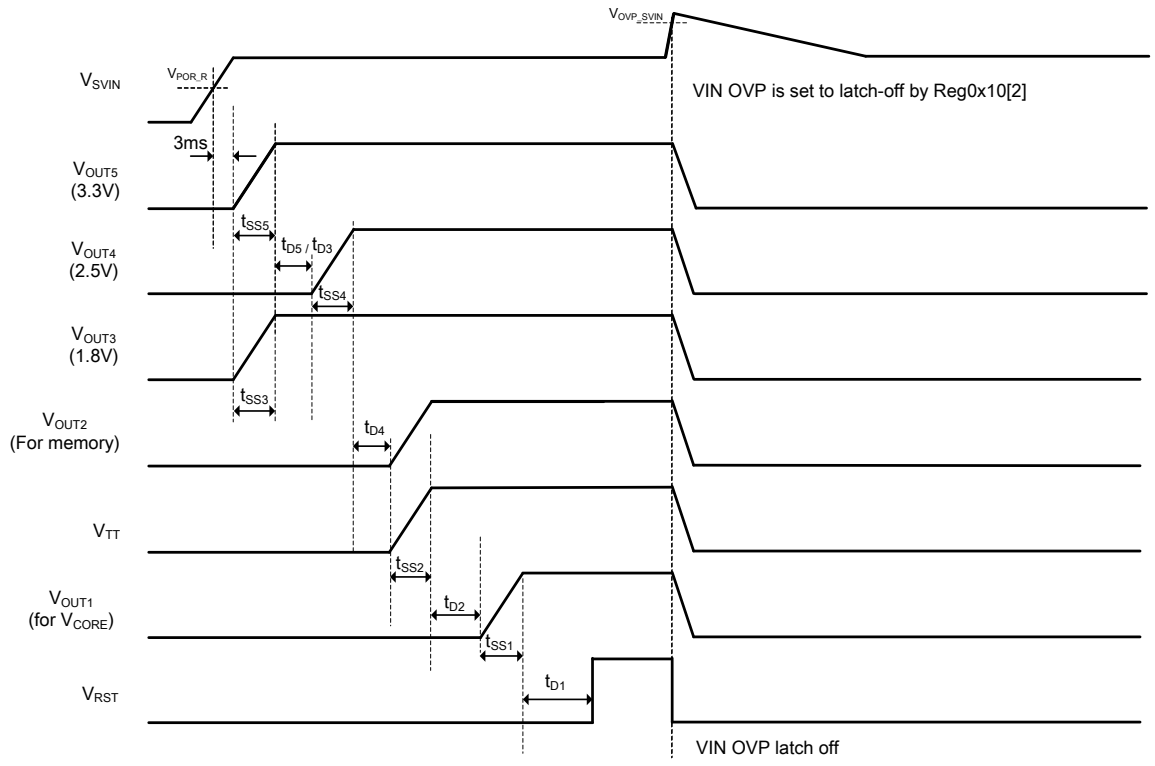


Timing Chart (Cont.)

VIN OVP (non-latchoff)

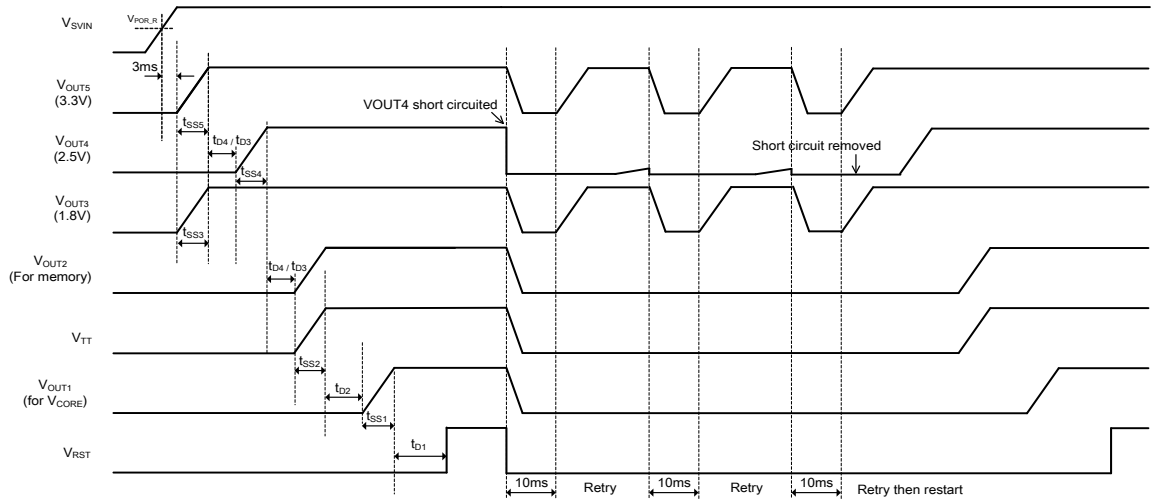


VIN OVP (latchoff)

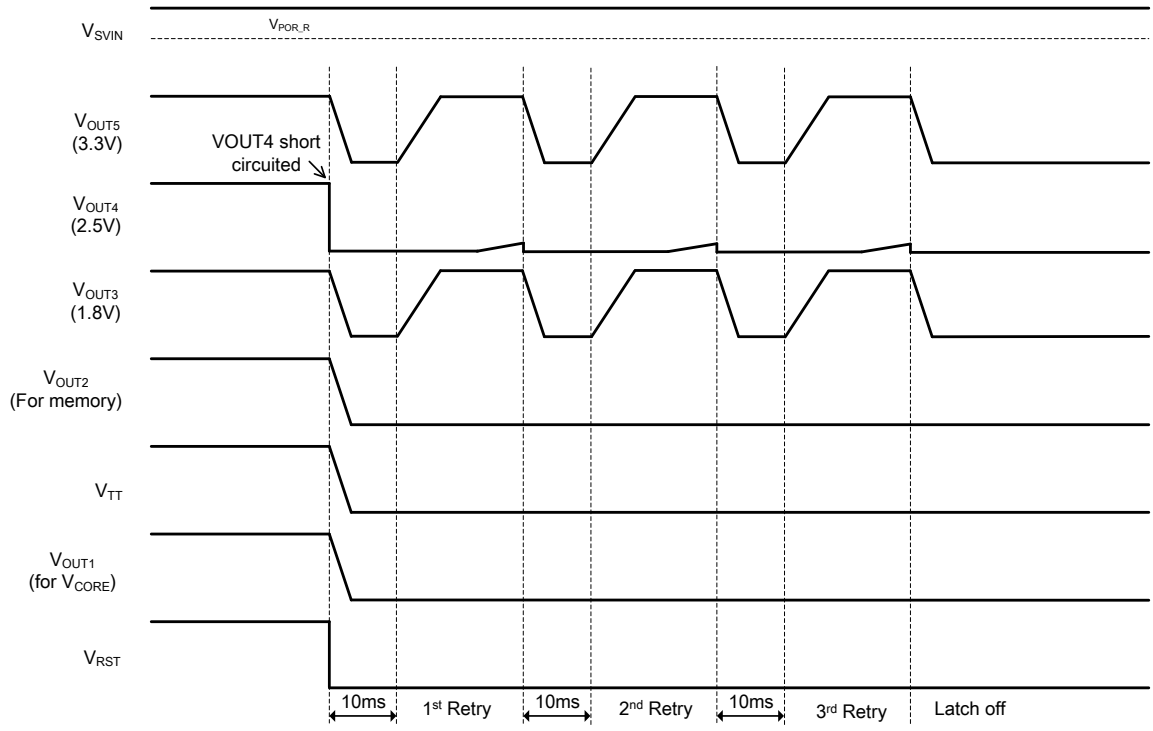


Timing Chart (Cont.)

SCP and restart



SCP and Latchoff



I2C 7bit hard-coded Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	0	0	1	R/W

Register Map

REGISTER ADDRESS	Field Name	BIT	Bit Name	DEFAULT	DESCRIPTION	R/W	Reset
0x00	ID	[5:0]	CHIP_ID[5:0]	8'h5B		R	POR
0x01	BUCK, VTT_ONOFF CONTROL	[6]	Fault_Clear	0	1 : Clear All Fault Flag 0 : Remain Fault Flag	R/W	Write "1"
		[5]	ONBUCK5	1	BUCK5 Enable Signal. 0 : Shutdown 1 : Operation	R/W	Pre-POR
		[4]	ONBUCK4	1	BUCK4 Enable Signal. 0 : Shutdown 1 : Operation	R/W	Pre-POR
		[3]	ONBUCK3	1	BUCK3 Enable Signal. 0 : Shutdown 1 : Operation	R/W	Pre-POR
		[2]	ONBUCK2	1	BUCK2 Enable Signal. 0 : Shutdown 1 : Operation	R/W	Pre-POR
		[1]	ONBUCK1	1	BUCK1 Enable Signal. 0 : Shutdown 1 : Operation	R/W	Pre-POR
		[0]	ONVTT	1	VTT Enable Signal. 0 : Shutdown (When ONBUCK2=1) 1 : Follow ONBUCK2 bit setting	R/W	Pre-POR
0x02	VBUCK1_NRM[7:0]	[7:6]	VBUCK1_NRM[7:6]	01	Setting the BUCK1 operating in auto PFM mode. 00 : Auto PWM/PFM disable 01 : Auto PWM/PFM enable 10 : Auto PWM/USM enable	R/W	Pre-POR
		[5:0]	VBUCK1_NRM[5:0]	011000	BUCK1 DAC[5:0] volt. Level: Pls. check the Vout setting table blank.	R/W	Pre-POR
0x03	VBUCK2_NRM[7:0]	[7:6]	VBUCK2_NRM[7:6]	01	Setting the BUCK2 operating in auto PFM mode. 00 : Auto PWM/PFM disable 01 : Auto PWM/PFM enable 10 : Auto PWM/USM enable	R/W	Pre-POR
		[5:0]	VBUCK2_NRM[5:0]	100000	BUCK2 DAC[5:0] volt. Level: Pls. check the Vout setting table blank.	R/W	Pre-POR
0x04	VBUCK3_NRM[7:0]	[7:6]	VBUCK3_NRM[7:6]	01	Setting the BUCK3 operating in auto PFM mode. 00 : Auto PWM/PFM disable 01 : Auto PWM/PFM enable 10 : Auto PWM/USM enable	R/W	Pre-POR
		[5:0]	VBUCK3_NRM[5:0]	010100	BUCK3 DAC[5:0] volt. Level: Pls. check the Vout setting table blank.	R/W	Pre-POR
0x05	VBUCK4_NRM[7:0]	[7:6]	VBUCK4_NRM[7:6]	01	Setting the BUCK4 operating in auto PFM mode. 00 : Auto PWM/PFM disable 01 : Auto PWM/PFM enable 10 : Auto PWM/USM enable	R/W	Pre-POR
		[5:0]	VBUCK4_NRM[5:0]	100010	BUCK4 DAC[5:0] volt. Level: Pls. check the Vout setting table blank.	R/W	Pre-POR
0x06	VBUCK5_NRM[7:0]	[7:6]	VBUCK5_NRM[7:6]	01	Setting the BUCK5 operating in auto PFM mode. 00 : Auto PWM/PFM disable 01 : Auto PWM/PFM enable 10 : Auto PWM/USM enable	R/W	Pre-POR
		[5:0]	VBUCK5_NRM[5:0]	110010	BUCK5 DAC[5:0] volt. Level: Pls. check the Vout setting table blank.	R/W	Pre-POR

Register Map (Cont.)

REGISTER ADDRESS	Field Name	BIT	Bit Name	DEFAULT	DESCRIPTION	R/W	Reset
0x07	POK	[5]	BUCK5_POK	0	BUCK5 voltage > 90%*Vref active high 0 : BUCK5 not ready 1 : BUCK5 ready	R	Pre-POR
		[4]	BUCK4_POK	0	BUCK4 voltage > 90%*Vref active high 0 : BUCK4 not ready 1 : BUCK4 ready	R	Pre-POR
		[3]	BUCK3_POK	0	BUCK3 voltage > 90%*Vref active high 0 : BUCK3 not ready 1 : BUCK3 ready	R	Pre-POR
		[2]	BUCK2_POK	0	BUCK2 voltage > 90%*Vref active high 0 : BUCK2 not ready 1 : BUCK2 ready	R	Pre-POR
		[1]	BUCK1_POK	0	BUCK1 voltage > 90%*Vref active high 0 : BUCK1 not ready 1 : BUCK1 ready	R	Pre-POR
		[0]	VTT_POK	0	VTT voltage > 90%*Vref active high 0 : VTT not ready 1 : VTT ready	R	Pre-POR
0x08	BUCK, LDO_ DISCHG CONTROL	[5]	ENDIS_BUCK5	1	Enable BUCK5 output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
		[4]	ENDIS_BUCK4	1	Enable BUCK4 output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
		[3]	ENDIS_BUCK3	1	Enable BUCK3 output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
		[2]	ENDIS_BUCK2	1	Enable BUCK2 output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
		[1]	ENDIS_BUCK1	1	Enable BUCK1 output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
		[0]	ENDIS_VTT	1	Enable VTT output discharge function during PMIC in shutdown mode. 0 : Disable 1 : Enable (default)	R/W	Pre-POR
0x09	BUCK, LDO UVP Status	[6]	OTP	0	PMIC over temperature.	R	EN/ POR
		[5]	BUCK5_UVP	0	Record the UVP protection of BUCK5 ever occurs.	R	EN/ POR
		[4]	BUCK4_UVP	0	Record the UVP protection of BUCK4 ever occurs.	R	EN/ POR
		[3]	BUCK3_UVP	0	Record the UVP protection of BUCK3 ever occurs.	R	EN/ POR
		[2]	BUCK2_UVP	0	Record the UVP protection of BUCK2 ever occurs.	R	EN/ POR
		[1]	BUCK1_UVP	0	Record the UVP protection of BUCK1 ever occurs.	R	EN/ POR
		[0]	VTT_UVP	0	Record the UVP protection of VTT LDO ever occurs.	R	EN/ POR

Register Map (Cont.)

REGISTER ADDRESS	Field Name	BIT	Bit Name	DEFAULT	DESCRIPTION	R/W	Reset
0x0A	BUCK, LDO OVP Status	[5]	BUCK5_OVP	0	Record the OVP protection of BUCK5 ever occurs.	R	EN/ POR
		[4]	BUCK4_OVP	0	Record the OVP protection of BUCK4 ever occurs.	R	EN/ POR
		[3]	BUCK3_OVP	0	Record the OVP protection of BUCK3 ever occurs.	R	EN/ POR
		[2]	BUCK2_OVP	0	Record the OVP protection of BUCK2 ever occurs.	R	EN/ POR
		[1]	BUCK1_OVP	0	Record the OVP protection of BUCK1 ever occurs.	R	EN/ POR
		[0]	VTT_OVP	0	Record the OVP protection of VTT LDO ever occurs.	R	EN/ POR
0x0B	T1	[4:2]	TD1	001	SET Buck1 POK Delay. 000 : 1.2ms, 001 : 1.7ms, 010 : 2.7ms, 011 : 5.7ms, 100 : 10ms, 101 : 25ms, 110 : 50ms, 111 : 75ms	R/W	Pre-POR
		[1:0]	TSS1	01	Set Buck1 Softstart Time. 00 : 0.5ms, 01 : 1ms, 10 : 1.5ms, 11 : 2ms	R/W	Pre-POR
0x0C	T2	[4:2]	TD2	001	SET Buck2 POK Delay. 000 : 1.2ms, 001 : 1.7ms, 010 : 2.7ms, 011 : 5.7ms, 100 : 10ms, 101 : 25ms, 110 : 50ms, 111 : 75ms	R/W	Pre-POR
		[1:0]	TSS2	01	Set Buck2 Softstart Time. 00 : 0.5ms, 01 : 1ms, 10 : 1.5ms, 11 : 2ms	R/W	Pre-POR
0x0D	T3	[4:2]	TD3	001	SET Buck3 POK Delay. 000 : 1.2ms, 001 : 1.7ms, 010 : 2.7ms, 011 : 5.7ms, 100 : 10ms, 101 : 25ms, 110 : 50ms, 111 : 75ms	R/W	Pre-POR
		[1:0]	TSS3	01	Set Buck3 Softstart Time. 00 : 0.5ms, 01 : 1ms, 10 : 1.5ms, 11 : 2ms	R/W	Pre-POR
0x0E	T4	[4:2]	TD4	001	SET Buck4 POK Delay. 000 : 1.2ms, 001 : 1.7ms, 010 : 2.7ms, 011 : 5.7ms, 100 : 10ms, 101 : 25ms, 110 : 50ms, 111 : 75ms	R/W	Pre-POR
		[1:0]	TSS4	01	Set Buck4 Softstart Time. 00 : 0.5ms, 01 : 1ms, 10 : 1.5ms, 11 : 2ms	R/W	Pre-POR
0x0F	T5	[4:2]	TD5	001	SET Buck5 POK Delay. 000 : 1.2ms, 001 : 1.7ms, 010 : 2.7ms, 011 : 5.7ms, 100 : 10ms, 101 : 25ms, 110 : 50ms, 111 : 75ms	R/W	Pre-POR
		[1:0]	TSS5	01	Set Buck5 Softstart Time. 00 : 0.5ms, 01 : 1ms, 10 : 1.5ms, 11 : 2ms	R/W	Pre-POR
0x10	VIN_Status	[2]	PMIC _VINOVP_L	0	1 : VIN OVP Latch off 0 : VIN OVP shutdown (non-latch off)	R/W	Pre-POR
		[1]	PMIC_VINOVP_EN	1	1 : Enable VIN OVP 0 : Disable VIN OVP	R/W	Pre-POR
		[0]	PMIC UVLO	0	1 : V_{SVIN}>POR 0 : V_{SVIN}<POR	R	Pre-POR
0x11	Power Off Delay Time	[7:6]	T_{D_OFF4}	00	00 : 20ms, 01 : 30ms, 10 : 40ms, 11 : 50ms	R/W	Pre-POR
		[5:4]	T_{D_OFF3}	00	00 : 20ms, 01 : 30ms, 10 : 40ms, 11 : 50ms	R/W	Pre-POR
		[3:2]	T_{D_OFF2}	00	00 : 20ms, 01 : 30ms, 10 : 40ms, 11 : 50ms	R/W	Pre-POR
		[1:0]	T_{D_OFF1}	00	00 : 20ms, 01 : 30ms, 10 : 40ms, 11 : 50ms	R/W	Pre-POR

Reg0x02~Reg0x06 Buck1 to Buck5 Voltage Setting Table

	Bits						Voltage (V)				
	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5
0	0	0	0	0	0	0	0.4	0.4	0.8	0.8	0.8
1	0	0	0	0	0	1	0.425	0.425	0.85	0.85	0.85
2	0	0	0	0	1	0	0.45	0.45	0.9	0.9	0.9
3	0	0	0	0	1	1	0.475	0.475	0.95	0.95	0.95
4	0	0	0	1	0	0	0.5	0.5	1	1	1
5	0	0	0	1	0	1	0.525	0.525	1.05	1.05	1.05
6	0	0	0	1	1	0	0.55	0.55	1.1	1.1	1.1
7	0	0	0	1	1	1	0.575	0.575	1.15	1.15	1.15
8	0	0	1	0	0	0	0.6	0.6	1.2	1.2	1.2
9	0	0	1	0	0	1	0.625	0.625	1.25	1.25	1.25
10	0	0	1	0	1	0	0.65	0.65	1.3	1.3	1.3
11	0	0	1	0	1	1	0.675	0.675	1.35	1.35	1.35
12	0	0	1	1	0	0	0.7	0.7	1.4	1.4	1.4
13	0	0	1	1	0	1	0.725	0.725	1.45	1.45	1.45
14	0	0	1	1	1	0	0.75	0.75	1.5	1.5	1.5
15	0	0	1	1	1	1	0.775	0.775	1.55	1.55	1.55
16	0	1	0	0	0	0	0.8	0.8	1.6	1.6	1.6
17	0	1	0	0	0	1	0.825	0.825	1.65	1.65	1.65
18	0	1	0	0	1	0	0.85	0.85	1.7	1.7	1.7
19	0	1	0	0	1	1	0.875	0.875	1.75	1.75	1.75
20	0	1	0	1	0	0	0.9	0.9	1.8	1.8	1.8
21	0	1	0	1	0	1	0.925	0.925	1.85	1.85	1.85
22	0	1	0	1	1	0	0.95	0.95	1.9	1.9	1.9
23	0	1	0	1	1	1	0.975	0.975	1.95	1.95	1.95
24	0	1	1	0	0	0	1	1	2	2	2
25	0	1	1	0	0	1	1.025	1.025	2.05	2.05	2.05
26	0	1	1	0	1	0	1.05	1.05	2.1	2.1	2.1
27	0	1	1	0	1	1	1.075	1.075	2.15	2.15	2.15
28	0	1	1	1	0	0	1.1	1.1	2.2	2.2	2.2
29	0	1	1	1	0	1	1.125	1.125	2.25	2.25	2.25
30	0	1	1	1	1	0	1.15	1.15	2.3	2.3	2.3
31	0	1	1	1	1	1	1.175	1.175	2.35	2.35	2.35
32	1	0	0	0	0	0	1.2	1.2	2.4	2.4	2.4

Reg0x02~Reg0x06 Buck1 to Buck5 Voltage Setting Table (Cont.)

	Bits						Voltage (V)				
	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5
33	1	0	0	0	0	1	1.225	1.225	2.45	2.45	2.45
34	1	0	0	0	1	0	1.25	1.25	2.5	2.5	2.5
35	1	0	0	0	1	1	1.275	1.275	2.55	2.55	2.55
36	1	0	0	1	0	0	1.3	1.3	2.6	2.6	2.6
37	1	0	0	1	0	1	1.325	1.325	2.65	2.65	2.65
38	1	0	0	1	1	0	1.35	1.35	2.7	2.7	2.7
39	1	0	0	1	1	1	1.375	1.375	2.75	2.75	2.75
40	1	0	1	0	0	0	1.4	1.4	2.8	2.8	2.8
41	1	0	1	0	0	1	1.425	1.425	2.85	2.85	2.85
42	1	0	1	0	1	0	1.45	1.45	2.9	2.9	2.9
43	1	0	1	0	1	1	1.475	1.475	2.95	2.95	2.95
44	1	0	1	1	0	0	1.5	1.5	3	3	3
45	1	0	1	1	0	1	1.525	1.525	3.05	3.05	3.05
46	1	0	1	1	1	0	1.55	1.55	3.1	3.1	3.1
47	1	0	1	1	1	1	1.575	1.575	3.15	3.15	3.15
48	1	1	0	0	0	0	1.6	1.6	3.2	3.2	3.2
49	1	1	0	0	0	1	1.625	1.625	3.25	3.25	3.25
50	1	1	0	0	1	0	1.65	1.65	3.3	3.3	3.3
51	1	1	0	0	1	1	1.675	1.675	3.35	3.35	3.35
52	1	1	0	1	0	0	1.7	1.7	3.4	3.4	3.4
53	1	1	0	1	0	1	1.725	1.725	3.45	3.45	3.45
54	1	1	0	1	1	0	1.75	1.75	3.5	3.5	3.5
55	1	1	0	1	1	1	1.775	1.775	3.55	3.55	3.55
56	1	1	1	0	0	0	1.8	1.8	3.6	3.6	3.6
57	1	1	1	0	0	1	1.825	1.825	3.65	3.65	3.65
58	1	1	1	0	1	0	1.85	1.85	3.7	3.7	3.7
59	1	1	1	0	1	1	1.875	1.875	3.75	3.75	3.75
60	1	1	1	1	0	0	1.9	1.9	3.8	3.8	3.8
61	1	1	1	1	0	1	1.925	1.925	3.85	3.85	3.85
62	1	1	1	1	1	0	1.95	1.95	3.9	3.9	3.9
63	1	1	1	1	1	1	1.975	1.975	3.95	3.95	3.95

Function Description

Constant-On-Time PWM Controller with input Feed Forward

The constant-on-time control architecture is a pseudo fixed frequency with input voltage feed-forward. The device will turn on the high-side MOSFET for a fixed time. When the feedback voltage is lower than the reference voltage, controller will adjust the off time to stabilize output voltage ripple. COT regulators are widely used in the industry due to their ability to provide fast transient response without complex loop compensation. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage and inversely protectional to input voltage. The on-time of PFM is written as below:

$$T_{ON\text{-}PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where:
FSW is the PWM switching frequency.

Setting the Ouptut Voltage

The APW6016E have 5 buck conveters and one 0.5A sink/soource VTT LDO. The 5 buck converter output volatge can adjust by I2C programmable. It can be set by REG02~06[5:0].

SVIN Under-voltage Lockout (UVLO)

The device contains a SVIN lockout (UVLO) circuit. The purpose of the UVLO circuit is to ensure that the SVIN high enough for reliable operation. When the SVIN falls below the under voltage threshold, the internal circuitry is turned off. If the SVIN rises by the under voltage lockout hysteresis, the device will restart. The APW6016E set different SEL pin resistor correspond to SVIN lockout threshold, V_{OUT2} and switching frequency. The SVIN lockout threshold voltage selection can refer to the below table:

SEL pin to gnd	V_{POR_R}	V_{OUT2}	F_{SW}
Floating	10.5V	1.35V	750kHz
400kΩ	10.5V	1.2V	750kHz
200kΩ	4.2V	1.35V	1.5MHz
GND	4.2V	1.2V	1.5MHz

Whether SVIN rises above the under voltage threshold or not, it can be read status by REG10[0].

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse frequ-ency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing.

Pulse-Width Modulation (PWM)

At light load condition and set up Forced-PWM function (REG02~06[7:6]), the controller will enter the Forced-PWM mode. In Forced-PWM mode, the zero-crossing comparator which truncates the low-side switch on-time at the inductor current zero crossing, is disabled. This causes low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of V_{OUT}/V_{IN}. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is MOSFET useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Ultra-sonic Modulation (USM)

At light load condition and set up USM function (REG02~06[7:6]), the controller will enter the USM mode. Audible noise and EMI can be reduced in USM mode. The switching frequency in USM mode is lower than the one in PFM/PWM mode. In USM mode, the output current capacity can't support heavy load, so controller acquires output current information to judge when to enter the PFM mode to stabilize the output voltage. In Forced-PWM mode, the zero-crossing comparator which truncates the low-side switch on-time at the inductor current zero crossing, is disabled.

Soft-start

All VRs are equipped soft-start function, when enable signal of each VR is activated, an internal soft start ramps the output voltage at a certain rate. This allows the output voltage to ramp up gradually, eliminating overshoot and excessive inrush current. The soft-start time can adjust by I2C programmable. It can be set by REG0B~0F[1:0].

Output Discharge

When any one of VR1~VR5 is shut down, both Upper and Lower MOSFETs will be turned off and an internal MOSFET with about 20 ohm (I^2C programmable) Rds-on discharges the output via its VOUT pin. The VTT also discharge the output via the output pin in shutdown mode. The all VRs output discharge function enable set by REG08.

Linear Regulator

The APW6016E provides an internal 5V VCC regulator for the internal control circuit. It is recommended to connect a 4.7uF X5R capacitor from the VCC pin to ground. Besides, It is an optiont to add zener diode (5.6V) to avoid spike voltage of VCC pin.

Function Description (Cont.)

Over Voltage Protection (OVP)

The over voltage protection circuitry monitors the output voltage to prevent the output from accidentally exceeding the desired set point. Once the output voltage exceeds typically 120% of the set point voltage the high/low side MOSFETs turn off and internal latch circuitry is activaged. This insures protection of the load damage and circuit reset is only achieved either by pulling low EN below 0.3V or cycling SVIN power off then on. When all VRs output voltage protection occurs, it can be read status by REG0A[5:0].
When the input voltage exceeds 18V (Typ.), the all VRs turn off and internal latch circuit is activage or automatic resofstart by input over voltage remove. Whether internal latch is control by REG010[2] after input OVP occur.

Over Current Protection (OCP) and Under Voltage Protection (UVP)

The each output of VRs is protected against gradual over current or sudden short on its output. When inductor current valley value exceeds the set threshold an internal over-current protection is activated which turns off the high side and low side MOSFETs. Once the output voltage drops below a typical threshold of 50% of the output set point value, both high side and low side MOSFETs turn off and an internal latch circuit is initiated.
When any of OCP or UVP is activated, the IC will be latch off. To release the latch-off is to pull low EN below 0.3V or to cycle SVIN power off then on. When the output voltage protection occurs, it can be read status by REG09[5:0].

RST Output

RST is an open-drain output, needing an external pullhigh resistor to VIN to provide the RST signal for system. The RST function is continuously monitoring the output voltage. When output voltage is greater than 90% of reference voltage and SVIN voltage exceeds the POR voltage threshold and the EN threshold exceeds 1.2V, RST will get high. When the output voltage VOUT outruns 120% (typ.) or falls below 87% (typ.) of the target output voltage and the events of uner-voltage, over-voltage, over-current, over-temper -ature, shutdown, RST signal will be pulled low immediately. When output voltage is greater than 90% of reference voltage, it can be read power ready status by REG07[5:0].

Over Temperature Protection (OTP)

A thermal shutdown function is implemented to prevent damages due to excessive heat. Typically the thermal shutdown threshold temperature is 150°C. When the thermal shutdown is triggered the device stops switching and output voltage restart after the junction temperature cools by 30°C.
When the over thermal protection occurs, it can be read status by REG09[6].

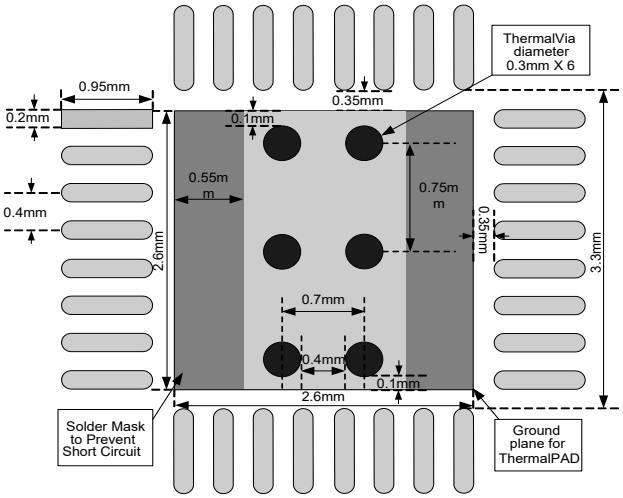
Enable/Disable

An Enable POR function is designed to preven wrong logic controls when the V_{EN} voltage is low. Pulling the V_{EN} above 1.2V will enable the driver output, and pulling V_{EN} below 0.3V will disable the driver output. If enable function is not used, connect EN to SVIN for normal operation. When the IC is disabled the supply current is reduced to less than 65μA (Typ.). The EN pin can not be left floating.

Application Information

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:



VTQFN4X4-32 Land Pattern Recommendation

1. Keep the switching nodes (BSTx, and LXx) away from sensitive small signal nodes (VOUTx).

2. Because the PGND pin signal has noise, It is connect to Thermal Pad will make APW6016E easy to interference. **Please do not connect the PGND pin of the PMIC to the thermal pad.**

3. Connect VTTIN pin to VOUT2 output capacitors' positive terminal with a short and wide trace which is capable of carrying1A. **Do NOT connect VTTIN directly to VOUT2 pin.**

4. VIN1~VIN5 and VTTIN decoupling capacitor should be put as close as possible to pins. The traces from these power supply input pins to decoupling capacitors' positive terminal should be as short as possible. The traces from PGND pins to the decoupling capacitors' negative terminal should be as short as possible.

5. Use a wide and large copper plane to connect the input capacitor PGND together with the output capacitor PGND. Keep the traces from output capacitors' negative terminal to PGND pin as short and wide as possible.

6. Use a high quality ceramic capacitor to decouple VCC. The decoupling capacitor should be close to pin.

7. Layout LXx and VINx planes as wide as possible to increase heat dissipation.

8. Put the SEL resistor and BSTx capacitors close to pins.

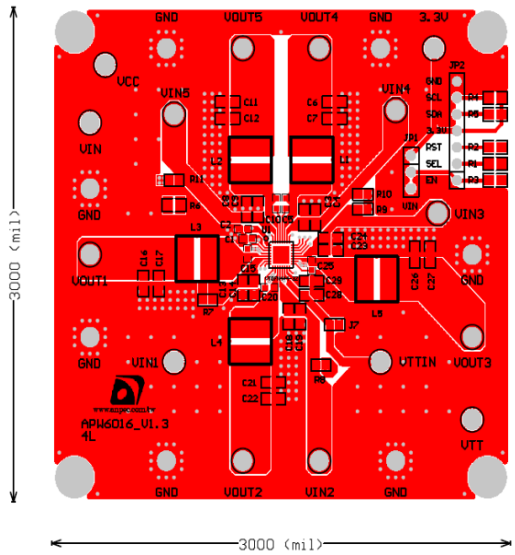
9. Connect thermal pad to a larger area of ground planes underneath with vias for proper heat dissipation.

Application Information (Cont.)

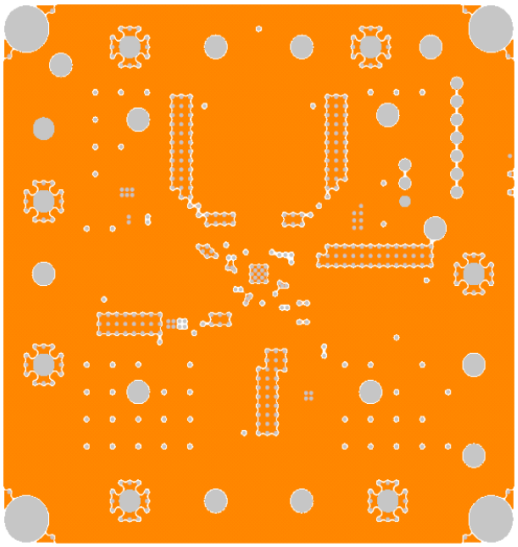
PCB Drawings

The following figures show component placement and layout of the demoboard.

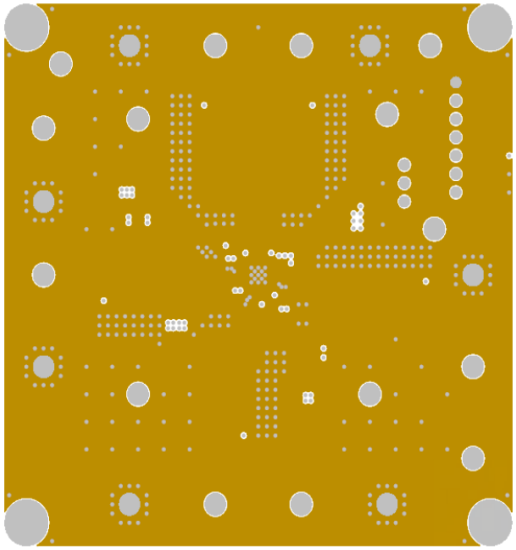
Top Side Routing



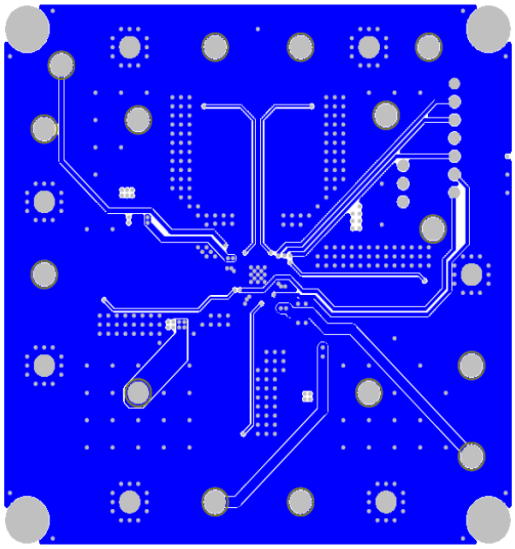
Layer 3 Routing



Layer 2 Routing

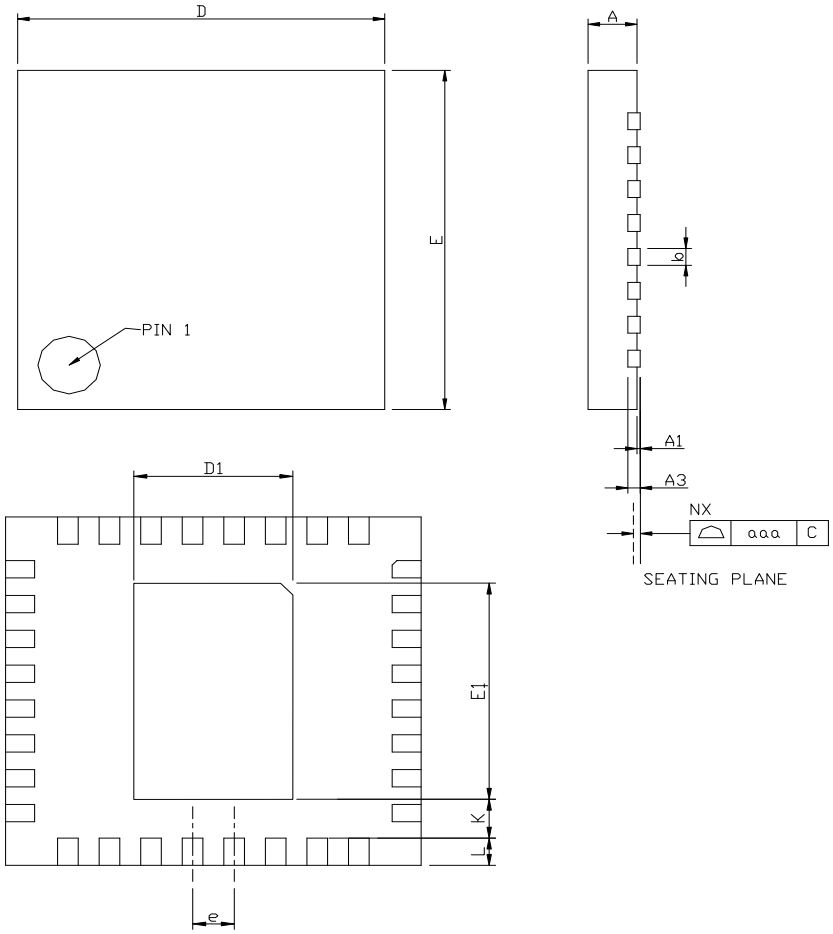


Bottom Layer Routing



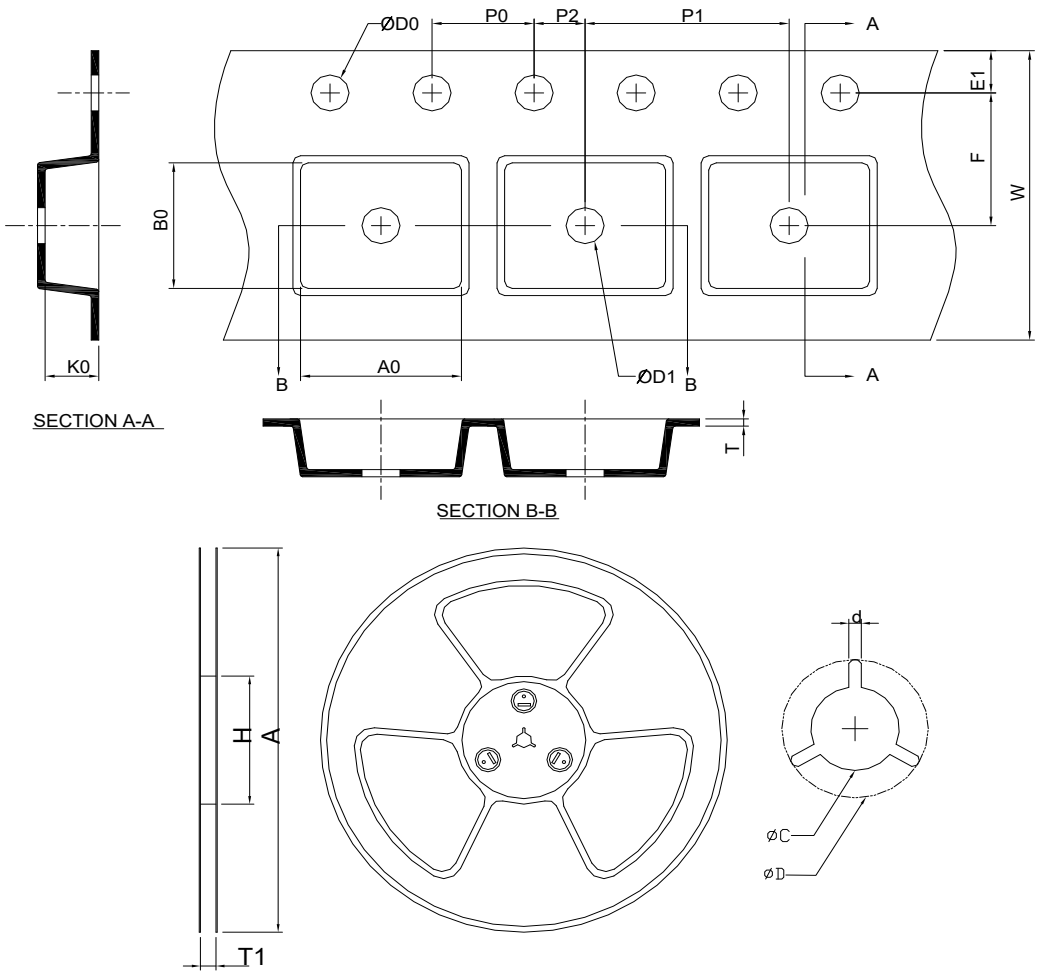
Package Information

VTQFN4x4-32



SYMBOL	VTQFN4x4-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.15	0.25	0.006	0.010
D	3.90	4.10	0.154	0.161
D1	1.2	1.4	0.047	0.055
E	3.90	4.10	0.154	0.161
E1	2.15	2.35	0.085	0.093
e	0.40 BSC		0.016 BSC	
L	0.25	0.35	0.010	0.014
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	0.75±0.20

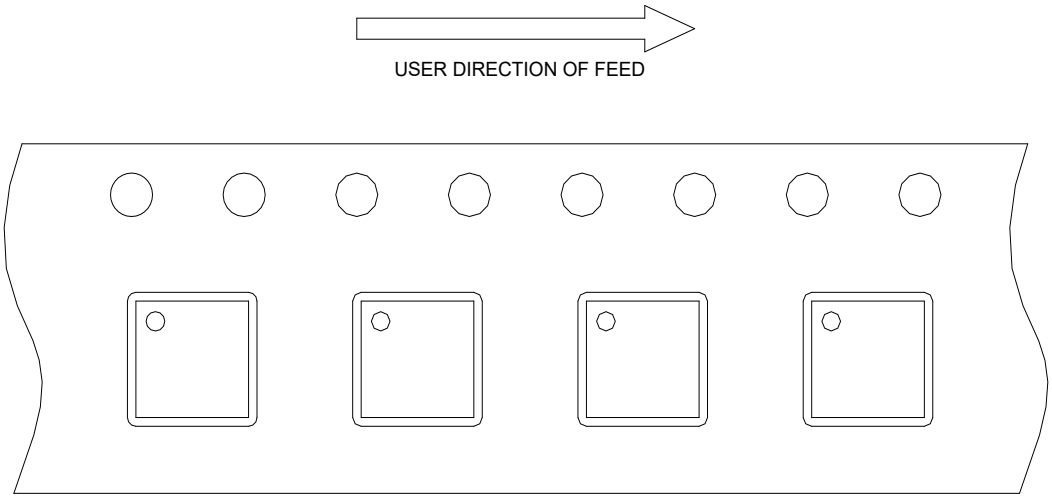
(mm)

Devices Per Unit

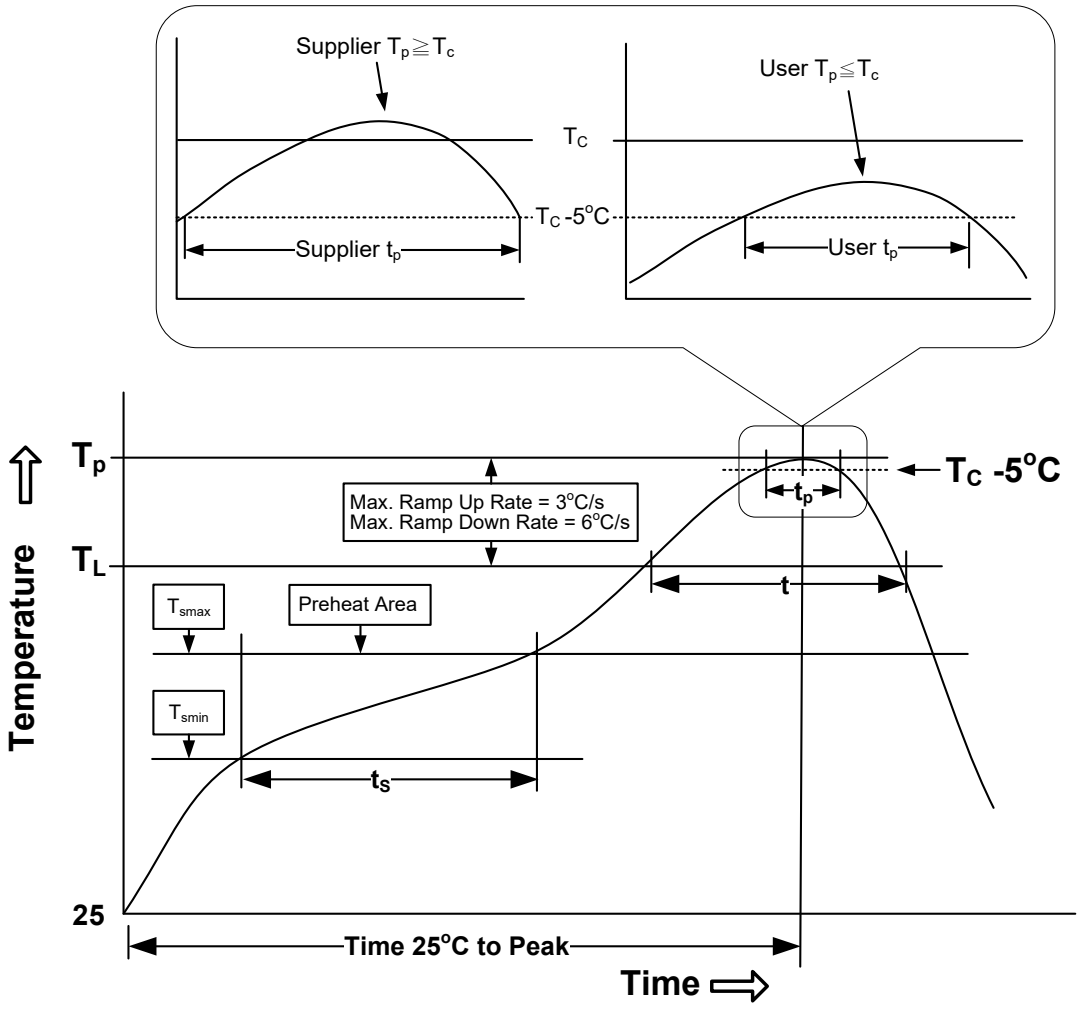
Package type	Packing	Quantity
VTQFN4x4	Tape & Reel	3000

Taping Direction Information

VTQFN4x4-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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