APW7436

3-CH Buck Converter, 4.5-18V Input Voltage, Tiny Package

Features

- **Wide Input Voltage from 4.5V to 18V**
- **2.5A/1.5A/1.5A Output Current on Channel1/2/3**
- **Low I_Q=160μA (typ.) per channel supply to improve Light Load Efficiency at Sync off**
- **Typical 0.6V ±1%Internal Reference Voltage**
- **Sync Pin Allows Synchronization to an External**
- **Clock from 500kHz to 2MHz**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **N-CH MOSFET (120 mΩ) for CH1/2/3 High Side**
  - **N-CH MOSFET (30 mΩ) for CH1 Low Side**
  - **N-CH MOSFET (50 mΩ) for CH2/3 Low Side**
- **Built in OVP, UVP, Current Limit and OTP**
- **Low Cost TQFN3x3-20A package**

General Description

The APW7436 is a three-channel synchronous mode PWM converter with 2.5A continuous current capability for one channel and 1.5A continuous current capability for the other two channels.

Although the switching frequency of the APW7436 is fixed at 600kHz, it can also change the switching frequency via the SYNC pin.

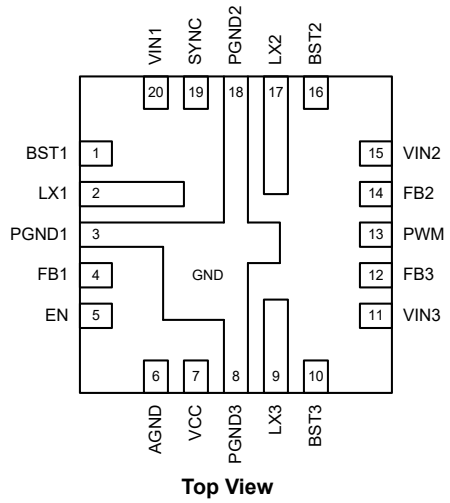
The APW7436 also provides a 120-degree phase shifting technique. to minimize switching noise. The output voltage of each channel can be adjusted using an external resistor divider. Other features include OVP, UVP, current limit, and OTP.

The APW7436 is available in a TQFN3x3-20A package with small size and excellent thermal capacity.

Applications

- **Digital Subscriber Line**
- **Passive Optical Network**
- **G.fast**
- **Set-Top-Box**

Pin Configuration



Top View

Ordering and Marking Information

APW7436 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB : TQFN3x3-20A
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Green Part

APW7436 QB :

XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN1/2/3 to PGND		-0.3 ~ 21	V
V_{LX}	LX1/2/3 to PGND	>10ns	-0.6 ~ 21	V
		<10ns	-6 ~ 24	V
V_{BS}	BST1 to LX1, BST2 to LX2, BST3 to LX3		-0.3 ~ 5.5	V
$V_{I/O}$	VCC, EN, FB1/2/3, SYNC, PWM to AGND		-0.3 ~ 6	V
V_{GND}	PGND1/2/3 to AGND		-0.3 ~ 0.3	V
PD	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
P_D	Power Dissipation @ TA=25°C (Note 2)	2.22	W
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	45	°C/W
θ_{JA}	Junction-to-Ambient Resistance (Note 3)	29.34	°C/W

Note 2: θ_{JA} is measured on 4 layers test board following the EIA/JESD51-7.
Note 3: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Range	Unit
VIN	VIN1/2/3 supply voltage		4.5 ~ 18	V
V_{EN}	EN input voltage		0 ~ 5	V
VOUT	Converter output voltage		0.6 ~ 5	V
I_{OUT}	Converter output current	CH1	0 ~ 2.5	A
		CH2	0 ~ 1.5	
		CH3	0 ~ 1.5	
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V. Typical values are at T_A=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT (for CH1, CH2 and CH3)						
I_{VIN}	VIN Input Current	V_{FB}=0.7V, LX=NC	-	160	-	μA
I_{VIN_SHDN}	VIN Shutdown Current	EN=AGND	-	-	5	μA
UNDER VOLTAGE LOCKOUT (for CH1, CH2 and CH3)						
V_{UVLO}	VCC UVLO Threshold Voltage	VCC Rising	-	4.3	-	V
V_{UVLO_HYS}	VCC UVLO Hysteresis Voltage	VCC Falling	-	0.4	-	V
T_{D_UVLO}	VCC UVLO ON Delay Time	When VCC UVLO ON to LX Switching	-	500	-	μs
EN INPUT (for CH1, CH2 and CH3)						
V_{EN_H}	EN Input Threshold High Voltage		1.2	1.4	1.6	V
V_{EN_Hys}	EN Input Hysteresis Voltage		-	0.2	-	V
$T_{DB\_EN\_OFF}$	EN Turn Off Debounce Time		-	20	-	μs
T_{D_EN}	EN Turn On Delay Time	When EN High to LX Switching	-	650	-	μs
I_{EN}	EN Input Current		-	-	0.1	μA
REFERENCE VOLTAGE (for CH1, CH2 and CH3)						
V_{REF}	Reference Voltage	T_J=25°C	594	600	606	mV
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A	-	5	-	V
	VCC Load Regulation	I_{VCC}=10mA	-	3	-	%
	VCC Maximum Current	When VCC drop to 4.75V	40	-	-	mA
t_{SS}	Soft Start Time		-	1	-	ms
R_{STOP}	Internal Soft-Stop Resistor		-	100	-	Ω
OSCILLATOR AND SYNCHRONIZATION FREQUENCY (for CH1, CH2 and CH3)						
F_{OSC}	Oscillator Frequency		-	600	-	kHz
	Frequency Accuracy	T_J=-40~125°C	-20	-	+20	%
	Minimum on Time	(Note 5)	-	70	-	ns
	Maximum Duty		-	90	-	%
F_{SYNC}	Synchronization Frequency Range		500	-	2000	kHz
V_{SYNC_H}	SYNC Input Threshold High Voltage		1.2	1.4	1.6	V
V_{SYNC_Hys}	SYNC Input Hysteresis Voltage		-	0.2	-	V

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V. Typical values are at T_A=25°C.

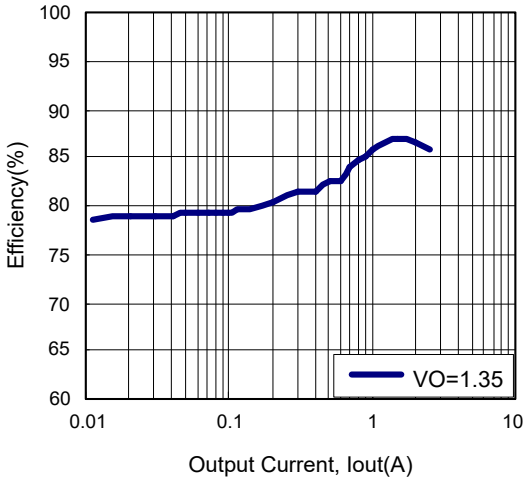
Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
POWER MOSFET (for CH1, CH2 and CH3)						
	CH1 High Side MOSFET Resistance		-	120	-	mΩ
	CH1 Low Side MOSFET Resistance		-	30	-	mΩ
	CH2 High Side MOSFET Resistance		-	120	-	mΩ
	CH2 Low Side MOSFET Resistance		-	50	-	mΩ
	CH3 High Side MOSFET Resistance		-	120	-	mΩ
	CH3 Low Side MOSFET Resistance		-	50	-	mΩ
	High Side MOSFET Leakage Current		-	1	-	μA
	Low Side MOSFET Leakage Current		-	1	-	μA
BOOTSTRAP POWER (for CH1, CH2 and CH3)						
R_{BST}	BST Switch On Resistance	BST Source 0.1A	-	10	-	Ω
	BST Leakage Current	V_{BST-LX}=5V	-	-	0.1	μA
PHASE SHIFT and Force PWM						
	CH1, CH2 and CH3 Phase Shift	(Note 5)	-	120	-	degree
V_{PWM_H}	PWM Input Threshold High Voltage	(Note 5)	1.2	1.4	1.6	V
V_{PWM_L}	PWM Input Threshold Low Voltage	(Note 5)	-	0.2	-	V
I_{PWM}	PWM Leakage Current		-	-	0.1	μA
PROTECTIONS (for CH1, CH2 and CH3)						
I_{LIM}	High Side MOSFET current-limit	For CH1	3.5	4.5	5.5	A
		For CH2	2.5	3.5	4.5	
		For CH3	2.5	3.5	4.5	
	Over-temperature Trip Point	(Note 5)	-	150	-	°C
	Over-temperature Hysteresis	(Note 5)	-	30	-	°C
	FB Over Voltage Protection	(Note 5)	120	125	130	$\%V_{REF}$
	FB Over Voltage Protection Hysteresis	(Note 5)	-	5	-	$\%V_{REF}$
	Under Voltage Protection		40	50	60	$\%V_{REF}$

Note 5: Guaranteed by design.

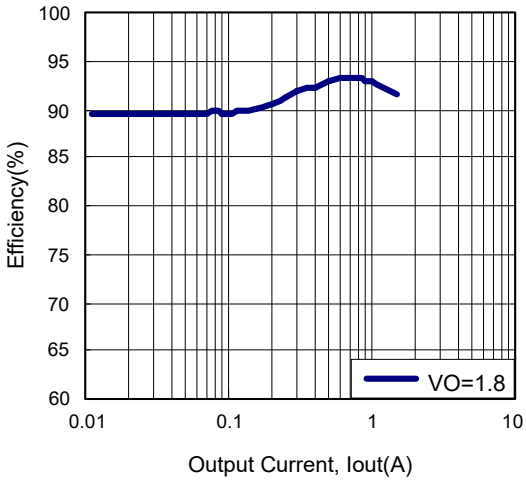
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

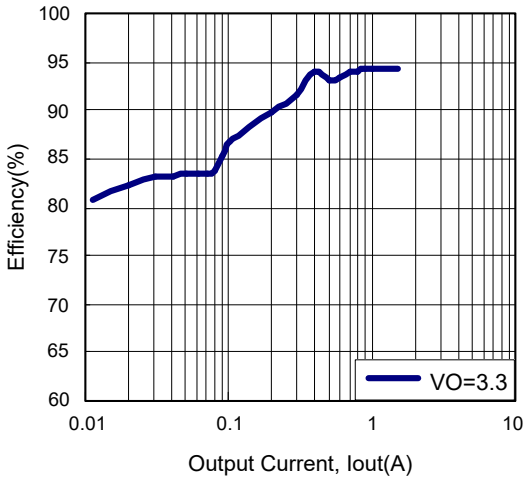
CH1 Efficiency



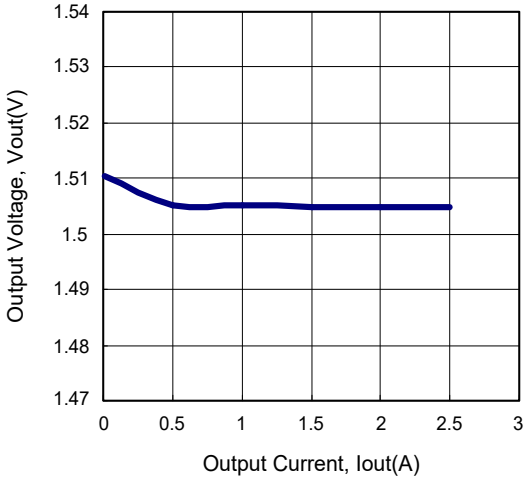
CH2 Efficiency



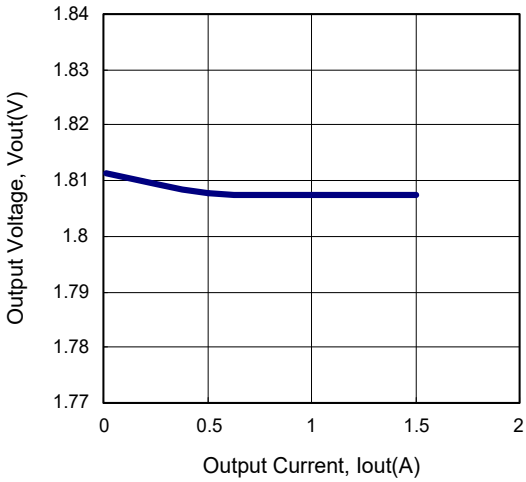
CH3 Efficiency



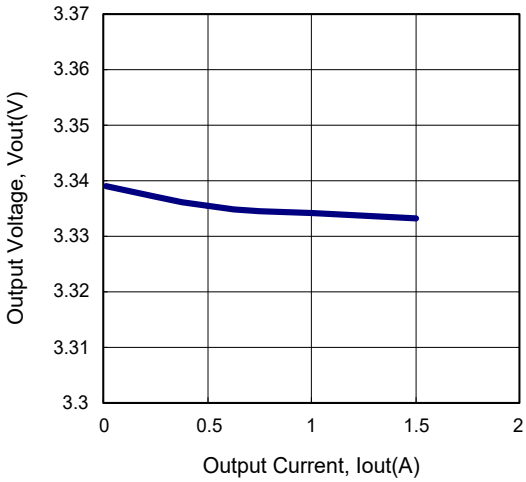
CH1 Load Regulation



CH2 Load Regulation



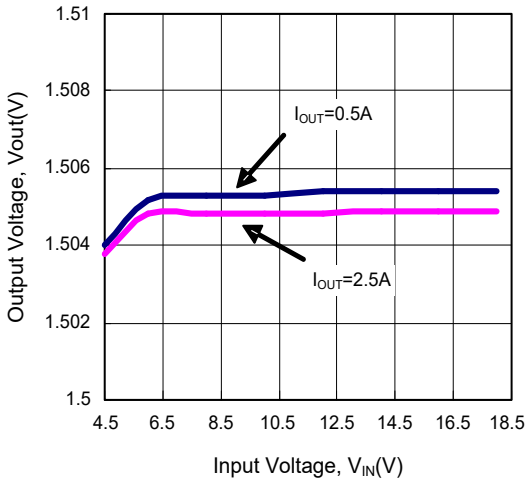
CH3 Load Regulation



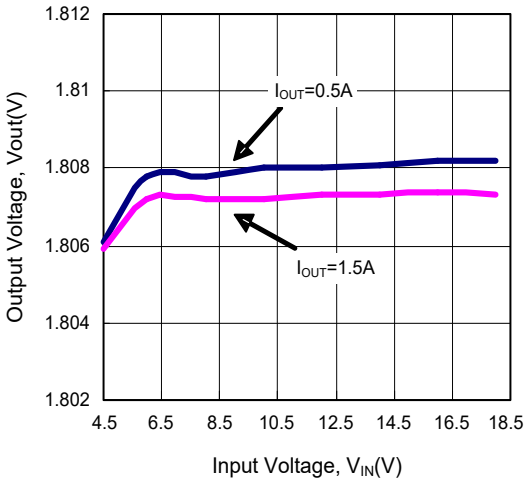
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

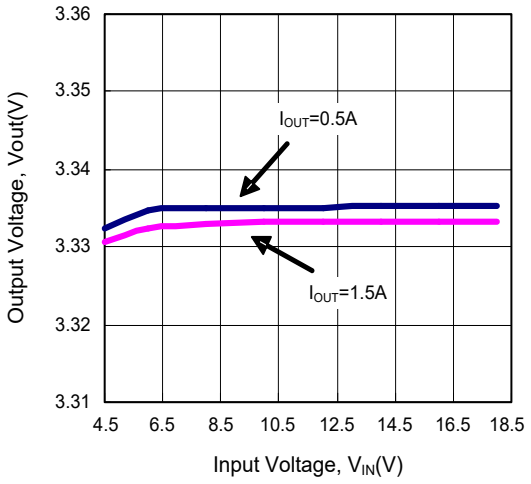
CH1 Line Regulation



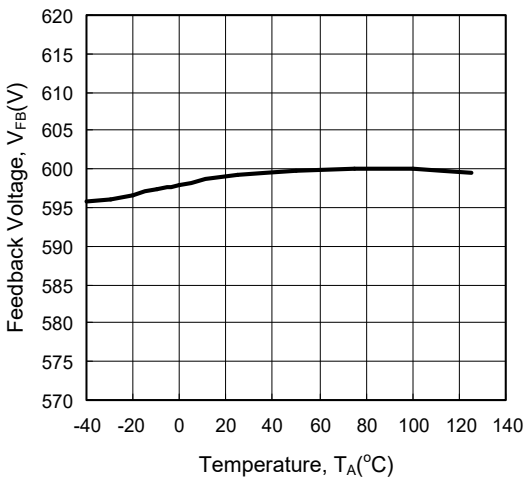
CH2 Line Regulation



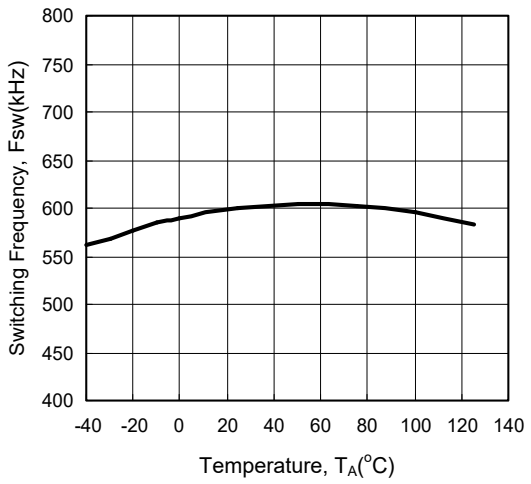
CH3 Line Regulation



Feedback Voltage vs. Temperture



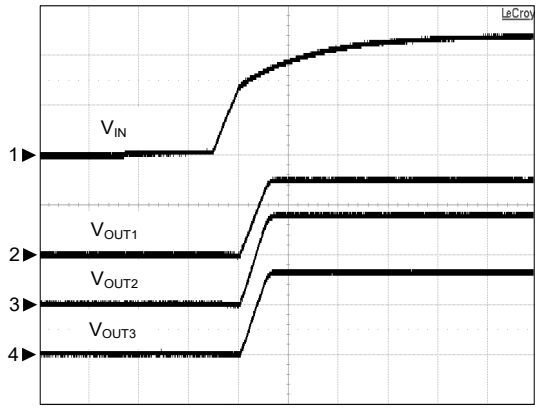
Switching Frequency vs. Temperture



Operating Waveforms

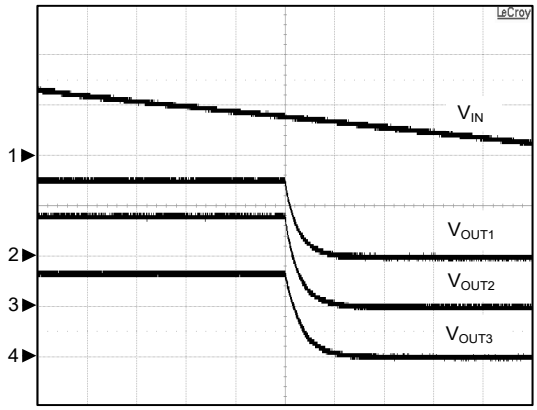
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

Power On without Loading



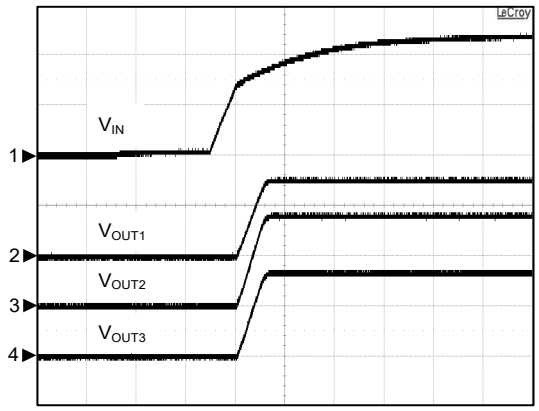
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 2ms/Div

Power Off without Loading



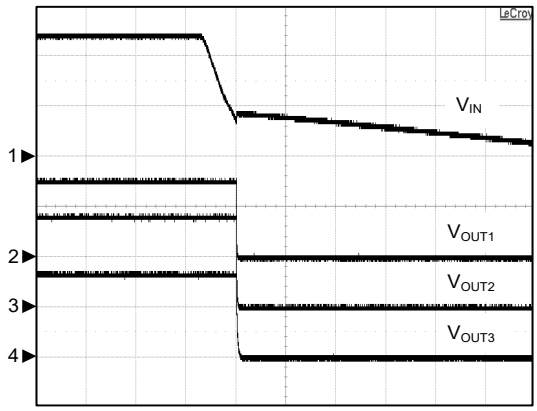
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 5ms/Div

Power On with Full Loading



CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 2ms/Div

Power Off with Full Loading

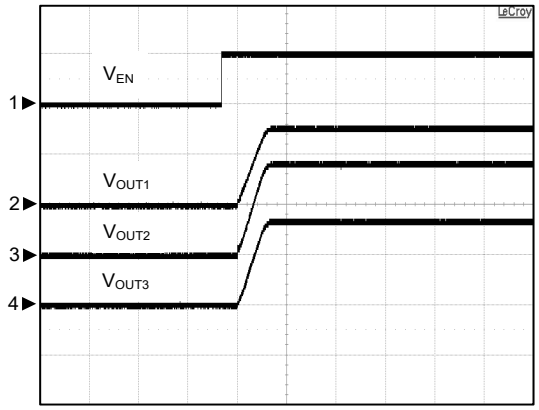


CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 5ms/Div

Operating Waveforms (Cont.)

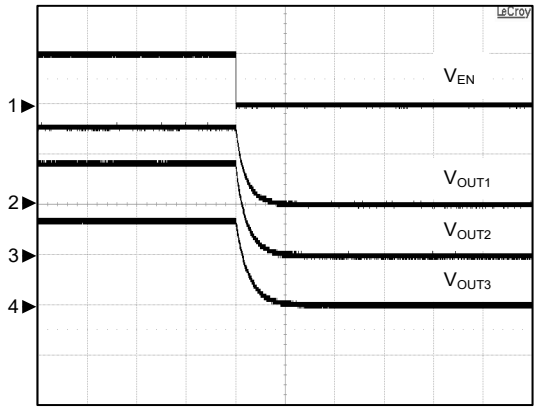
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

Enable without Loading



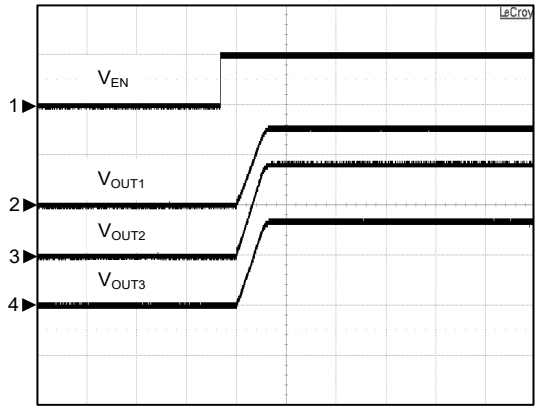
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 2ms/Div

Shutdown without Loading



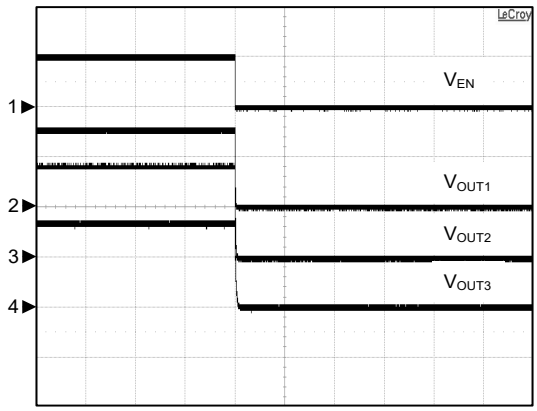
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 5ms/Div

Enable with Full Loading



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 2ms/Div

Shutdown with Full Loading

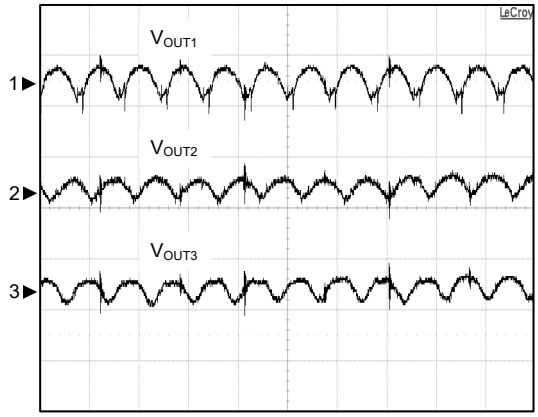


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 5ms/Div

Operating Waveforms (Cont.)

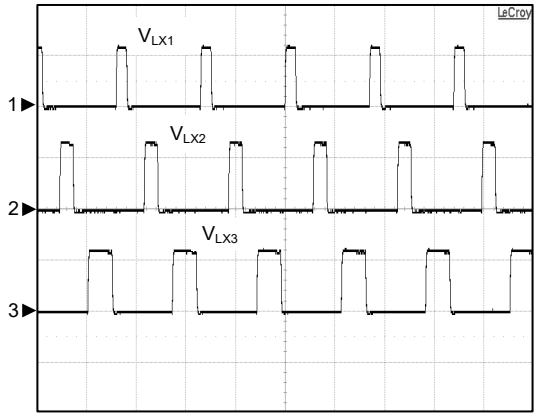
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

Normal Operation



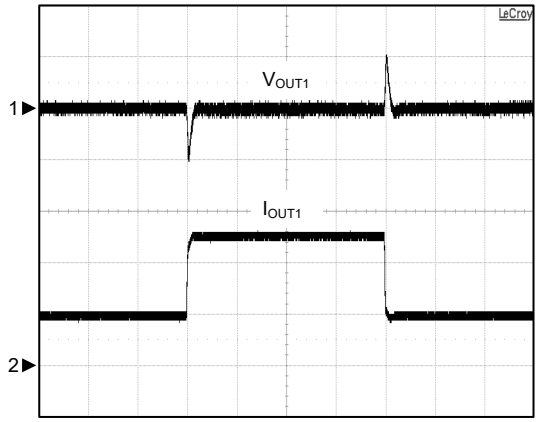
CH1: V_{OUT1}, 20mV/Div, AC
CH2: V_{OUT2}, 20mV/Div, AC
CH3: V_{OUT3}, 20mV/Div, AC
TIME: 2μs/Div

Normal Operation



CH1: V_{LX1}, 10V/Div, DC
CH2: V_{LX2}, 10V/Div, DC
CH3: V_{LX3}, 10V/Div, DC
TIME: 1μs/Div

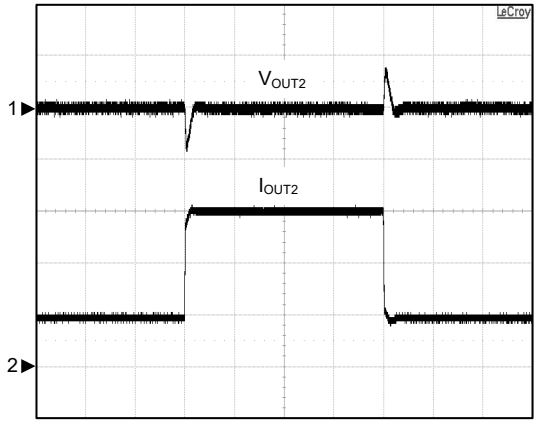
CH1 Load Transient



I_{OUT1}=1-2.5A

CH1: V_{OUT1}, 100mV/Div, AC
CH2: I_{OUT1}, 1A/Div, DC
TIME: 100μs/Div

CH2 Load Transient



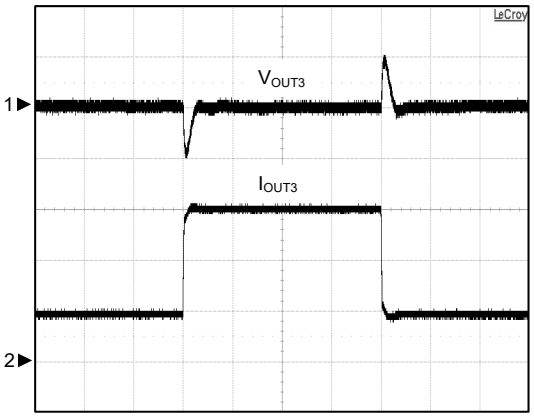
I_{OUT2}=0.5-1.5A

CH1: V_{OUT2}, 100mV/Div, AC
CH2: I_{OUT2}, 500mA/Div, DC
TIME: 100μs/Div

Operating Waveforms (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

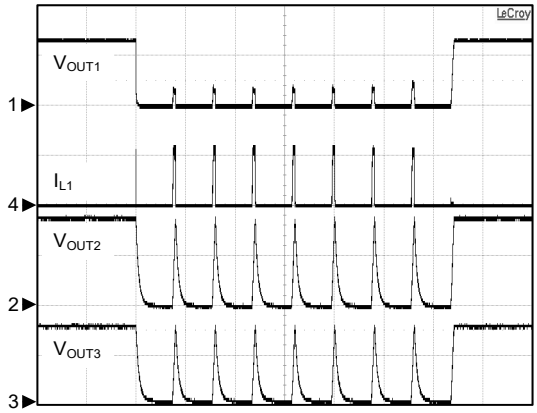
CH3 Load Transient



I_{OUT1}=0.5-1.5A

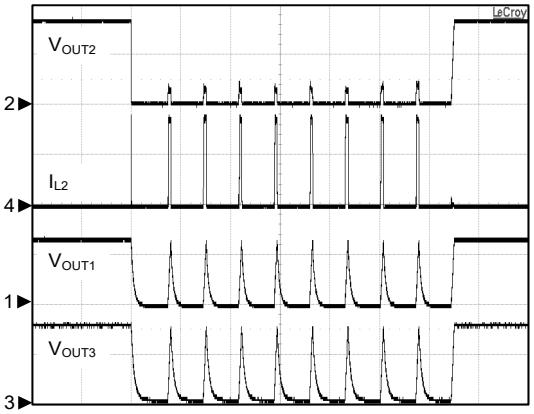
CH1: V_{OUT3}, 100mV/Div, AC
CH2: I_{OUT3}, 500mA/Div, DC
TIME: 100μs/Div

CH1 Short Circuit



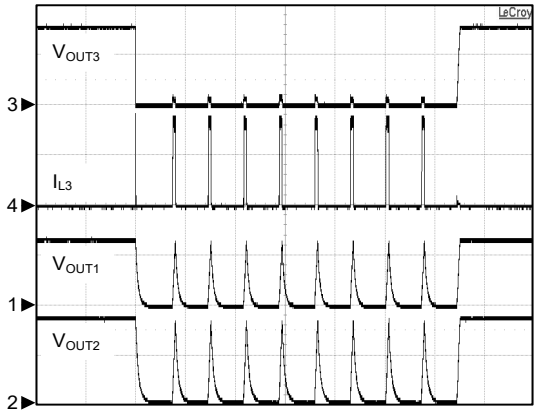
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 2V/Div, DC
CH4: I_{L1}, 4A/Div, DC
TIME: 20ms/Div

CH2 Short Circuit



CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 2V/Div, DC
CH4: I_{L2}, 2A/Div, DC
TIME: 20ms/Div

CH3 Short Circuit

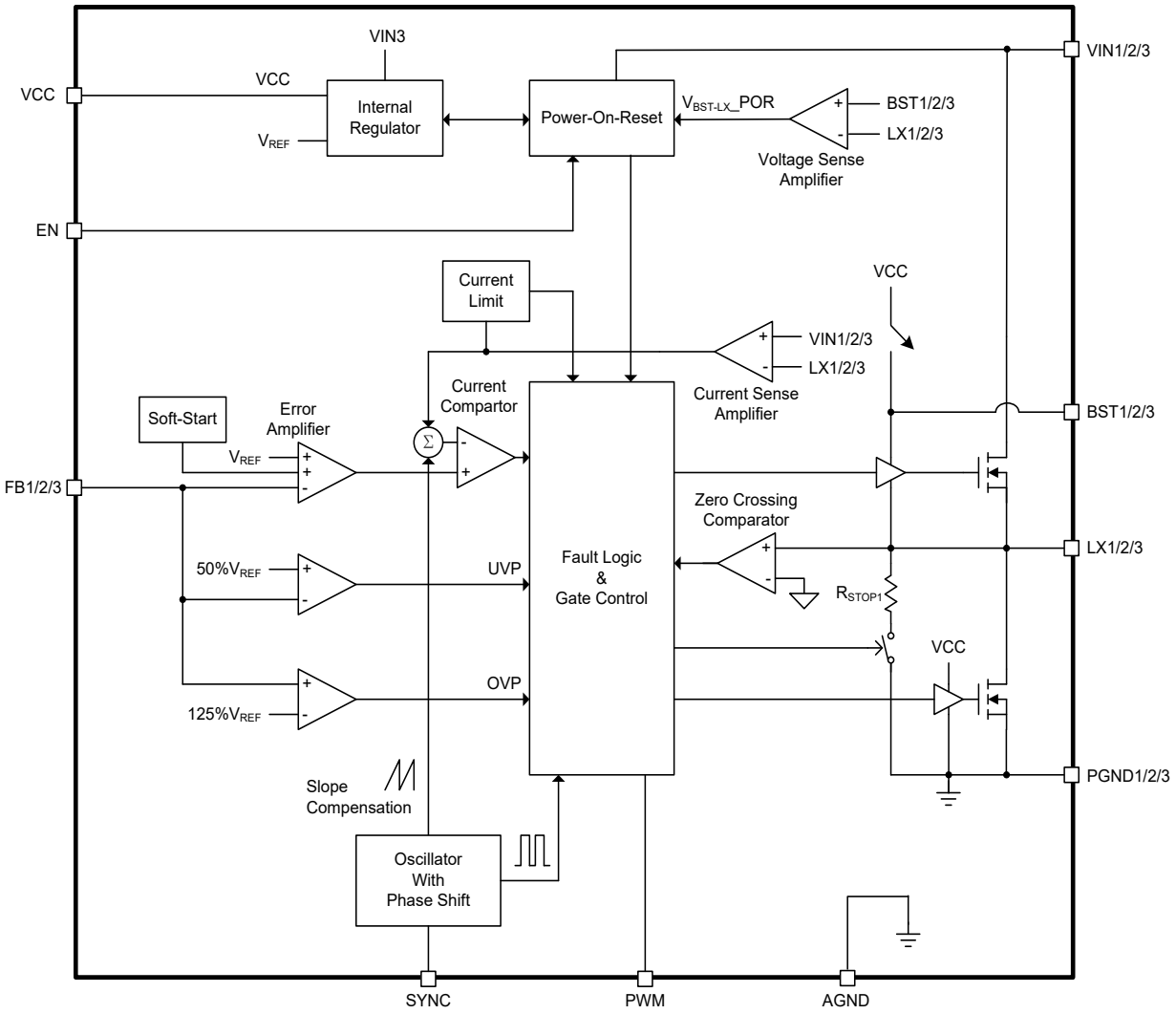


CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 2V/Div, DC
CH4: I_{L3}, 2A/Div, DC
TIME: 20ms/Div

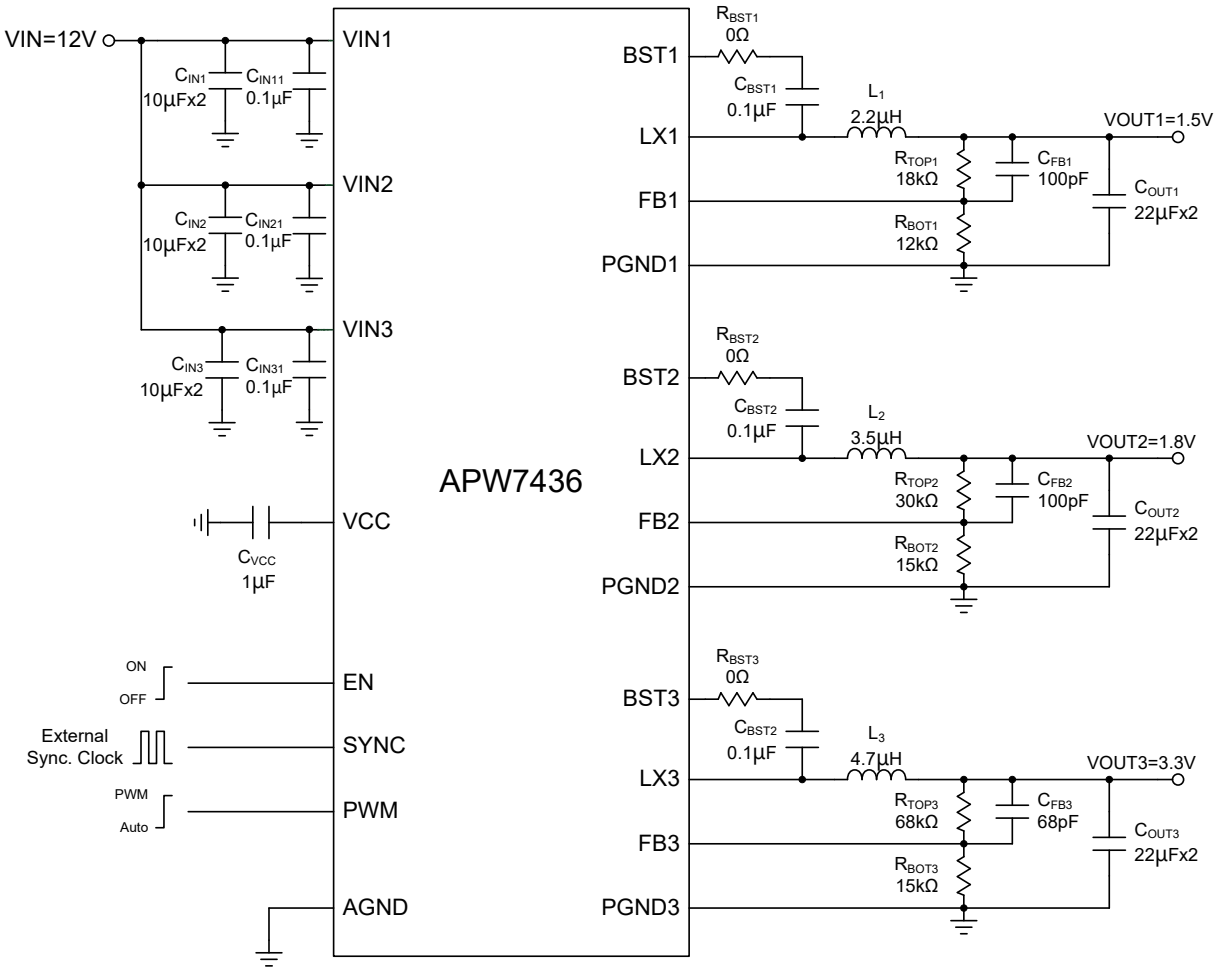
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	BST1	CH1 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX1 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
2	LX1	CH1 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
3	PGND1	CH1 Power Ground. These pins must be connected directly to the GND plane of the PCB using low inductance vias.
4	FB1	CH1 Output Feedback Pin. FB1 senses the output voltage of channel1 and regulates it. Connect the resistor divider from the output through FB1 to the ground to set the output voltage.
5	EN	Enable Input Pin. Drive EN high to turn the all converters on and drive it low to turn all converters off. The EN pin cannot be left floating.
6	AGND	The Ground of IC.
7	VCC	Internal Regulator Output Pin. The VCC pin is the output of an internal 5V regulator for internal control circuitry. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
8	PGND3	CH3 Power Ground. These pins must be connected directly to the GND plane of the PCB using low inductance vias.
9	LX3	CH3 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
10	BST3	CH3 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX3 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
11	VIN3	CH3 Power Input Pin. VIN3 supplies the power to the CH3 buck converter.
12	FB3	CH3 Output Feedback Pin. FB3 senses the output voltage of channel3 and regulates it. Connect the resistor divider from the output through FB3 to the ground to set the output voltage.
13	PWM	Force PWM Mode Enable Pin. If this pin is pulled low, the IC will operate in automatic PSM / PWM mode. If this pin is pulled high, the IC will operate in forced PWM mode.
14	FB2	CH2 Output Feedback Pin. FB2 senses the output voltage of channel2 and regulates it. Connect the resistor divider from the output through FB2 to the ground to set the output voltage.
15	VIN2	CH2 Power Input Pin. VIN2 supplies the power to the CH2 buck converter.
16	BST2	CH2 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX2 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
17	LX2	CH2 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
18	PGND2	CH2 Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
19	SYNC	Synchronous Clock Input Pin. Input an external 500kHz to 2MHz clock signal to this pin for synchronization function. If the SYNC pin is not used, it should be grounded.
20	VIN1	CH1 Power Input Pin. VIN1 supplies the power to the CH1 buck converter.

Block Diagram



Typical Application Circuit



Components Selection for Different Output Voltage

Application	Channel	VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
1	1	12	1.5	0 ~ 2.5A	10µ × 2	2.2µ	22µ × 2	18k	12k	100pF
	2	12	1.8	0 ~ 1.5A	10µ × 2	3.5µ	22µ × 2	30k	15k	100pF
	3	12	3.3	0 ~ 1.5A	10µ × 2	4.7µ	22µ × 2	68k	15k	68pF
2	1	12	5	0 ~ 2.5A	10µ × 2	4.7µ	22µ × 2	110k	15k	68pF
	2	12	1.5	0 ~ 1.5A	10µ × 2	2.2µ	22µ × 2	18k	12k	100pF
	3	12	1.2	0 ~ 1.5A	10µ × 2	1.5µ	22µ × 2	15k	15k	100pF
3	1	12	3.3	0 ~ 2.5A	10µ × 2	4.7µ	22µ × 2	68k	15k	68pF
	2	12	2.5	0 ~ 1.5A	10µ × 2	3.5µ	22µ × 2	51k	16k	68pF
	3	12	1	0 ~ 1.5A	10µ × 2	1.5µ	22µ × 2	10k	15k	100pF
4	1	12	1.2	0 ~ 2.5A	10µ × 2	1.5µ	22µ × 2	15k	15k	100pF
	2	12	5	0 ~ 1.5A	10µ × 2	6.8µ	22µ × 2	110k	15k	68pF
	3	12	1.35	0 ~ 1.5A	10µ × 2	1.5µ	22µ × 2	15k	12k	100pF

Function Descriptions

MainControl Loop

The IC uses current mode control to regulate the output voltage.
The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier.
The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage.
The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VCC Regulator

The IC provides an internal 5V VCC regulator for the internal control circuitry. The VCC regulator is powered by the VIN1 voltage. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation.

VCC Under Voltage Lockout (UVLO)

VCC is an internal voltage regulator that is activated when the IC is powered by VIN3.
The APW7436 continuously monitors the voltage on the VCC pin. The soft start is activated when the VCC voltage and the EN voltage are above their respective UVLO thresholds.
VCC UVLO is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC UVLO also has hysteresis to resist ripple on the VCC voltage.

Enable/Shutdown

The IC provides the EN pin, which is a digital input that turns all the converters (CH1, CH2 and CH3) on or off. Drive EN high to turn the converter on and drive it low to turn it off.

External frequency synchronization

Although the switching frequency of the IC is fixed at 600kHz, it can also change the switching frequency via the SYNC pin.
When an external clock is input to the SYNC pin, the IC can synchronize the switching frequency of the converter with the external clock frequency, which can be synchronized from 500 Hz to 2 MHz.

Single Frequency and Phase shift

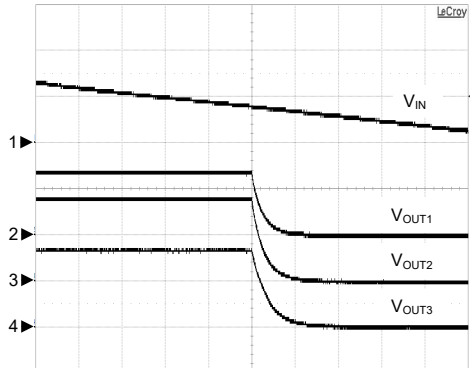
The IC has three converters that use the same operating frequency to avoid beat frequencies and improve noise immunity.
But it also increases input current and EMI, so more input capacitors and additional EMI components must be used. Therefore, the IC provides a 120-degree phase shifting technique that allows three high-side power MOSFETs to be turned on at different times to eliminate these defects. It will greatly reduce the RMS input current, resulting in less input capacitance, EMI components and input losses.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Fast Discharge

When the EN signal goes low or the VCC voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered.
The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.
The following figure shows the Vout1=1.5V, Vout2=1.8V and Vout3=3.3V without load then shut down, we can see the output can be fully discharged within 8ms.



CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{OUT3}, 2V/Div, DC
TIME: 5ms/Div

Function Descriptions (Cont.)

Current Limit and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.

When the current limit protection is activated, the output current will be limited and the output voltage will drop. When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode. In hiccup mode, the converter will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the overcurrent condition is removed, the IC will exit the hiccup mode.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.

When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature.

The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Over-Voltage Protection (OVP)

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.

Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.

Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.

The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.

A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to Typical Application Circuit. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

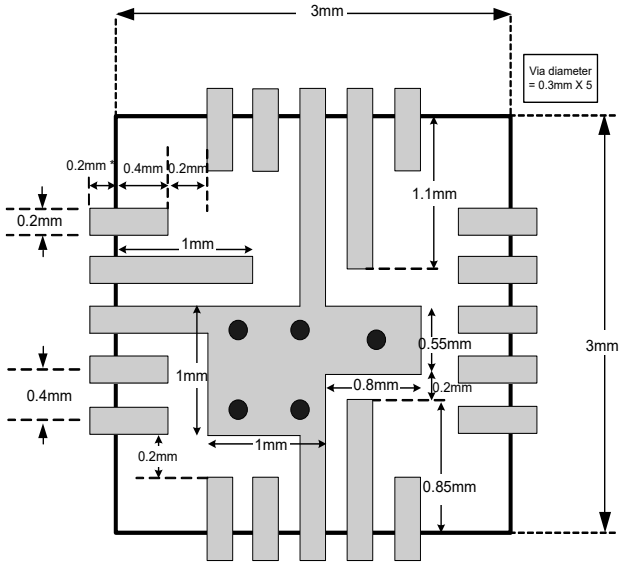
Application Information (Cont.)

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/ PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/ PGND to capacitor less than 2mm respectively is recommended.
2. Place the VCC capacitor to VCC pin and AGND pin as close as possible.
3. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
4. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
5. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
6. For better heat dissipation, it is highly recommended to place a large ground plane under the thermal pad of all PCB layers and place as many vias as possible on the thermal pad from the top layer to the bottom layer.
7. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

Recommended Minimum Footprint (Top View)



* Just Recommend

Thermal Consideration

It highly recommends all customers to keep the maximum junction temperature under 125°C in continuous operation. The junction temperature can be calculated by following formula.

$T_J=T_A + P_D \times \theta_{JA}$
T_J: Junction temperature of APW7436
T_A: Operated ambient temperature
P_D: APW7436 power dissipation (not include inductors loss)
θ_{JA}: Junction to ambient thermal resistance

APW7436 is an optimized solution for thermal dissipation. By following the PCB layout recommendation provided in datasheet, customer can reach θ_{JA} to only 30°C/W.
For a standard TQFN3*3 θ_{JA} is around 45°C/W.

For example:
Case 1:
θ_{JA} is 30°C/W, T_A is 50°C and maximum junction temperature <125°C,
The maximum power dissipation of APW7436 will be.
$P_{D\,(MAX)}$=(125°C - 50°C) / (30°C/W)=2.5W

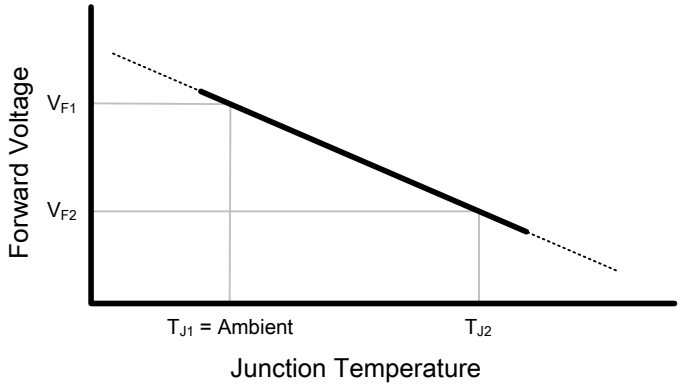
Case 2:
θ_{JA} is 45°C/W, T_A is 50°C and maximum junction temperature<125°C,
The maximum power dissipation of APW7436 will be.
$P_{D\,(MAX)}$=(125°C - 50°C) / (45°C/W)=1.67W

Application Information (Cont.)

Thermal Information Measurement

Thermal characteristics table provides the thermal dissipation's ability of the device on the evaluation board following the layout consideration. The θ_{JA} is mainly dependent on the PCB layout design, the value followed the standard of JESD51 is hard to use to estimate the junction temperature in the real application.

Therefore, when testing on the Anpec's evaluation board, a method by measuring forward voltage (V_F) of diode is used to monitor junction temperature (T_J). As shown in the figure below, the relationship between T_J and V_F is nearly linear.



The relationship between T_J and V_F can also be expressed equation as:

$T_J = m \times V_F + T_O$

Where
T_J= junction temperature in °C
m= slope in °C/Volt
V_F= forward voltage drop
T_O= intercept in °C

Therefore, with this equation, the junction temperature can be acquired by having the corresponding forward voltage drop V_F.

The method to know the relationship between T_J vs V_F is introducing below. First of all, puts the EVB in a chamber with still air, and connects the internal diode to the outside multi-meter. Normally, the body diode of Power Good FET can be used. Or if any pin pulls low or fixed a low voltage would not affect the normal application, their ESD diode can be used to measure the die temperature as well. Secondly, heat the ambient temperature to a specific point and record the corresponding VF. Because thermal equilibrium is important for minimizing the error, make sure T_{case} and $T_{ambient}$ are very close. Forward voltage should be stable at that moment.

The results will be more accurate with more test data because the real curve of temperature sensitive parameter is not perfectly linear.

Once the relationship between T_J and V_F is known, it can be used to measure the actual junction temperature by knowing V_F with various conditions, such as different operating power, environment temperature, or packaging way.

$\theta_{JA} = (T_J - T_A)/P_D$

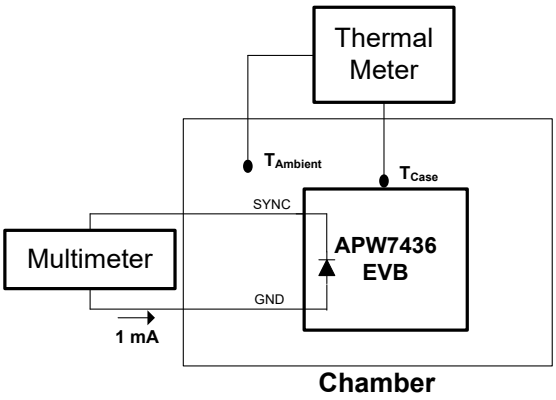
With the actual junction temperature, the thermal resistance θ_{JA} is easy to calculate by equation above. The device power dissipation is given by:

$P_D = (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT}) - (L_{AC\_LOSS} + L_{DC\_LOSS})$

L_{AC_LOSS} and L_{DC_LOSS} can be calculated from the inductor vendor's website.

Application Information (Cont.)

Setup for measuring forward voltage

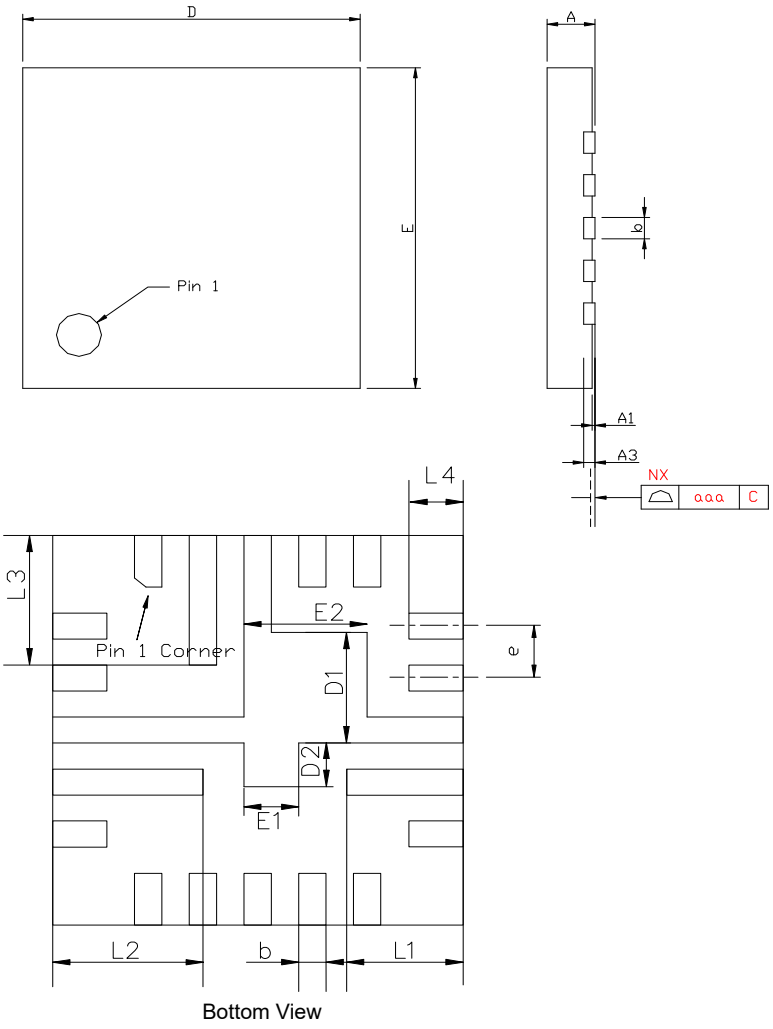


For the APW7436 EVB, the ESD diode of the SYNC pin (from the GND pin to the SYNC) can be used to measure the die temperature. It will not affect normal application when pulling low to SYNC pin. The current provided from multi-meter is 1mA, which is exactly the most suitable value that JEDEC suggests in JESD51-1. Test current 1mA is large enough to obtain a reliable forward voltage reading not influenced by surface leakage but small enough not to cause significant self heating.

The detail measurement result can refer “ANPEC Thermal Test Report”.

Package Information

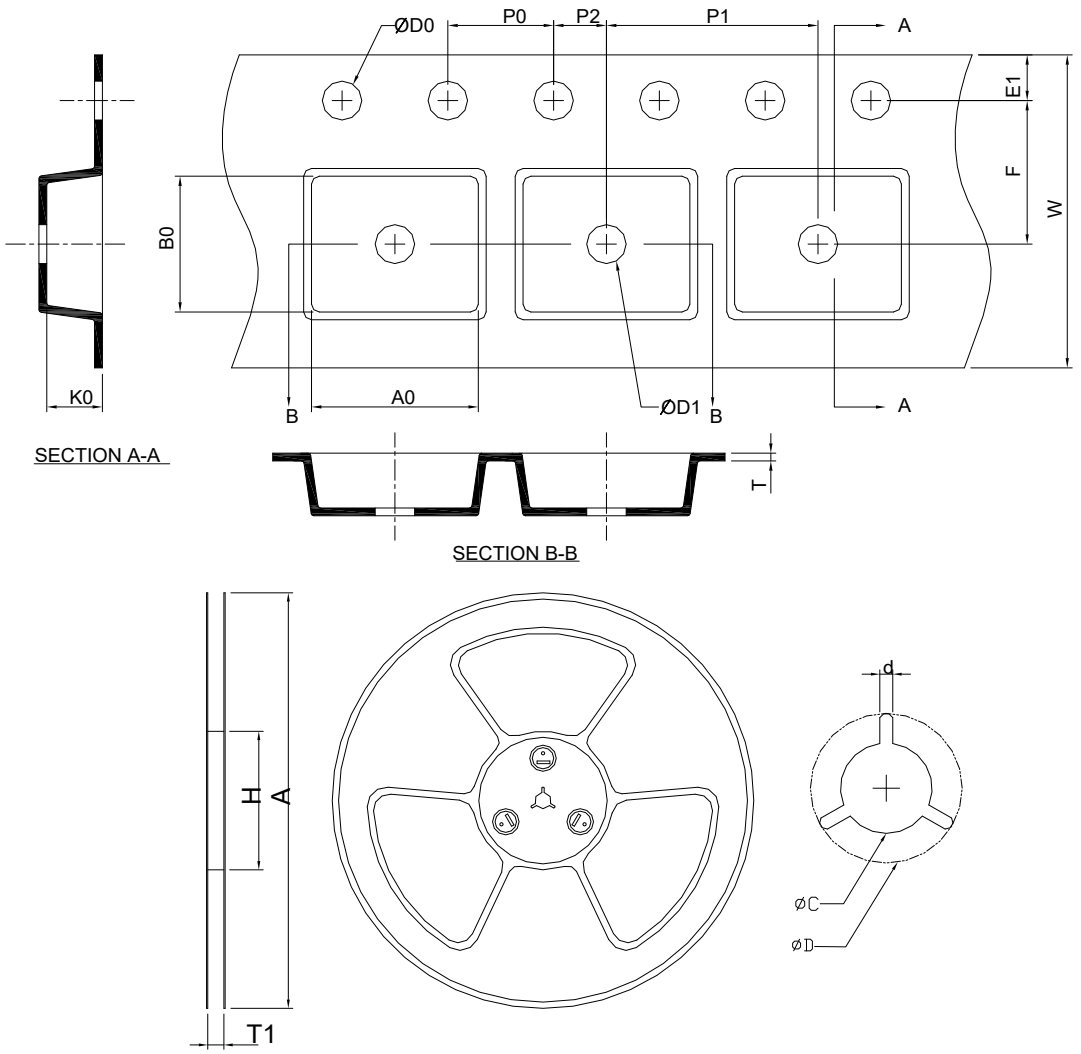
TQFN3x3-20A



Bottom View

SYMBOL	TQFN3*3-20A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D1	0.75	0.95	0.030	0.037
D2	0.275	0.375	0.011	0.015
E	2.90	3.10	0.114	0.122
E1	0.30	0.50	0.012	0.020
E2	0.75	0.95	0.030	0.037
e	0.40 BSC		0.016 BSC	
L1	0.75	0.95	0.030	0.037
L2	1.00	1.20	0.039	0.047
L3	0.90	1.10	0.035	0.043
L4	0.30	0.50	0.012	0.020
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

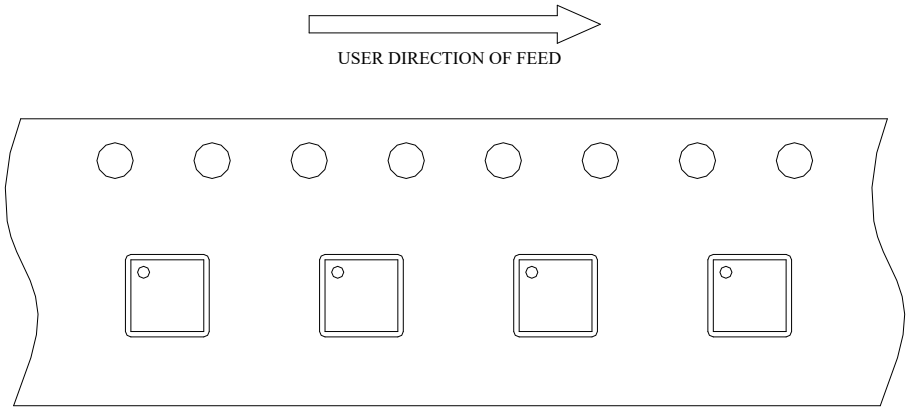
(mm)

Devices Per Unit

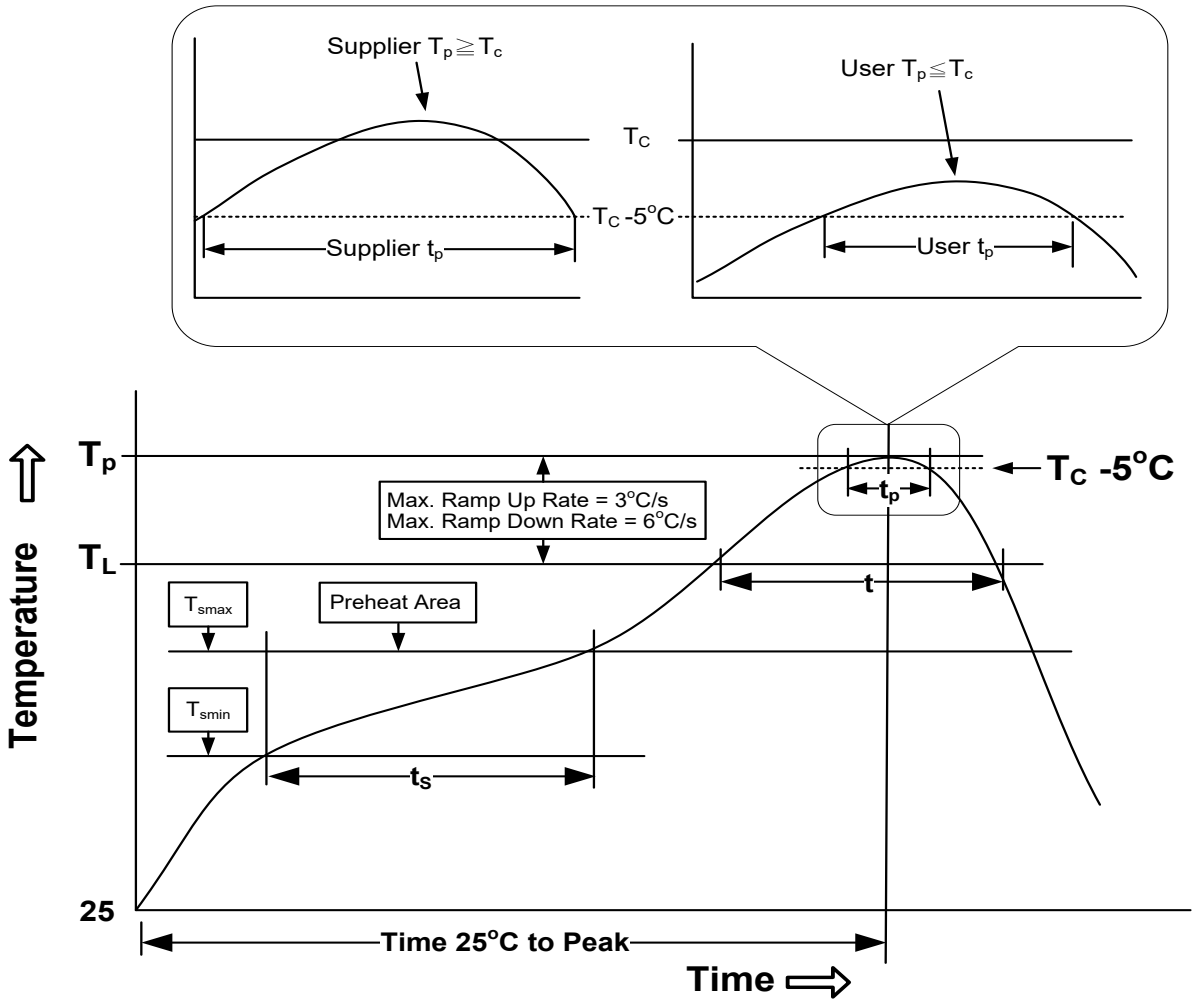
Application	Packing	Devices Per Reel
TQFN3x3	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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