

Features

- Wide Input Voltage from 2.7V to 5.5V
- Programmable LED Source Current up to 1.37A per 10mA/step
- Programmable LED Source Current Slew Rate 10mA/0.5 μ s to 10mA/64 μ s
- Bypass Mode for Standby Mode
- 40 μ A Operation Standby Current
- Programmable Ramp-up Time for IR-LED Current
- Support Dimming Frequency up to 5KHz
- 1MHz/2MHz Selectable Switching Frequency
- I²C Interface
- Short Circuit and Thermal Shutdown Protection
- Available in WLCSP-9 (1.42mm $\times$ 1.42mm) and TQFN-9 (1.8mm $\times$ 1.8mm) Packages

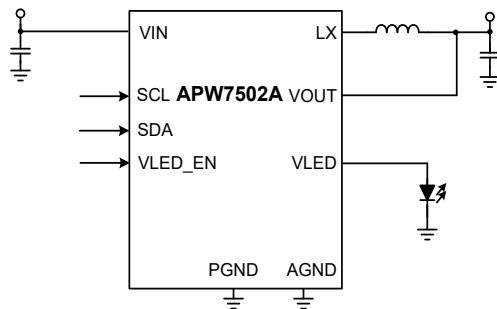
General Description

The APW7502A is a 5V/1.37A, 2MHz buck converter with a 7-bit current DAC to provide a well regulated current source for VCSEL and IR_LED applications. Through I²C interface, the start-up slew rate of the current source can be 8-segment adjustable and the regulated level can be adjusted too from 100mA to 1.37A in 10mA resolution.

When the buck converter output is overloaded or short circuited, the device limits the current at a safety level to prevent catastrophic failure. The over-temperature protection shuts down the device when junction temperature reaches 150°C and will automatically resume operating when junction temperature cools down by 20°C.

The cathode of the flash LED is referenced to GND, which improves thermal performance. The device is available in two package options: WLCSP-9 (1.42mm $\times$ 1.42mm) and TQFN-9 (1.8mm $\times$ 1.8mm).

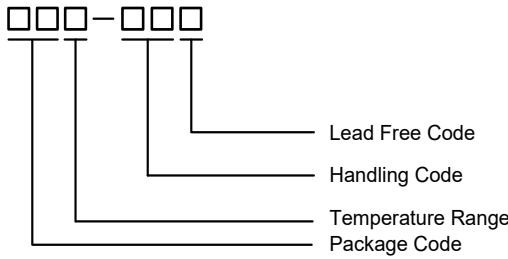
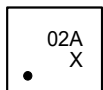
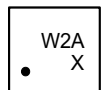
Simplified Application Circuit



Applications

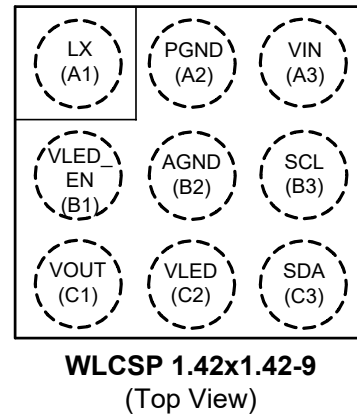
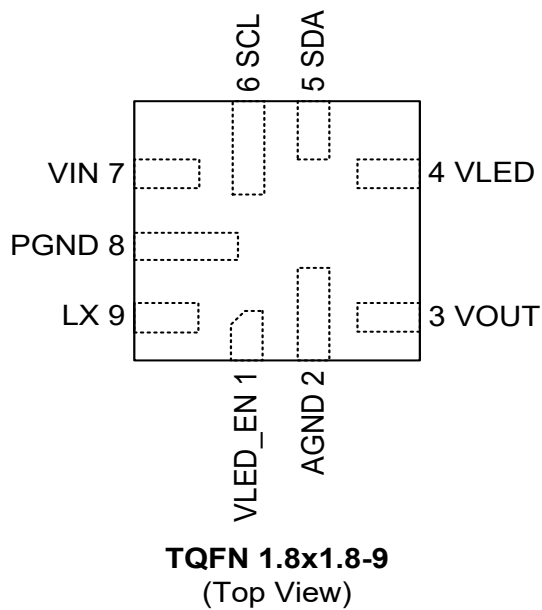
- IR-LED Driver
- VCSEL Driver

Ordering and Marking Information

APW7502A 	Package Code QB : TQFN 1.8x1.8-9 HA : WLCSP 1.42x1.42-9 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW7502A QB :  X - Date Code	APW7502A HA :  X - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration (Note 1)



Note 1: If you choose WLCSP package, please prevent IR-LED illumination on the package body.

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to PGND	-0.3 ~ 7	V
V_{LX}	LX to PGND >20ns Pulse Width <20ns Pulse Width	-0.3 ~ $V_{IN}+0.3$ -3 ~ 8	V
Other Pins	VOOUT, VLED, SCL, SDA, and VLED_EN to PGND Voltage	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 2: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 3) TQFN 1.8x1.8-9 WLCSP 1.42x1.42-9	120 165	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN to GND Voltage	2.7 ~ 5.5	V
I_{OUT}	Converter Output Current	0 ~ 1.37	A
L1	Converter Output Inductor	1 ~ 2.2	μH
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}=5V$, and $T_A=25^{\circ}C$.

Symbol	Parameter	Test Conditions	APW7502A			Unit
			Min.	Typ.	Max.	
Supply Current						
I _{IN}	V _{IN} Shutdown Supply Current	I ² C active, VLED_EN=Low	-	40	60	μA
Power-On-Reset (POR)						
V _{IN_POR}	V _{IN} POR Threshold Voltage	V _{IN} Rising	-	2.5	-	V
	V _{IN} POR Hysteresis Voltage	V _{IN} Falling	-	150	-	mV
Power Switch						
F _{SW}	Switching Frequency	PWM Mode Register 0x03: 0000 0000	1.5	2	2.5	MHz
	High-side FET On-Resistance	I _{LX} =0.5A	-	150	180	mΩ
	Low-side FET On-Resistance	I _{LX} =0.5A	-	80	100	mΩ
D _{MAX}	Maximum Converter's Duty		-	-	100	%
VLED_EN Input						
V _{LED_EN_H}	VLED_EN Input Logic High		1.5	-	-	V
V _{LED_EN_L}	VLED_EN Input Logic Low		-	-	0.4	V
	Pull down resistance at VLED_EN pin	VLED_EN=5V	-	400	-	kΩ
LED Driver						
I _{LED}	Flash Current Setting	Register 0x00: 0010 1000	475	500	525	mA
V _{OL}	Current Source Headroom Voltage	ILED Source Current=1A at T _A =25°C	-	200	-	mV
t _{RU}	ILED Ramp-up Time	ILED Source Current at 10mA/step (Note 5) Register 0x01: 0000 0000	-	0.5	-	μs
		ILED Source Current at 10mA/step (Note 5) Register 0x01: 0000 0111	-	64	-	μs
t _{RD}	ILED Ramp-down Time	ILED Source Current at 10mA/step (Note 5)	-	0.5	-	μs
Protection						
I _{LIM}	High-side FET switch current limit	Register 0x04:0000 0000	1.7	2	2.3	A
T _{OTP}	Thermal Shutdown Threshold	T _J Rising (Note 5)	-	150	-	°C
	Thermal Shutdown Hysteresis	T _J Falling (Note 5)	-	20	-	°C

Note 5: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VIN}=5V$, and $T_A=25^{\circ}C$.

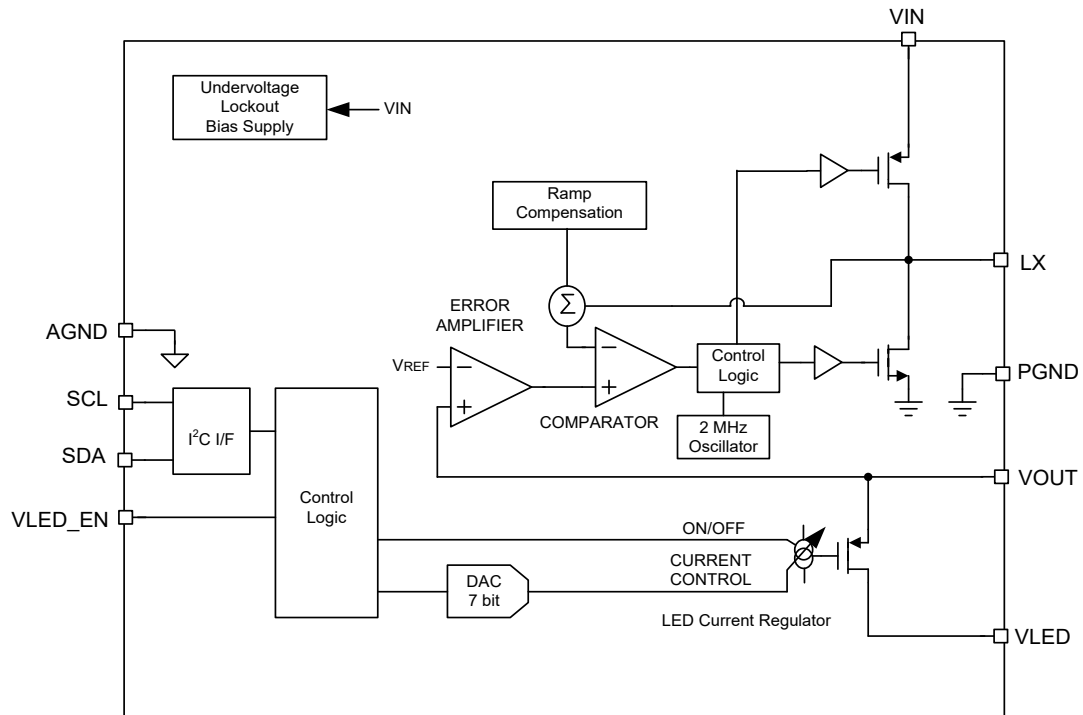
Symbol	Parameter	Test Conditions	APW7502A			Unit
			Min.	Typ.	Max.	
I ² C INTERFACE (Recommended Operating Conditions)						
	Input Capacitance	SDA, SCL (Note 5)	-	5	-	pF
V _{IL}	Input Low Voltage	SDA, SCL (Note 5)	-	-	0.5	V
V _{IH}	Input High Voltage	SDA, SCL (Note 5)	1.5	-	-	V
F _{SCL}	SCL Frequency	(Note 5)	-	-	400	kHz
t _{HIGH}	SCL High Time	(Note 5)	600	-	-	ns
t _{LOW}	SCL Low Time	(Note 5)	1300	-	-	ns
t _R	SDA, SCL Rise Time	C _{BUS} =Total Bus Line Capacitance (pF) (Note 5)	20+	-	300	ns
			10xC _{BUS}			
t _F	SDA, SCL Fall Time	C _{BUS} =Total Bus Line Capacitance (pF) (Note 5)	20+	-	300	ns
			10xC _{BUS}			
t _{HD:STA}	START Hold Time	10% of SDA to 90% of SCL (Note 5)	600	-	-	ns
t _{SU:STA}	START Setup Time	(Note 5)	600	-	-	ns
t _{HD:DAT}	Data Input Hold Time	(Note 5)	100	-	-	ns
t _{SU:DAT}	Data Input Setup Time	(Note 5)	100	-	-	ns
t _{SU:STO}	STOP Setup Time	(Note 5)	600	-	-	ns
t _{BUF}	Bus Free Time	(Note 5)	1300	-	-	ns
	Input Spike Suppression	SDA, SCL (Note 5)	-	-	50	ns

Note 5: Guarantee by design, not production test.

Pin Descriptions

PIN			Function
TQFN NO.	WLCSP NO.	NAME	
1	B1	VLED_EN	Enable input pin. Driving this pin to logic high enables the device.
2	B2	AGND	Ground for internal circuitry.
3	C1	VOUT	Buck converter's feedback pin. Connect this pin to the output of buck converter for voltage regulation.
4	C2	VLED	Current source output pin to drive external LED(s). Connect the anode of LED(s) to LED pin.
5	C3	SDA	I ² C Interface.
6	B3	SCL	
7	A3	VIN	Power supply input pin for internal circuitry and power stage.
8	A2	PGND	Ground for power stage.
9	A1	LX	Switching node of buck converter.

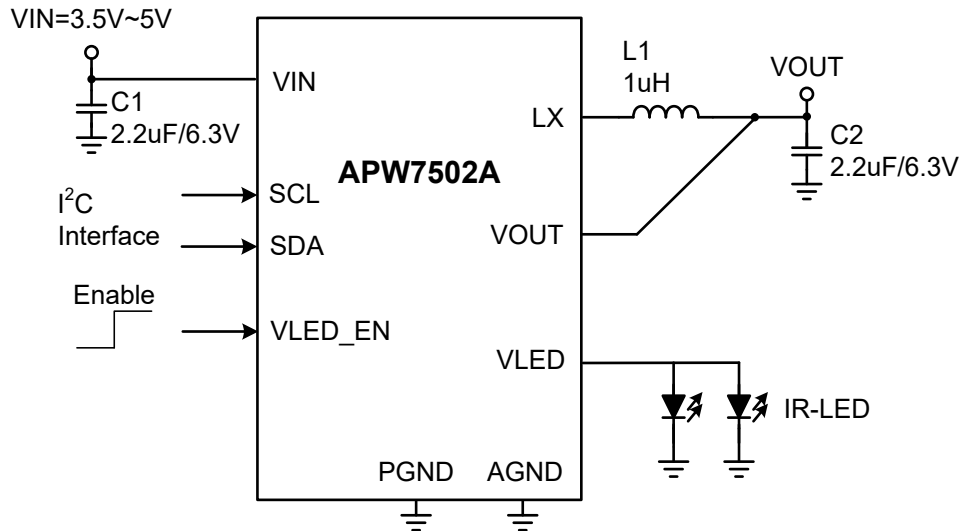
Block Diagram



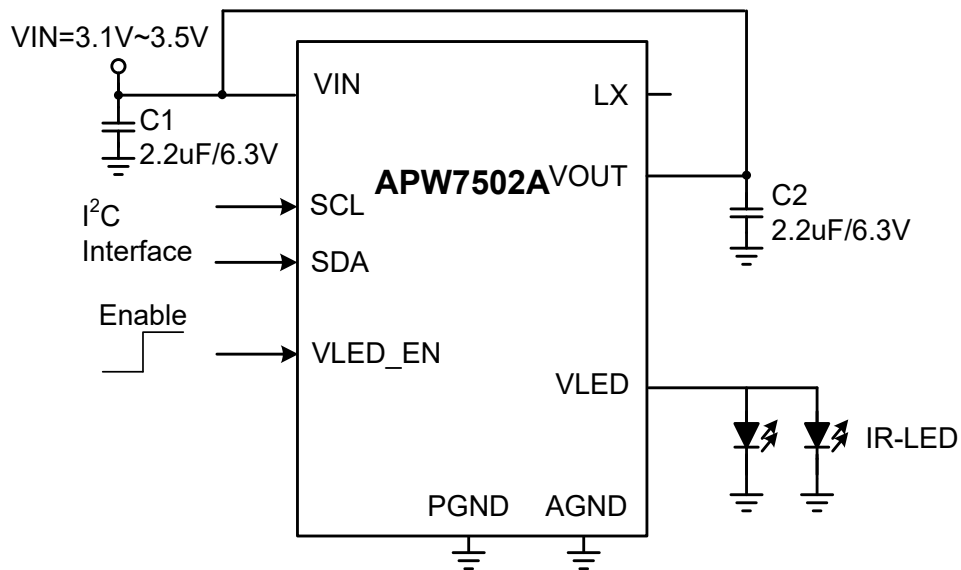
Typical Application Circuit

1. For IR-LED application

1.1 Buck Mode: $V_{IN} - 0.5V \geq V_F(\text{IR-LED})$



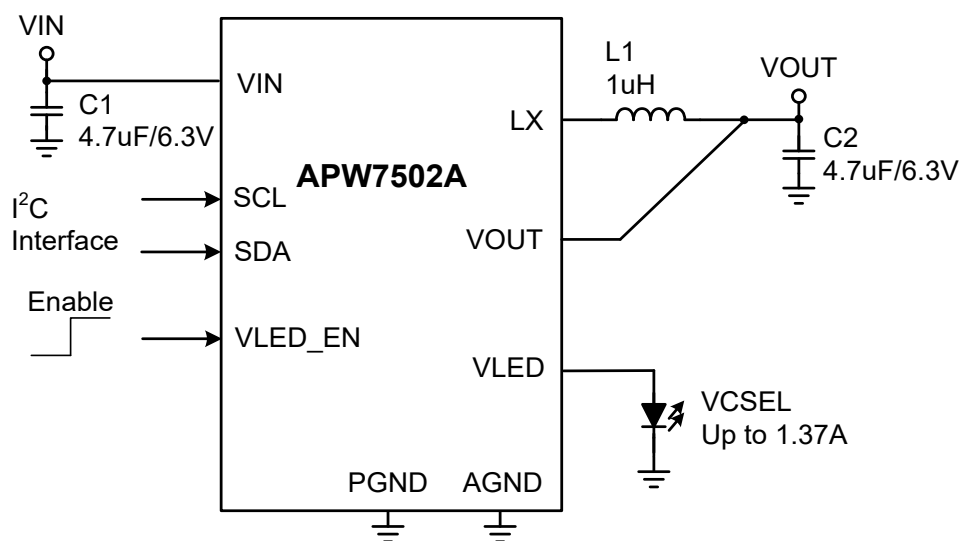
1.2 Bypass Mode: $V_{IN} - 0.2V \geq V_F(\text{IR-LED})$



Reference	Description	Manufacturer
C1,C2	2.2uF, 6.3V, X5R, 0201 size, GRM033R60J225ME47	Murata
IR-LED	LTE-R28206AS-Q-LP	LiteON

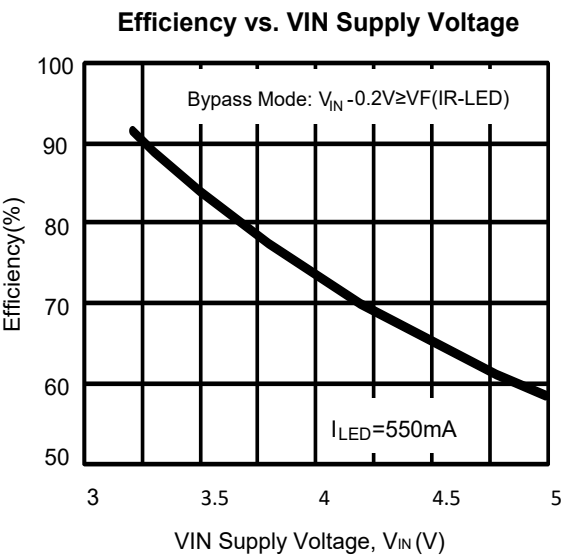
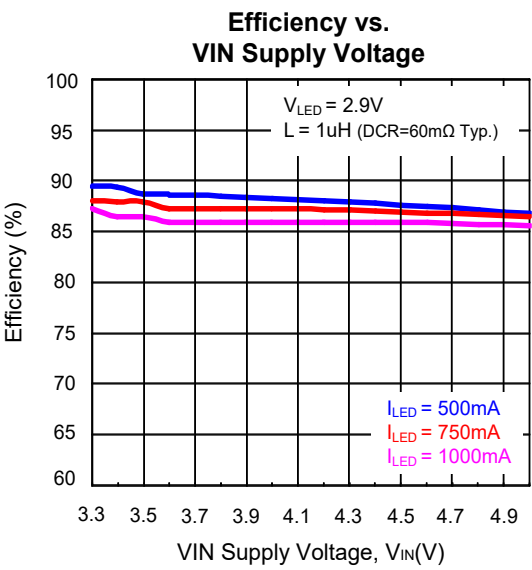
Typical Application Circuit (Cont.)

2. For VCSEL application



Reference	Description	Manufacturer
C1,C2	4.7uF, 6.3V, X5R, 0201 size, GRM033R60J225ME47	Murata

Typical Operating Characteristics

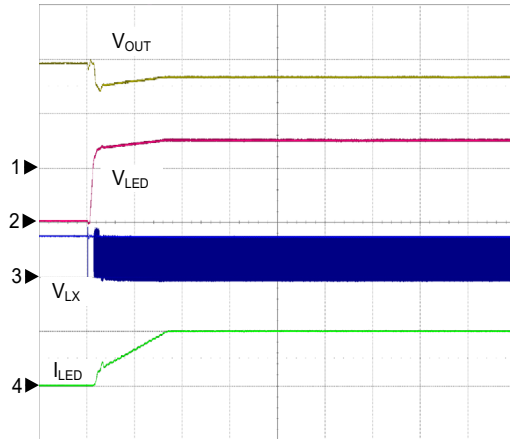


Operating Waveforms

Refer to the typical application circuit 1.1. The test condition is $V_{IN}=3.7V$, $I_{LED}=500mA$, $T_A=25^{\circ}C$ unless otherwise specified.

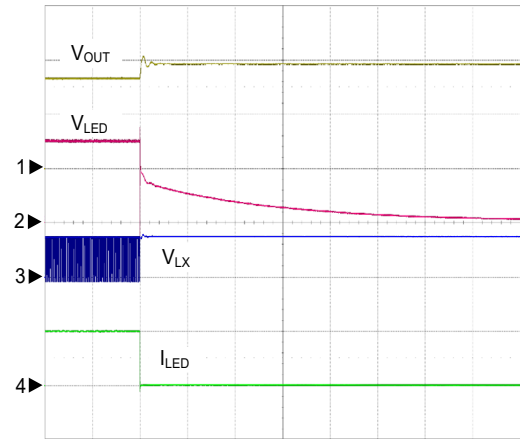
1.1 Buck Mode ($V_{IN}=3.7V$, $I_{LED}=500mA$)

I_{LED} Ramp-up at 4us Slew Rate



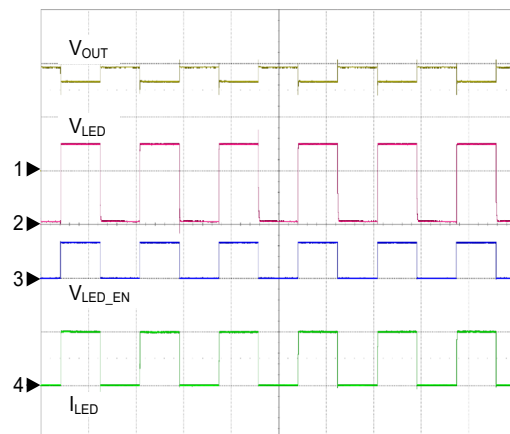
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LX} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

I_{LED} Ramp-down at 0.5us Slew Rate



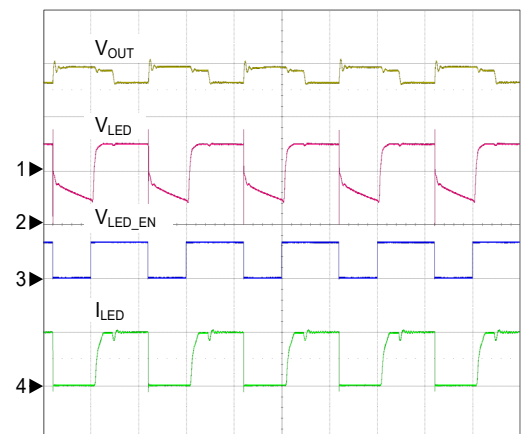
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LX} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 50 μ s/Div

Dimming, 30Hz at 50% duty



I_{LED} Ramp-up Time 10mA/4 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 20ms/Div

Dimming, 5KHz at 60% duty



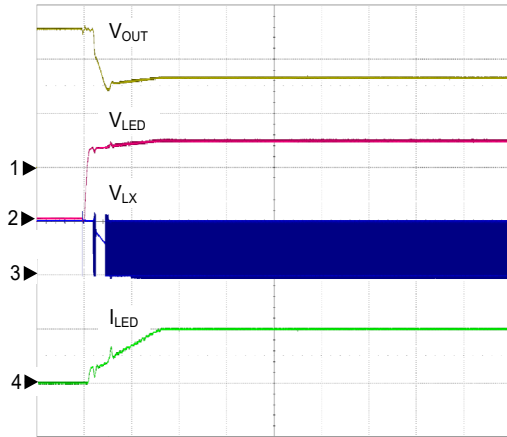
I_{LED} Ramp-up Time 10mA/0.5 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

Operating Waveforms (Cont.)

Refer to the typical application circuit 1.1. The test condition is $V_{IN}=5V$, $I_{LED}=500mA$, $T_A=25^{\circ}C$ unless otherwise specified.

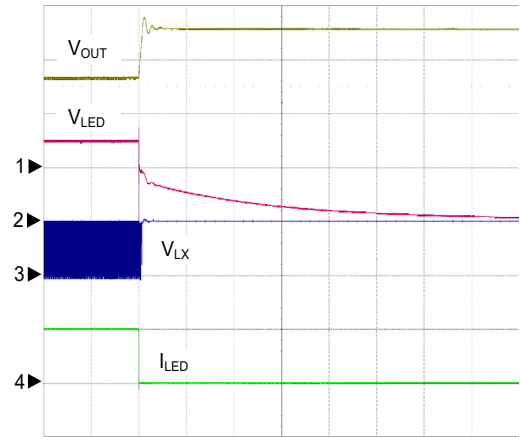
1.1 Buck Mode ($V_{IN}=5V$, $I_{LED}=500mA$)

I_{LED} Ramp-up at 4us Slew Rate



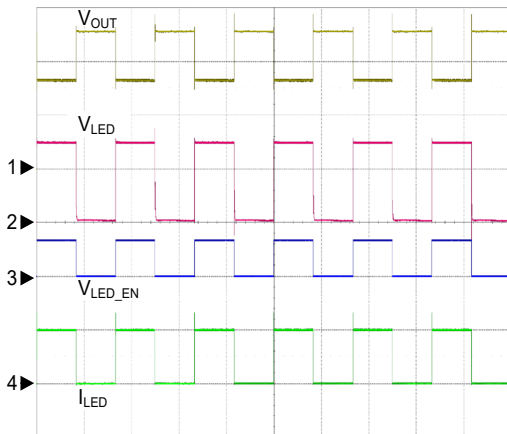
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LX} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

I_{LED} Ramp-down at 0.5us Slew Rate



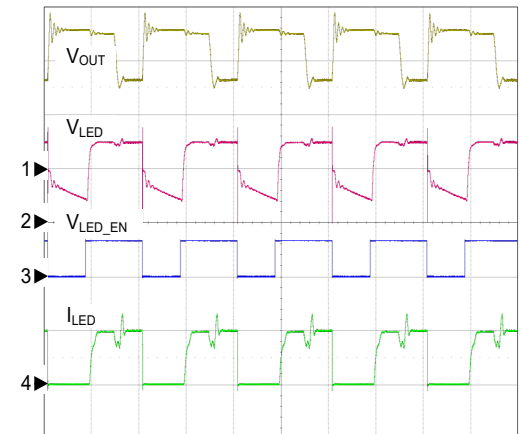
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LX} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 50 μ s/Div

Dimming, 30Hz at 50% duty



I_{LED} Ramp-up Time 10mA/4 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 20ms/Div

Dimming, 5KHz at 60% duty



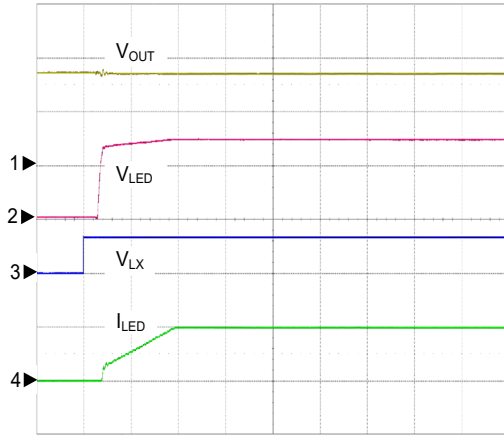
I_{LED} Ramp-up Time 10mA/0.5 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

Operating Waveforms (Cont.)

Refer to the typical application circuit1.2. The test condition is $V_{IN}=3.7V$, $I_{LED}=500mA$, $T_A=25^{\circ}C$ unless otherwise specified.

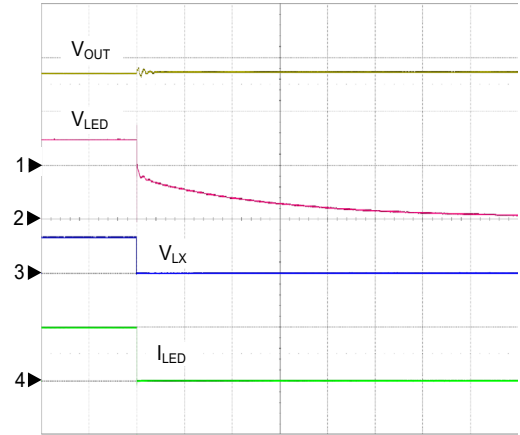
1.2 Bypass Mode ($V_{IN}=3.7V$, $I_{LED}=500mA$)

I_{LED} Ramp-up at 4us Slew Rate



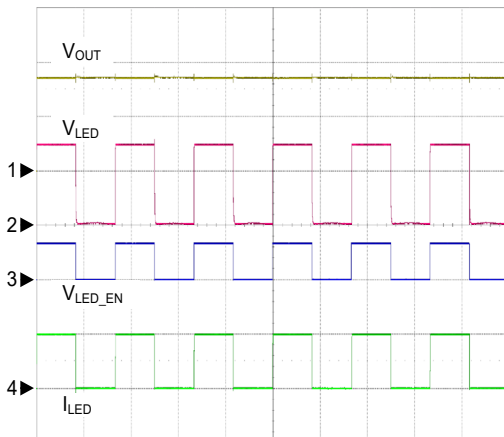
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

I_{LED} Ramp-down at 0.5us Slew Rate



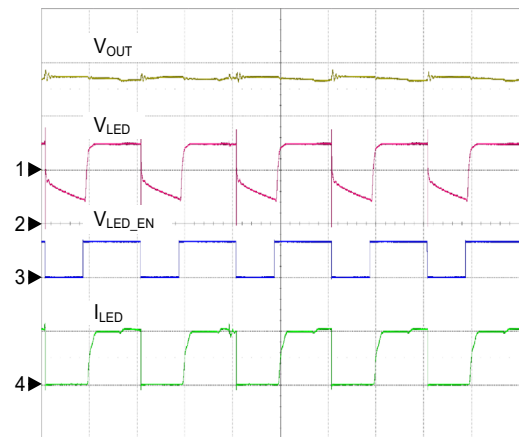
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 50 μ s/Div

Dimming, 30Hz at 50% duty



I_{LED} Ramp-up Time 10mA/4 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 20ms/Div

Dimming, 5KHz at 60% duty

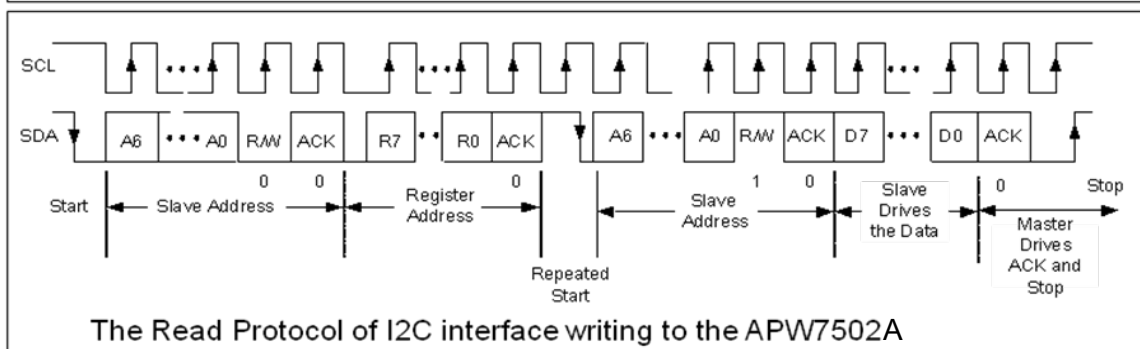
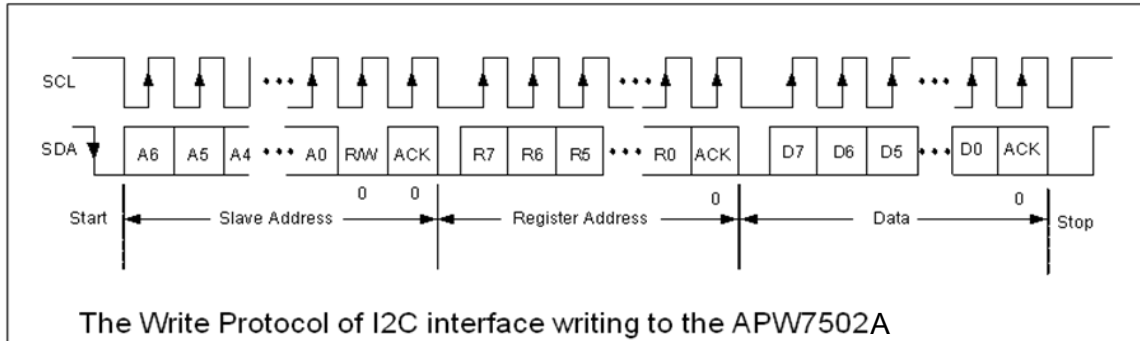


I_{LED} Ramp-up Time 10mA/0.5 μ s
CH1: V_{OUT} , 2V/Div, DC
CH2: V_{LED} , 2V/Div, DC
CH3: V_{LED_EN} , 5V/Div, DC
CH4: I_{LED} , 500mA/Div, DC
TIME: 100 μ s/Div

Function Descriptions

I²C Programming

The APW7502A's I²C Slave Address is a hard-coded 7 bit address **0000010**. The APW7502A supports the following write and read protocol.



Registers Map

NAME	Address	Default	R/W	Data							
ILED Source Current	0x00	0x28	R/W		ILED6	ILED5	ILED4	ILED3	ILED2	ILED1	ILED0
ILED Ramp-up Time	0x01	0x03	R/W						TRUT2	TRUT1	TRUT0
ILED Enable Control	0x02	0x02	R/W							EN1	EN0
Switching Frequency	0x03	0x00	R/W								FSW
PWM Current Limit	0x04	0x00	R/W								LXCL
Product Version	0x06	0x00	R						VER2	VER1	VER0

Function Descriptions (Cont.)

▪Register name: ILED Source Current

▪Register Address: 0x00

Bit	7	6	5	4	3	2	1	0	
Bit Name	-	ILED6	ILED5	ILED4	ILED3	ILED2	ILED1	ILED0	
Default	0	0	1	0	1	0	0	1	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name	Bit Definition								Reset
ILED[6:0]	ILED Source Current Setting 000 0000: 100mA 000 0001: 110mA 000 0010: 120mA 000 0011: 130mA 010 1000: 500mA (default) 111 1100: 1340mA 111 1101: 1350mA 111 1110: 1360mA 111 1111: 1370mA								by VIN POR

▪Register name: ILED Ramp-up Time

▪Register Address: 0x01

Bit	7	6	5	4	3	2	1	0	
Bit Name	-	-	-	-	-	TRUT2	TRUT1	TRUT0	
Default	0	0	0	0	0	0	1	1	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name	Bit Definition								Reset
TRUT[2:0]	ILED Ramp-up Time Setting 000: 10mA/0.5μs 001: 10mA/1μs 010: 10mA/2μs 011: 10mA/4μs (default) 100: 10mA/8μs 101: 10mA/16μs 110: 10mA/32μs 111: 10mA/64μs								by VIN POR

▪Register name: ILED Enable Control

▪Register Address: 0x02

Bit	7	6	5	4	3	2	1	0	
Bit Name	-	-	-	-	-	-	EN1	EN0	
Default	0	0	0	0	0	0	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name	Bit Definition								Reset
EN[1:0]	ILED Enable Control Setting 01: ILED Source Current Control by I ² C Register 10: ILED Source Current Control by External EN pin (default)								by VIN POR

Function Descriptions (Cont.)

▪Register name: Switching Frequency

▪Register Address: 0x03

Bit	7	6	5	4	3	2	1	0	
Bit Name	-	-	-	-	-	-	-	FSW	
Default	0	0	0	0	0	0	0	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name	Bit Definition								Reset
FSW	PWM Switching Frequency Selection: 0: 2MHz (default) 1: 1MHz								by VIN POR

▪Register name: PWM Current Limit

▪Register Address: 0x04

Bit	7	6	5	4	3	2	1	0	
Bit Name	-	-	-	-	-	-	-	LXCL	
Default	0	0	0	0	0	0	0	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Name	Bit Definition								Reset
LXCL	PWM Current Limit Setting: 0: 2A(default) 1: 3A								-

▪Register name: Product Version

▪Register Address: 0x06

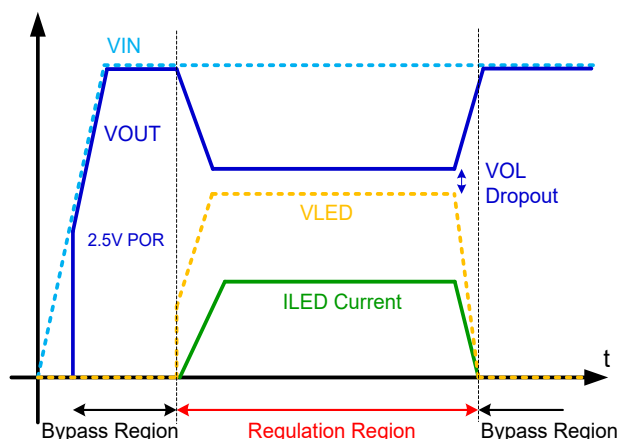
Bit	7	6	5	4	3	2	1	0	
Bit Name	-	-	-	-	-	VER2	VER1	VER0	
Default	0	0	0	0	0	0	0	0	
Read/Write	R	R	R	R	R	R	R	R	
Bit Name	Bit Definition								Reset
VER[2:0]	Product Version: 000: Version A 001: Version B 010: Version C 011: Version D 100: Version E 101: Version F 110: Version G 111: Version H								-

Function Descriptions (Cont.)

The APW7502A is a 5V/1.37A, 2MHz buck converter with I²C interface. The output current is well regulated to a fixed level to drive VCSEL or IR_LED. The driving current can be adjusted from 100mA to 1.37A in 10mA resolution.

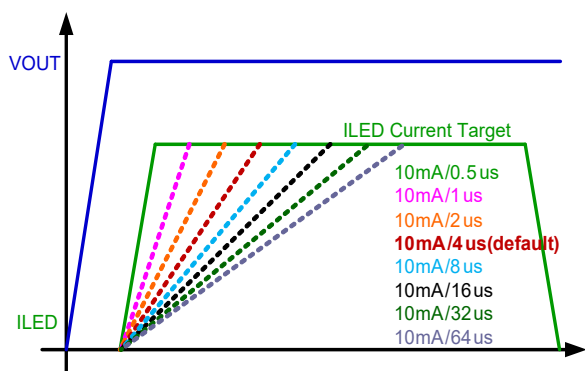
Bypass and Regulation Region

When the device is powered by a valid voltage but not enabled, the device turns the high side MOSFET fully on. In this manner the device can quickly respond to receiving enable input and then provide instant current to drive LED(s). Once enabled, the device controls and regulates its output current to a preset target. Both the ILED start-up slew rate and ILED target are adjustable via I²C interface.



ILED Start-up Slew Rate Adjustment

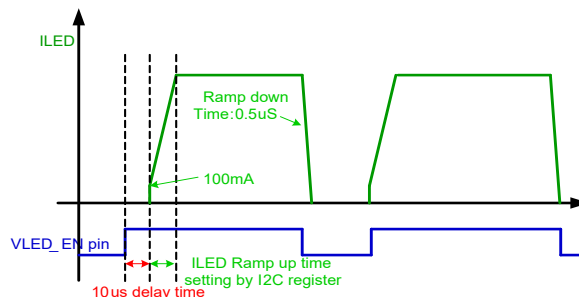
The APW7502A provides ILED start-up slew rate adjustment via I²C interface. There are 8 segments of adjustment range which is from 10mA/0.5μs to 10mA/64μs, as shown as the diagram blow.



Enable

Pull the VLED_EN above 1V to enable the device and pull VLED_EN pin below 0.4V to disable the device. In shutdown mode, all internal control circuits are turned off. When the device exits shutdown mode, the output has soft-start function as the input voltage startup.

EN Control

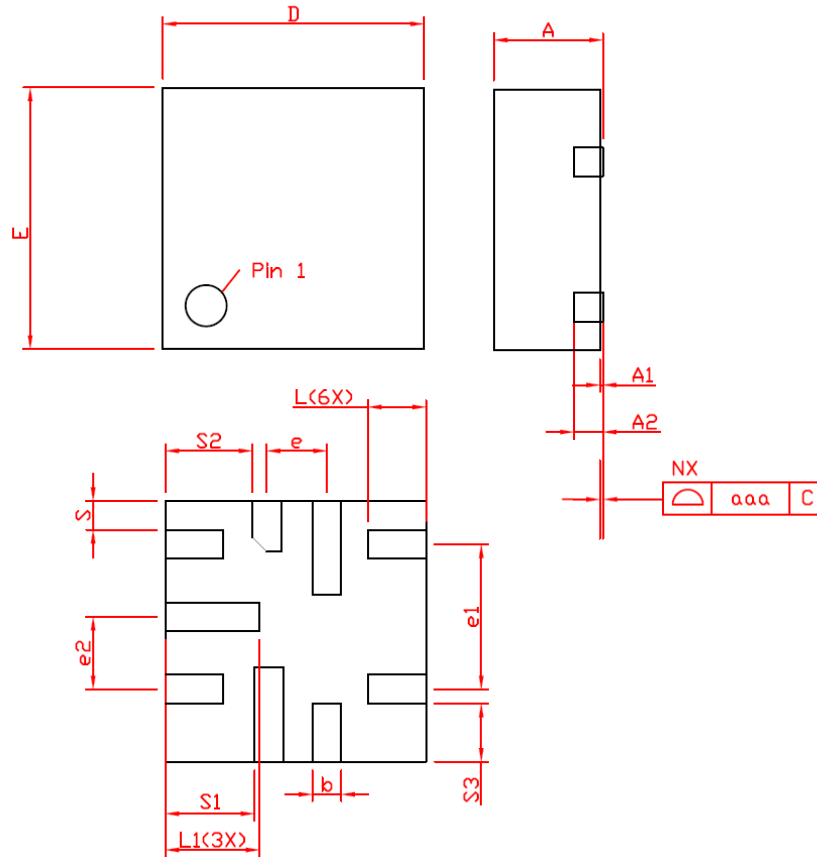


Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7502A. When the junction temperature exceeds $T_J = +150^{\circ}\text{C}$, a thermal sensor turns off the power MOSFET, allowing the device to cool down. The thermal sensor allows the converter to start a start-up process and regulate the output voltage again after the junction temperature cools by 20°C .

Package Information

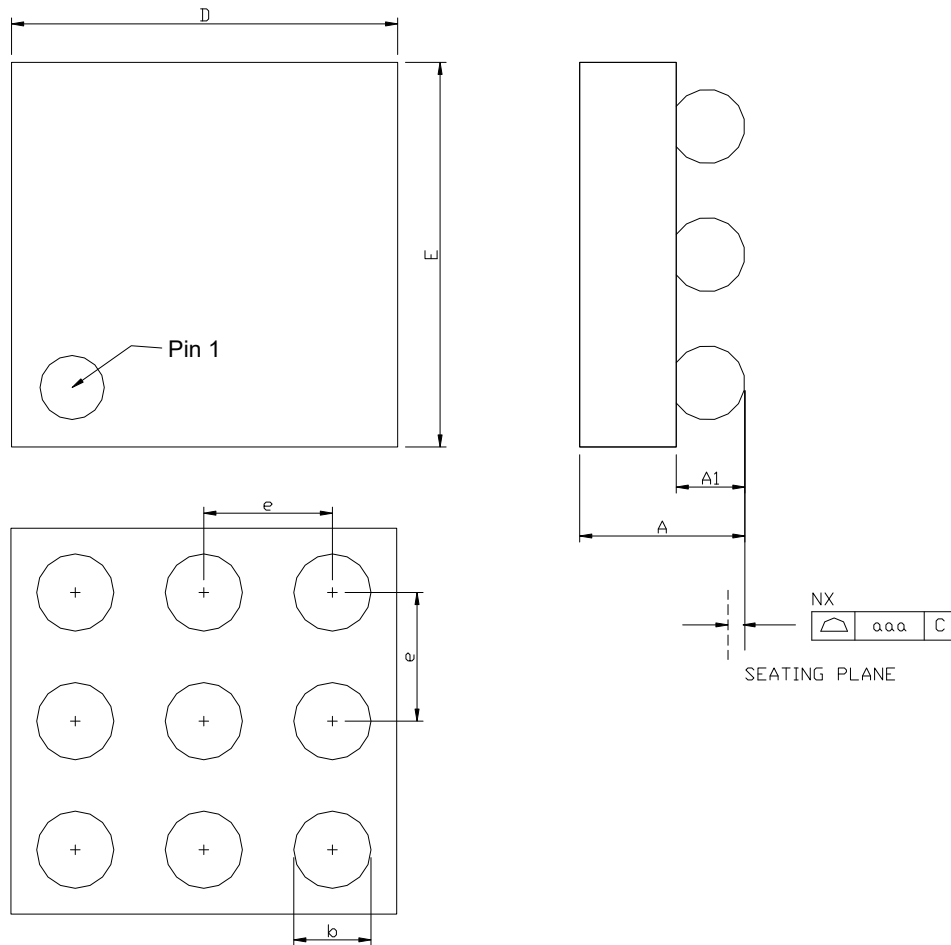
TQFN 1.8x1.8-9



SYMBOL	TQFN 1.8x1.8-9			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A2	0.20 REF		0.008 REF	
D	1.70	1.90	0.067	0.075
E	1.70	1.90	0.067	0.075
b	0.15	0.25	0.006	0.010
L	0.35	0.45	0.014	0.018
L1	0.60	0.70	0.024	0.028
e	0.40 BSC		0.016 BSC	
e1	1.00 BSC		0.039 BSC	
e2	0.50 BSC		0.020 BSC	
S	0.20 REF		0.008 REF	
S1	0.615 REF		0.024 REF	
S2	0.60 REF		0.024 REF	
S3	0.40 REF		0.016 REF	
aaa	0.08		0.003	

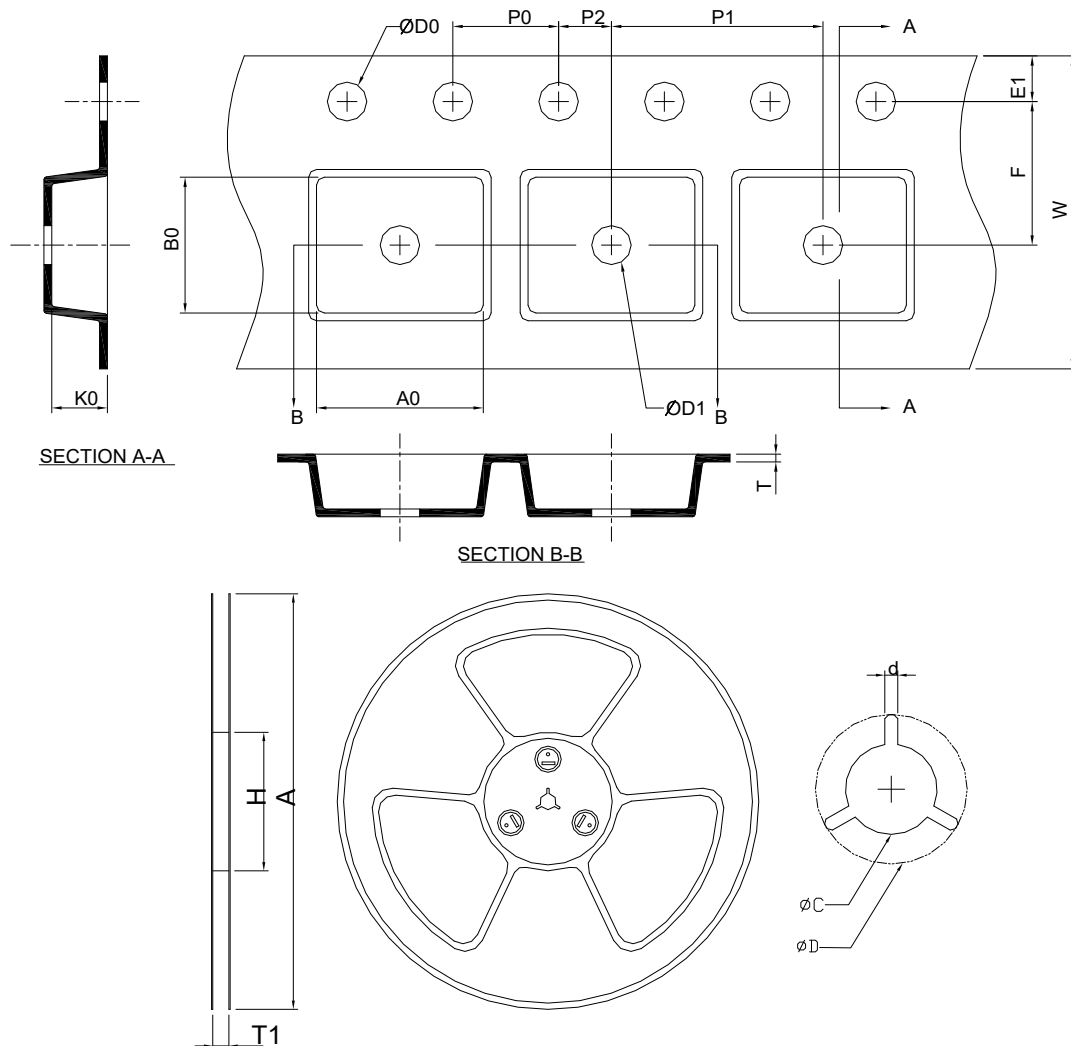
Package Information (Cont.)

WLCSP 1.42x1.42-9



SYMBOL	WLCSP1.42x1.42-9			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.60		0.024
A1	0.18	0.22	0.007	0.009
b	0.22	0.30	0.009	0.012
D	1.42	1.50	0.056	0.059
E	1.42	1.50	0.056	0.059
e	0.50 BSC		0.020 BSC	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 1.8x1.8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0+0.30 -0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	2.05±0.10	2.05±0.10	1.00±0.20
Application	A	H	T1	C	d	D	W	E1	F
WLCSP 1.42x1.42	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.5 MIN.	0.6+0.00 -0.40	1.60±0.20	1.60±0.20	0.75±0.20

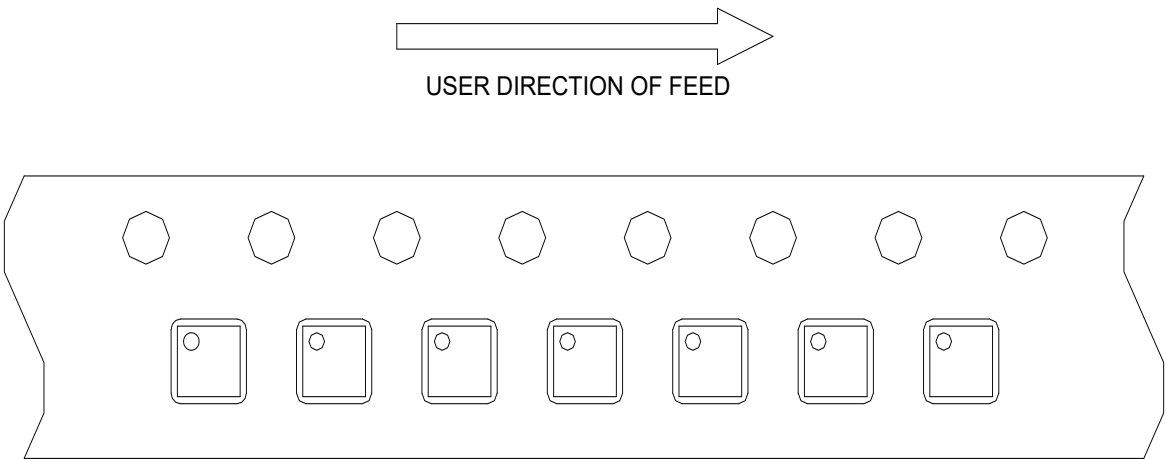
(mm)

Devices Per Unit

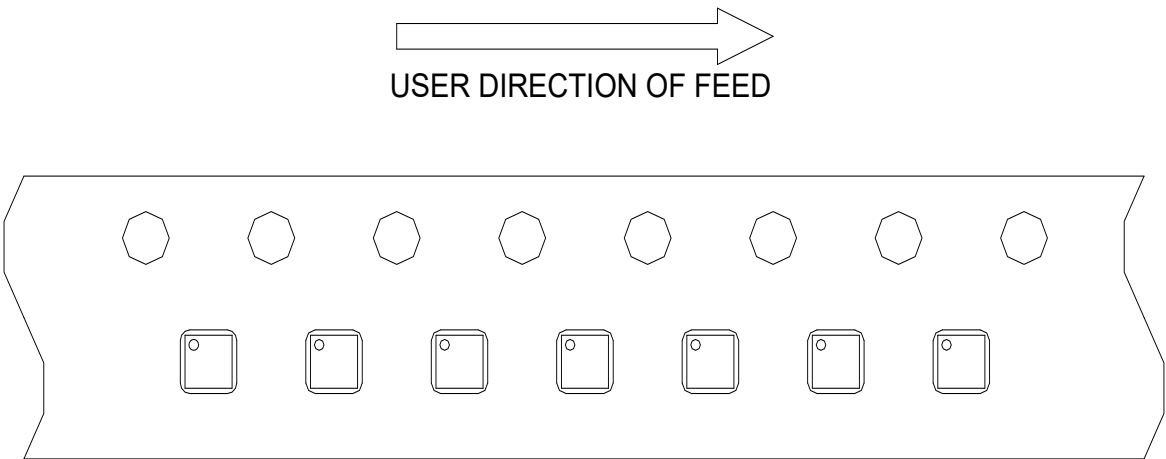
Package Type	Packing	Quantity
TQFN 1.8x1.8	Tape & Reel	3000
WLCSP 1.42x1.42	Tape & Reel	3000

Taping Direction Information

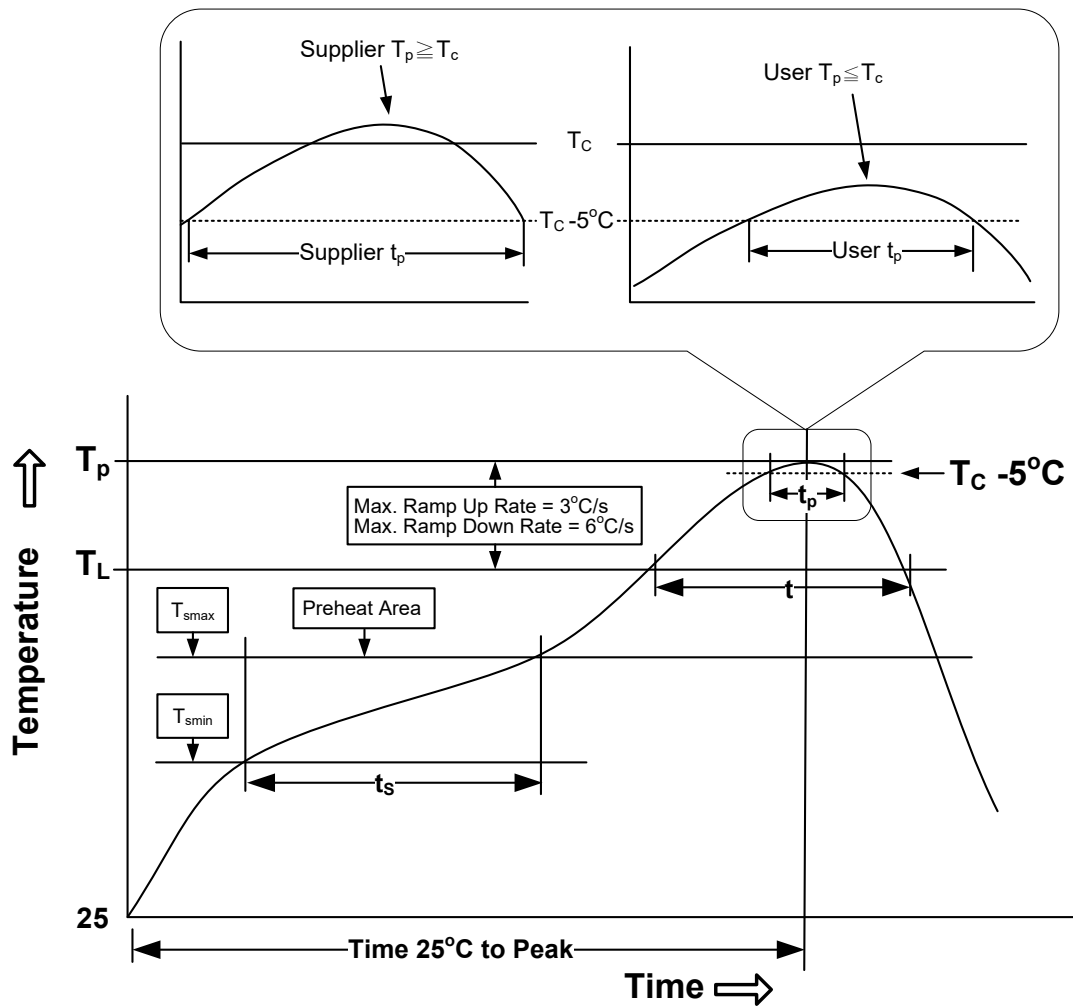
TQFN 1.8x1.8-9



WLCSP 1.42x1.42-9



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100°C 150°C 60-120 seconds	150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 9	See Classification Temp in table 10
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 9. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 10. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test Item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD-78	10ms, $1_{tr} \geq 100\text{mA}$

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