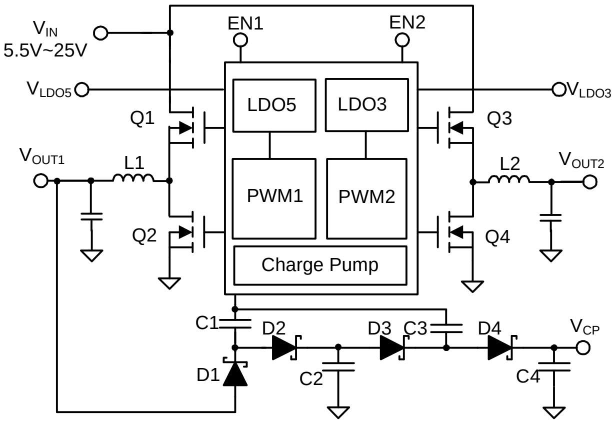
System Power PWM Controller with Economy Standby Mode

Features

- Wide Input voltage Range from 5.5V to 25V
- Provide 5 Independent Outputs with ±1.0% Accuracy Over-Temperature
  - PWM1 Controller with Adjustable (2V to 5.5V) Output
  - PWM2 Controller with Adjustable (2V to 5.5V) Output
  - 100mA Low Dropout Regulator (LDO5) with Fixed 5V Output
  - 100mA Low Dropout Regulator (LDO3) with Fixed 3.3V Output
  - 250kHz Clock Signal for 15V Charge Pump (Used PWM1 as Its Power Supply)
- Excellent Line/Load Regulations about ±1.5% over temperature range at PWM Channels
- Low Consumption in Standby Mode
- 2Cells Input Battery Support
- Built in POR Control Scheme Implemented
- Constant On-Time Control Scheme
- Built in Soft Start for PWM Outputs and Soft Stop for PWM Outputs and LDO Outputs
- Integrated Bootstrap Forward P-CH MOSFET
- High Efficiency over Light to Full Load Range (PWMs)
- Built in Power Good Indicators (PWMs)
- 60% Under-Voltage and 115% Over-Voltage Protections (PWM)
- Adjustable Current-Limit Protection (PWMs)
  - Using Sense Low-Side MOSFET's $R_{DS(ON)}$
- Over-Temperature Protection
- 3mmx3mm Thin QFN-20 (TQFN3x3-20) Package
- Lead Free and Green Device Available (RoHS Compliant)

Simplified Application Circuit



General Description

The APW8833A integrates dual step-down, constant-on-time, synchronous PWM controllers (that drives dual N-channel MOSFETs for each channel) and two low drop-out regulators as well as various protections into a chip. The PWM controllers step down high voltage of a battery to generate low-voltage for NB applications. The output of PWM1 and PWM2 can be adjusted from 2V to 5.5V by setting a resistive voltage-divider from VOUTx to GND. The linear regulators provide 5V and 3.3V output for standby power supply. The linear regulators provide up to 100mA output current. When the PWMx output voltage is higher than LDOx bypass threshold, the related LDOx regulator is shut off and its output is connected to VOUTx by internal switchover MOSFET. It can save power dissipation. The charge pump circuit with 250kHz clock driver uses VOUT1 as its power supply to generate approximately 15V DC voltage.

The APW8833A provides excellent transient response and accurate DC output voltage in either PFM or PWM Mode. In Pulse-Frequency Mode (PFM), the APW8833A provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. The Forced-PWM Mode works nearly at constant frequency for low-noise requirements. The unique ultrasonic mode maintains the switching frequency above 25kHz, which eliminates noise in audio application.

General Description (Cont.)

The APW8833A has individual enable controls for each PWM channels. Pulling both EN1/2 pin low shuts down the all of outputs. The LDO3 and LDO5 of APW8833A are always on standby power.The APW8833A is available in a TQFN3x3-20 package.

Applications

- **Notebook and Sub-Notebook Computers**
- **Portable Devices**
- **3-Cell and 4-Cell Li+ Battery-Powered Devices**
- **Graphic Cards**
- **Game Consoles**
- **Telecommunications**

Ordering and Marking Information

APW8833A □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB : TQFN3x3-20
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device G : Halogen and Lead Free Device

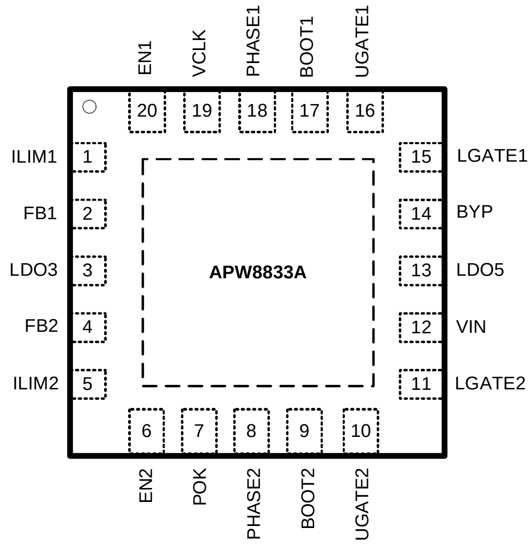
APW8833A QB :
APW
8833A
XXXXX

XXXXX - Date Code

Device Number	POK Enable Delay	Switching Frequency	SKIP Mode	UVP Enable Blanking Time	Soft-Start Time	Current Limit
APW8833A	1.4ms	300kHz/355kHz	Auto-skip	1.4ms	0.9ms	10uA

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN3x3-20
(Top View)

= GND and Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Power Voltage (VIN to GND)	-0.3 ~ 28	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
$V_{UG-PHASE}$	UGATE Voltage (UGATE to PHASE) <50ns pulse width >50ns pulse width	-5 ~ V_{BOOT}+5 -0.3 ~ V_{BOOT}+0.3	V
V_{LG-GND}	LGATE Voltage (LGATE to GND) <50ns pulse width >50ns pulse width	-5 ~ V_{LDO5} +5 -0.3 ~ V_{LDO5} +0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <100ns pulse width >100ns pulse width	-5 ~ 35 -0.3 ~ 28	V
	All Other Pins (FBx, BYP, LDO5, LDO3, VCLK, ENx, ILIMx to GND)	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient	65	°C/W
θ_{JC}	Thermal Resistance - Junction to Case	10	

Note 2: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective the thermal conductivity test board in free air. The thermal pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	PWM1/2 Converter Input Voltage	5.5 ~ 25	V
V_{OUT1}	PWM1 Converter Output Voltage	2 ~ 5.5	V
V_{OUT2}	PWM2 Converter Output Voltage	2 ~ 5.5	V
V_{LIMx}	I_{LIMx} Adjustment Range ($V_{ILIMx-GND}$)	0.2 ~ 2	V
C_{IN}	PWM1/2 Converter Input Capacitor (MLCC)	10 ~	μF
C_{LDO}	LDO Output Capacitor (MLCC)	1.0 ~	μF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8833A			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY POWER						
I_{VIN}	VIN Supply Current	Supply Current1, BYP=0V, EN1=EN2=5V, V_{FB1}=V_{FB2}=2.05V	-	280	520	μA
		Supply Current2, BYP=5V, EN1=EN2=5V, V_{FB1}=V_{FB2}=2.05V	-	10	-	μA
		Standby Current2, BYP=0V, EN1=EN2=0V	-	40	-	
UNDER VOLTAGE LOCK OUT PROTECTION (UVLO)						
	LDO5 UVLO Threshold	Rising Edge, PWM 1/2 Enable	4.15	4.55	4.75	V
		Hysteresis	-	0.4	-	V
	LDO3 UVLO Threshold	Rising Edge	2.9	3.0	3.1	V
		Hysteresis	-	0.1	-	V
	VIN UVLO Threshold	Rising Threshold, LDO3 & LDO5 Enable	-	4.58	-	V
		Falling Threshold, LDOx Shutdown with Soft Stop	-	4.1	-	V
PWM CONTROLLERS						
V_{FB}	FBx Reference Voltage	T_A= -40°C to 85°C	1.98	2.0	2.02	V
I_{FB}	FBx Input Current	V_{FBX}=2.0V, T_A=25°C	-20	-	20	nA
T_{SS}	Soft-Start Time	ENx High to V_{OUT} 95% Regulation, LDO5=5V	0.45	0.9	1.6	ms
	Soft-Stop Time	ENx Low to V_{FBX} < 0.1V	-	3.0	-	ms
F_{SW1}	PWM1 Switching Frequency	V_{IN}=20V, PWM1=5V	240	300	360	kHz
F_{SW2}	PWM2 Switching Frequency	V_{IN}=20V, PWM2=3.33V	280	355	420	
	UGATEx Minimum Off-Time		200	300	400	ns

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8833A			Unit
			Min.	Typ.	Max.	
LOW DROPOUT LINEAR REGULATORS (LDO5/LDO3)						
	LDO5 Output Voltage	BYP=GND, 7V < V_{IN} < 25V, I_{LDO5} < 100mA	4.9	5.0	5.1	V
	LDO3 Output Voltage	7V < V_{IN} < 25V, I_{LDO3} < 100mA	3.267	3.300	3.333	V
V_{THBYP5}	LDO5 Switch-Over Threshold to BYP	Rising Edge at BYP Regulation Point	-	4.66	-	V
	VOUT1-to-LDO5 Switch On Resistance	VOUT1=5V, 50mA	-	1.5	3	Ω
	LDOx Current Limit	VOUTx=GND, LDOx=GND	120	200	400	mA
	LDOx Discharge On Resistance	I_{LDOX}=5mA	-	50	100	Ω
CHARGE PUMP CLOCK						
V_{CLKH}	High Level Voltage	I_{VCLK}= -10mA, LDO5=5V, T_A=25°C	-	4.92	-	V
V_{CLKL}	Low Level Voltage	I_{VCLK}=10mA, LDO5=5V, T_A=25°C	-	0.06	-	V
F_{CLK}	Clock Frequency	T_A=25°C	-	250	-	kHz
PWM1/2 PROTECTIONS						
	Over Voltage Protection Threshold	V_{FBX} Rising	110	115	120	%
	Over Voltage Fault Propagation Delay	Delta Voltage=10mV	-	3	-	µs
I_{LIM}	Current Limit Current Source	V_{ILIMx}=1V, T_A=25°C	9	10	11.5	µA
	Current Limit Current Source	On the Basis of 25°C	-	4500	-	ppm/°C
	Maximum Setting Voltage	V_{ILIMx}=5V, Setting Current Limit Threshold	205	250	-	mV
	Current Limit Comparator Offset	($V_{ILIMx-GND}$-$V_{PGND-PHASEx}$), V_{ILIMx}=920mV	-15	0	15	mV
	Zero-Crossing Threshold	$V_{PGND-PHASE}$	-5	0	5	mV
	Under-Voltage Protection Threshold		55	60	65	%
	Under-Voltage Protection Debounce Interval		-	25	-	µs
	Under-Voltage Protection Enable Blanking Time	From EN Signal go High to POK goes High	-	1.4	-	ms
	Over-Temperature Protection Threshold	T_J Rising	-	160	-	°C
	Over-Temperature Protection Threshold	Hysteresis	-	25	-	°C

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8833A			Unit
			Min.	Typ.	Max.	
POWER GOOD						
	POK Threshold	POK in from Lower (POK goes High)	87	90	93	%
		POK Hysteresis	-	10	-	
		POK Upper Threshold (POK goes Low)	110	115	120	
	POK Enable Delay	From EN Signal go High to POK goes High	-	1.4	-	ms
	POK Sink Current	V_{POK}=500mV	2.5	7.5	-	mA
	POK Leakage Current	V_{POK}=5V	-	0.1	1	μA
LOGIC LEVELS						
	ENx Input Voltage Threshold	Enable	-	-	1.5	V
		Shutdown	0.4	-	-	
	ENx Input Leakage Current	V_{EN}=5V	-	0.1	1	μA
GATE DRIVERS						
	UG Pull-Up Resistance	$V_{BOOTx} – V_{UGATEx}$=250mV	-	3	5	Ω
	UG Sink Resistance	$V_{UGATEx} – V_{PHASEx}$=250mV	-	1.7	2.5	Ω
	LG Pull-Up Resistance	$V_{LDO5} – V_{LGATEx}$=250mV	-	3	5	Ω
	LG Sink Resistance	$V_{LGATEx} – V_{PGND}$=250mV	-	1.0	2	Ω
	Dead Time	UG Falling to LG Rising	-	20	-	ns
		LG Falling to UG Rising	-	20	-	ns
BOOTSTRAP SWITCH						
V_F	Forward Voltage	$V_{LDO5} – V_{BOOTx-GND}$, I_F=10mA	-	0.15	0.25	V
I_R	Reverse Leakage	$V_{BOOTx-GND}$=30V, V_{PHASEx}=25V, V_{LDO5}=5V	-	-	0.5	μA

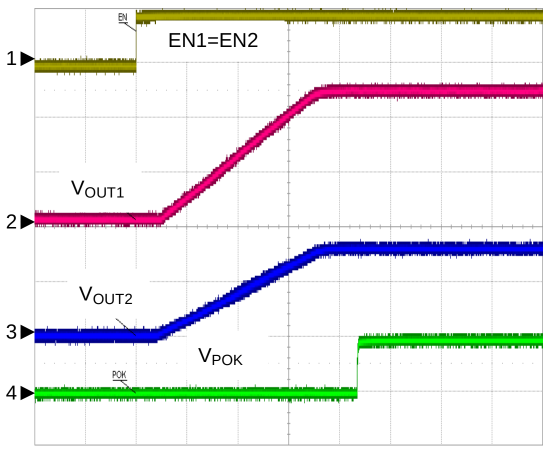
Pin Description

PIN		FUNCTION
NO.	NAME	
1	ILIM1	Current Limit Adjustment. There is an internal 10µA current source from LDO5 to ILIM1 and connected a resistor from ILIM1 to GND to set the current limit threshold. The PGND-PHASE1 current-limit threshold is 1/8th the voltage set at ILIM1 over a 0.2 to 2V range. The logic current limit threshold is default to 250mV value if ILIM1 is 5V.
2	FB1	Output voltage feedback pin (PWM1). It can use a resistive divider from VOUT1 to GND to adjust the output from 2V to 5.5V.
3	LDO3	3.3V Linear Regulator Output. LDO3 can provide a total of 100mA, 3.3V external loads. Bypass to GND with a minimum of 1.0uF ceramic capacitor for stability.
4	FB2	Output voltage feedback pin (PWM2). It can use a resistive divider from VOUT2 to GND to adjust the output from 2V to 5.5V.
5	ILIM2	Current Limit Adjustment. There is an internal 10µA current source from LDO5 to ILIM2 and connected a resistor from ILIM2 to GND to set the current limit threshold. The PGND-PHASE2 current-limit threshold is 1/8th the voltage set at ILIM2 over a 0.2 to 2V range. The logic current limit threshold is default to 250mV value if ILIM2 is 5V.
6	EN2	PWM2 Enable. PWM2 is enabled when EN2=1. When EN2=0, PWM2 is in shutdown.
7	POK	Power-Good Output Pin of Both PWMs (Logic AND). POK is an open-drain output used to indicate the status of the PWMx output voltage. Connect the POK in to +5V through a pull-high resistor.
8	PHASE2	Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM2. Connect this pin to the Source of the high-side MOSFET. PHASE2 serves as the lower supply rail for the UGATE2 high-side gate driver. PHASE2 is the current-sense input for the PWM2.
9	BOOT2	Supply Input for The UGATE2 Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
10	UGATE2	Output of The High-Side MOSFET Driver for PWM2. Connect this pin to Gate of the high-side MOSFET.
11	LGATE2	Output of The Low-Side MOSFET Driver for PWM2. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to LDO5.
12	VIN	Battery voltage input pin. VIN powers linear regulators and is also used for the constant on-time PWM on-time one-shot circuits. Connect VIN to the battery input and bypass with a 1µF capacitor for noise interference.
13	LDO5	5V Linear Regulator Output. LDO5 can provide a total of 100mA, 5V external loads. When LDO5 is at 5V and PWM1 output voltage is over bypass threshold and POK is in high state and PWM1 is not in current limit condition, the internal LDO will shut down, and LDO5 output pin connects to VOUT1 through a 1.5Ω switch. Bypass to GND with a minimum of 1.0uF ceramic capacitor for stability.
14	BYP	BYP is the input pin of switchover voltage for the LDO5. This pin makes a direct measurement of the PWM1 output voltage.
15	LGATE1	Output of The Low-Side MOSFET Driver for PWM1. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to LDO5.
16	UGATE1	Output of The High-Side MOSFET Driver for PWM1. Connect this pin to Gate of the high-side MOSFET.
17	BOOT1	Supply Input for The UGATE1 Gate Driver and an internal level-shift circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
18	PHASE1	Junction Point of The High-Side MOSFET Source, Output Filter Inductor and The Low-Side MOSFET Drain for PWM1. Connect this pin to the Source of the high-side MOSFET. PHASE1 serves as the lower supply rail for the UGATE1 high-side gate driver. PHASE1 is the current-sense input for the PWM1.
19	VCLK	250kHz Clock Output for 15V Charge Pump.
20	EN1	PWM1 Enable. PWM1 is enabled when EN1=1. When EN1=0, PWM1 is in shutdown.
Thermal Pad	GND	Signal Ground for The IC.

Operating Waveforms

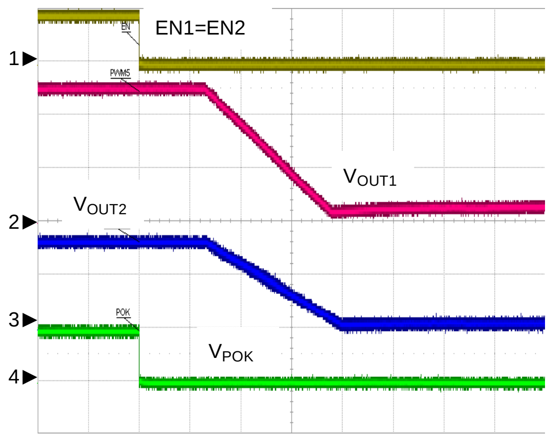
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

Enbale



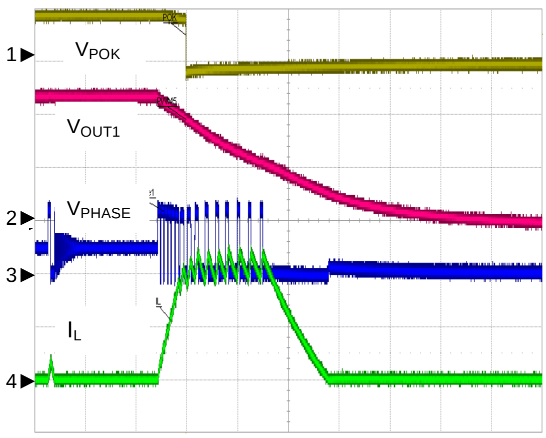
CH1: EN1=EN2, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
CH4: V_{POK}, 5V/Div
TIME: 200us/Div

Shutdown



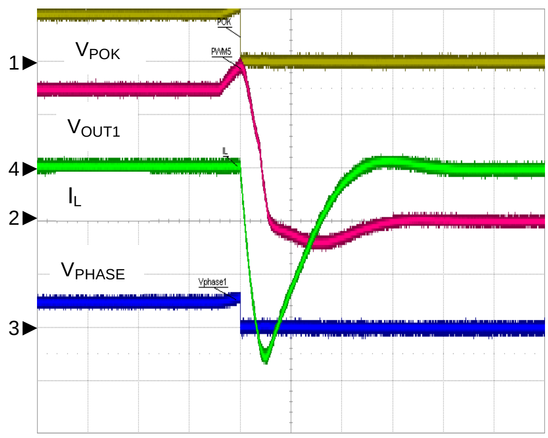
CH1: EN1=EN2, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
CH4: V_{POK}, 5V/Div
TIME: 1ms/Div

Under Voltage Protection



CH1: POK, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{PHASE1}, 10V/Div
CH4: I_L, 5A/Div
TIME: 20us/Div

Over Voltage Protection

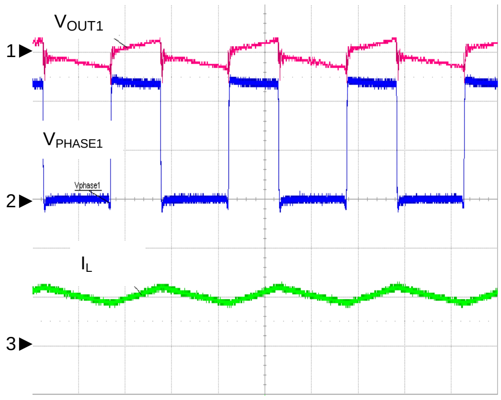


CH1: POK, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{PHASE1}, 10V/Div
CH4: I_L, 10A/Div
TIME: 100us/Div

Operating Waveforms (Cont.)

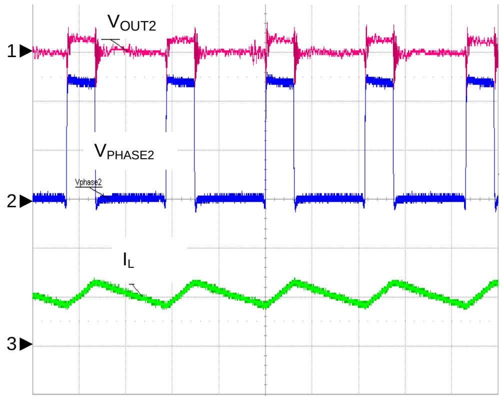
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

Output 1 Ripple Voltage



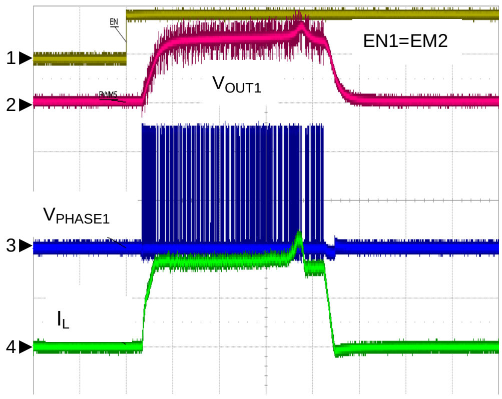
CH1: V_{OUT1}, 50mV/Div,AC
CH2: V_{PHASE1}, 2V/Div
CH3: I_{L1}, 5A/Div
TIME: 1us/Div

Output 2 Ripple Voltage



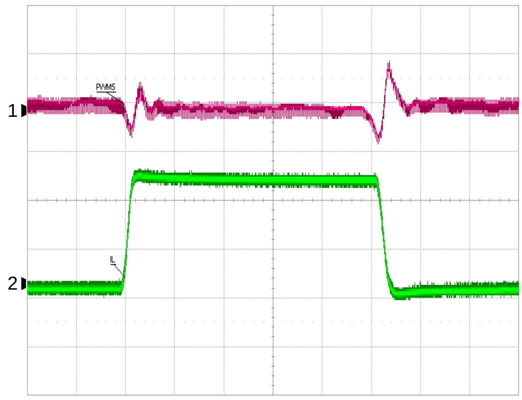
CH1: V_{OUT2}, 20mV/Div,AC
CH2: V_{PHASE2}, 2V/Div
CH3: I_{L2}, 5A/Div
TIME: 1us/Div

Current Limit , R_{ILIM} = 39K



CH1: EN, 5V/Div
CH2: V_{OUT1}, 50mV/Div
CH3: V_{PHASE1}, 5V/Div
CH4: I_L, 5A/Div
TIME: 20us/Div

Load transient

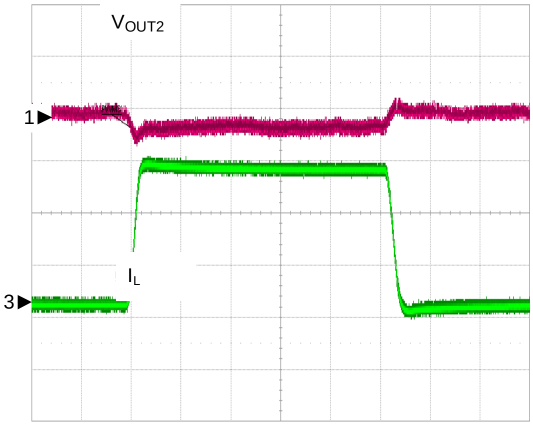


CH1: V_{OUT1}, 50mV/Div,AC
CH2: IL, 2A/Div
TIME: 100us/Div

Operating Waveforms (Cont.)

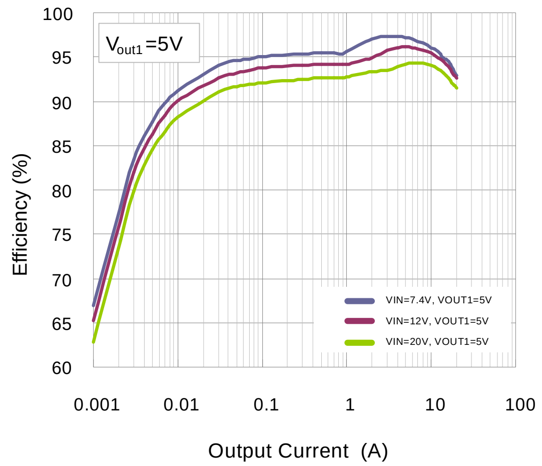
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A=25°C unless otherwise specified.

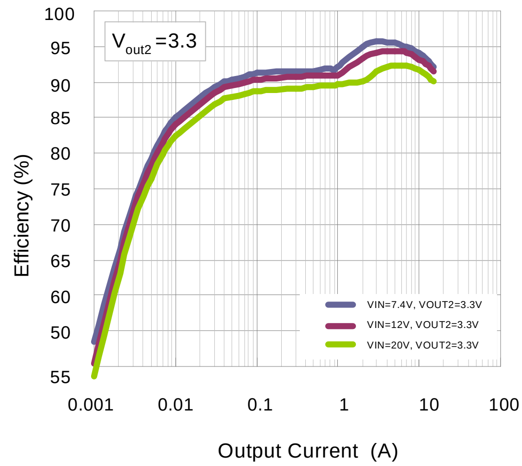
Load transient

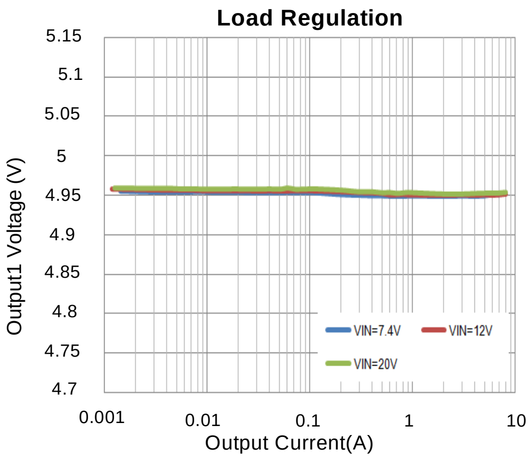


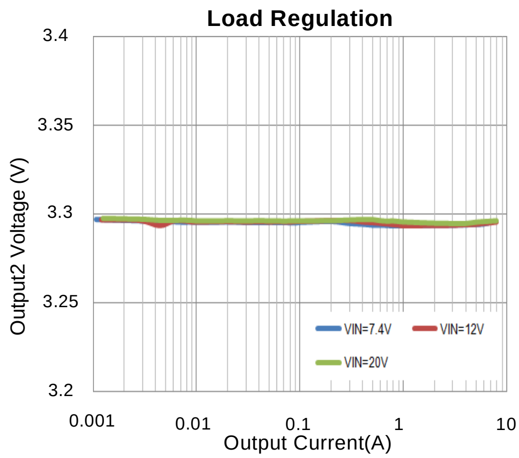
CH1: V_{OUT2}, 20mV/Div,AC
CH2: IL, 2A/Div
TIME: 100us/Div

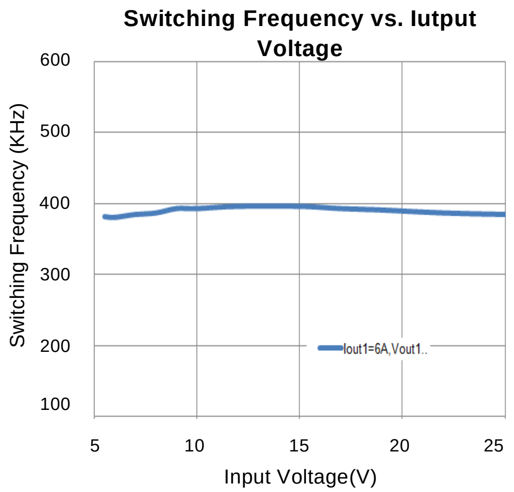
Typical Operating Characteristics

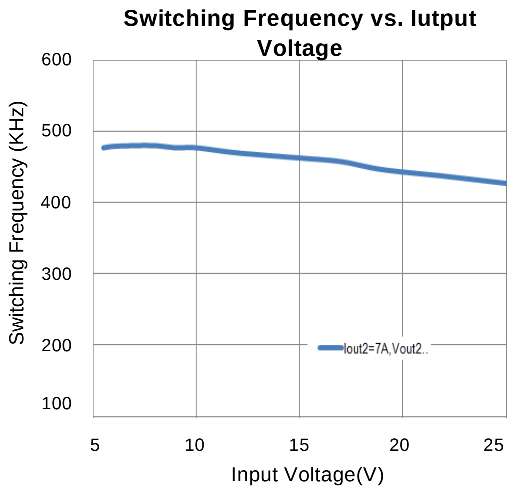




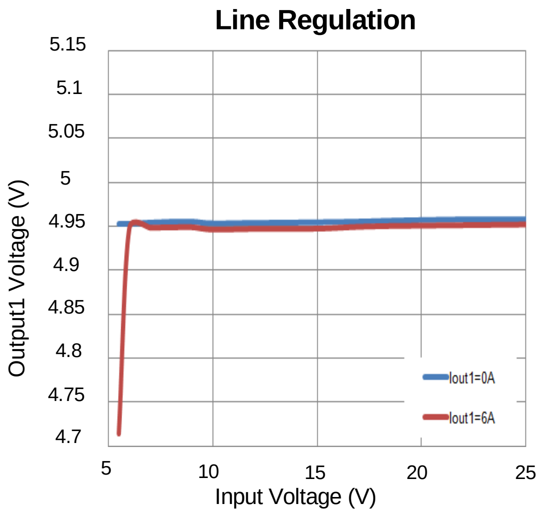


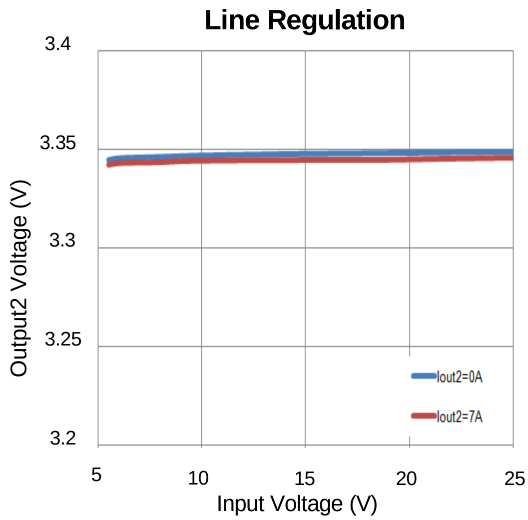




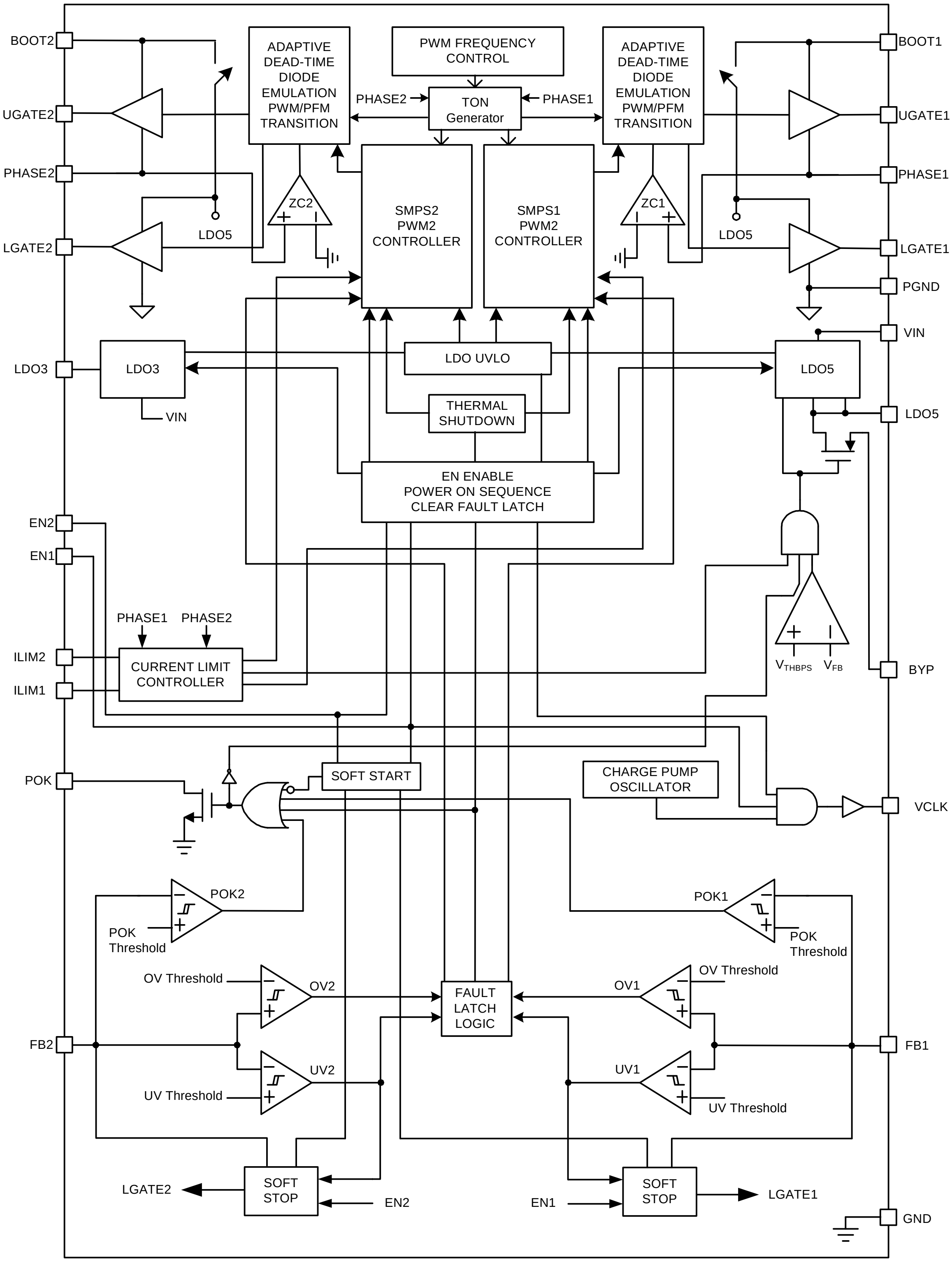


Typical Operating Characteristics (Cont.)

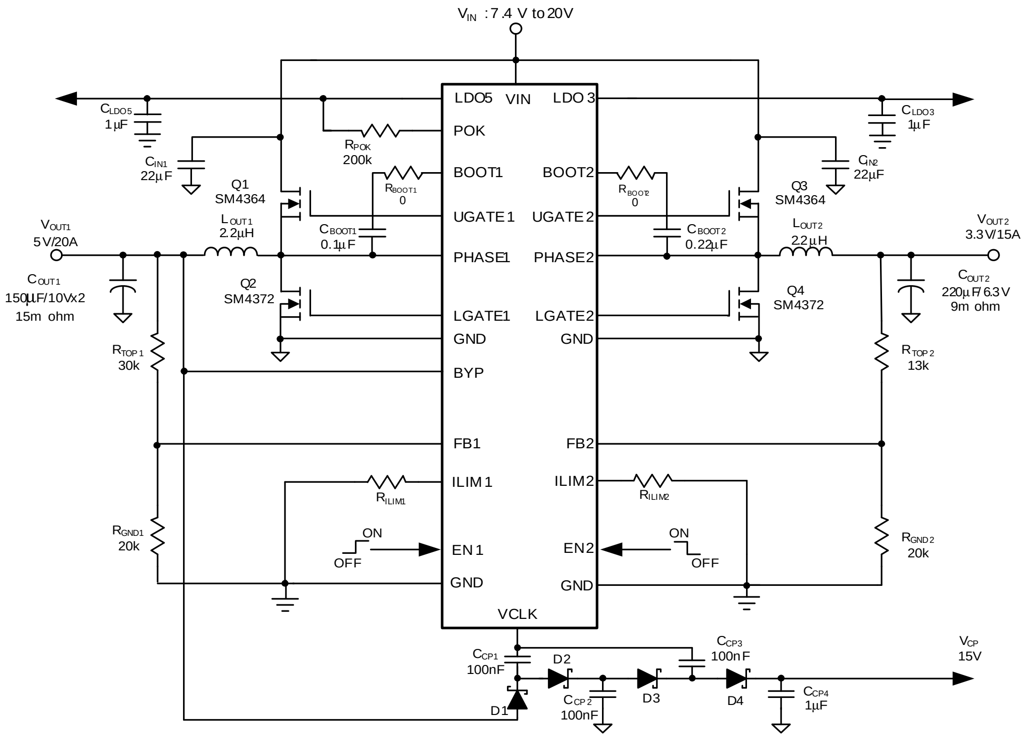




Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage.

In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typ.300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads.

This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON\text{ - }PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode. Similarly, the on-time of ultrasonic mode is the same with PFM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM}$$

$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Linear Regulator (LDO3 and LDO5)

The LDO3 and LDO5 regulators can supply up to 100mA for external loads. Bypass to GND with a minimum of 1uF ceramic capacitor for stability. For APW8833A, When VIN reaches POR rising threshold, the V_{LDO3} is fixed 3.33V and the V_{LDO5} is fixed 5V in standby mode. Let's see the table1 "Operating Mode Truth Table" for the detail description about standby mode. For all of APW8833A series, When PWM1 output voltage is over whose bypass threshold, and POK is in high state and PWM1 is not in current limit condition, the internal LDO5 to VOUT1 switchover is active. These actions change the current path to power the loads from the PWM regulator voltage, rather than from the internal linear regulator.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls. The POR function continually monitors the supply voltage on the LDO5 pins. LDO5 POR circuitry inhibits wrong switching. When the rising V_{LDO5} voltage reaches the rising POR threshold (4.3V typical), the PWM output voltages begin to ramp up.

When the LDO5 voltage is lower than 4.2V(typ.) or LDO3 voltage is lower than 2.9V(typ.), both switch power supplies are shut off. This is non-latch protection. LDO5 POR threshold could reset the under-voltage, over-voltage.

Function Description (Cont.)

Soft Start

The APW8833A integrates soft-start circuit to ramp up the PWMx output voltage of the converter to the programmed regulation set point at a predictable slew rate.
The slew rate of PWMx output voltage is internally controlled to limit the inrush current through the output capacitors during soft start process. When the ENx pin is pulled above the rising threshold voltage, the related PWM initiates a soft-start process to ramp up the output voltage. The soft-start interval is 0.9ms(typical) and independent of the UGATE switching frequency.

Enable Controls

The APW8833A has two independent enable controls for PWM part. When the ENx pin is high at standby mode, the PWMx initiates a soft-start process to ramp up the output voltage. The PWM1 and PWM2 are controlled individually by EN1 and EN2. When EN1 and EN2 are both low, the chip is in its low-power standby state. When the EN1 is high, the clock signal becomes available from VCLK pin. Both PWM outputs are discharged to low voltage by the soft stop method and both LDO outputs are discharged to 0V through a 50Ω switch in soft stop state. Driving EN1 and EN2 (logic AND) below low threshold clears the over-voltage, and under-voltage fault latches.

Charge Pump

The condition of the 250kHz clock signal can be used is that the EN1 is high. When V_{OUT1} regulates at 5V and the clock signal uses V_{OUT1} as its power supply, the charge pump circuit can generate 15V DC voltage approximately. The example of charge pump circuit is shown in typical application circuit.

Soft-Stop (PWMs)

In the event of PWM under-voltage or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the PWM output voltages to low voltage by the soft stop method. The reference remains active to provide an accurate threshold and to provide over-voltage protection.

Power Good Indicator (PWMs)

When the junction temperature increases above the rising threshold temperature 160°C, the IC will enter the over temperature protection (OTP). When the OTP occurs, LDO and PWM controllers circuitry shuts down. It is non-latch protection.

Current Limit (PWMs)

The current limit circuit employs a "valley" current-sensing algorithm (See Figure 1). The APW8833A uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

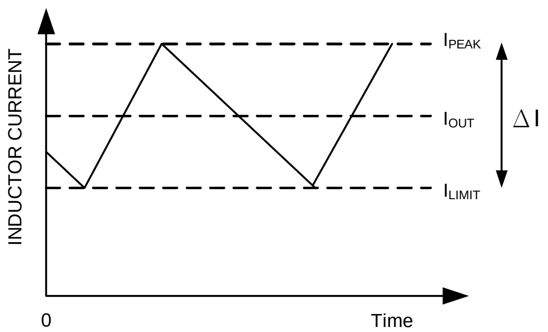


Figure 1. Current Limit Algorithm

Function Description (Cont.)

Current Limit (PWMs)(cont.)

Both PWM controllers use the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.

The current Limit threshold of APW8833A is adjusted with an external resistor. The current-limit threshold voltage is 1/8th the voltage at ILIMx pin. As shown in Figure 2.

The voltage at ILIMx pin is equal to 50µA x R_{ILIM}. The logic current limit threshold is default to 250mV value if voltage at ILIMx pin is above 2V. The relationship between the sampled voltage V_{ILIM} and the current limit threshold ILIMIT is given by:

$$\frac{1}{8} \times V_{ILIMX} = I_{LIMIT} \times R_{DS(ON)}$$

Where V_{ILIMX} is the voltage at the ILIMx pin. $R_{DS(ON)}$ is the low side MOSFETs conducive resistance. I_{LIMIT} is the setting current limit threshold. I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

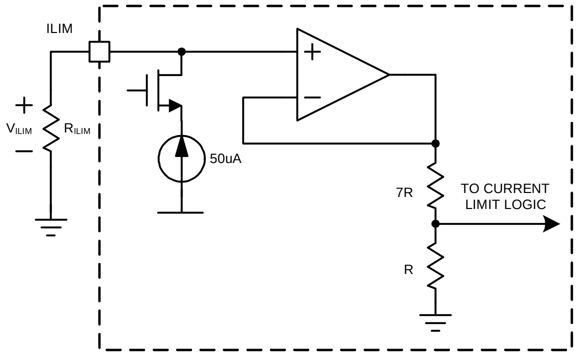


Figure 2. Current-Limit Setting Block Diagram

Table 1. Operating Mode Truth Table

MODE	CONDITION	COMMENT
Run	ENx=1	PWM is in normal operation.
Standby & Soft Stop	ENx=0	PWMx is in shutdown with soft stop function. LDO3 and LDO5 are active.
UVP	Either V_{OUT1}, or V_{OUT2} < 60% of Nominal Output Voltage	The soft stop function will enable to pull low output voltage. LDOx is active. Reset by toggling EN1 and EN2 (logic AND).
OVP	Either V_{OUT1} and V_{OUT2} >115% of Normal Output Voltage	LGATE of the PWM channel, which occurs OVP event is forced high, the other PWM channel is in shutdown with soft stop. LDOx is active. Reset by toggling EN1 and EN2 (logic AND).
OTP	T_J > +160°C	All circuitry off. It is non-latch protection after the junction temperature cools by 25°C.

Function Description (Cont.)

V_{EN1}	V_{EN2}	LDO5	LDO3	PWM1	PWM2	VCLK*
Low	Low	ON	ON	OFF	OFF	OFF
High	High	ON	ON	ON	ON	ON
High	Low	ON	ON	ON	OFF	ON
Low	High	ON	ON	OFF	ON	OFF

* Need connected the correct charge pump circuit on VCLK pin.

Application Information

Output Voltage Selection

The output voltage of PWM1 can be adjusted from 2V to 5.5V with a resistor-driver at FB1 between VOUT1 and GND. Using 1% or better resistors for the resistive divider is recommended. The FB1 pin is the inverter input of the error amplifier, and the reference voltage is 2V. Take the example, the output voltage of PWM1 is determined by:

$$V_{OUTI} = 2 \times \left(1 + \frac{R_{TOP1}}{R_{GND1}}\right)$$

Where R_{TOP1} is the resistor connected from V_{OUTI} to V_{FB1} and R_{GND1} is the resistor connected from FB1 to GND. Similarly, the output voltage of PWM2 can be alsoadjusted from 2V to 5.5V.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Increasing the inductor value and frequency will reduce the ripple current and voltage. However, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter.

The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are remmended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

- For the low-side MOSFET, before it is turned on, the body diode has been conducted. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, the less the $R_{DS(ON)}$ of the low-side MOSFET, the less the power loss. The gate charge for this MOSFET is usually a secondary consideration. The high-side MOSFET does not have this zero voltage switching condition, and because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}{}^2(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}{}^2(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

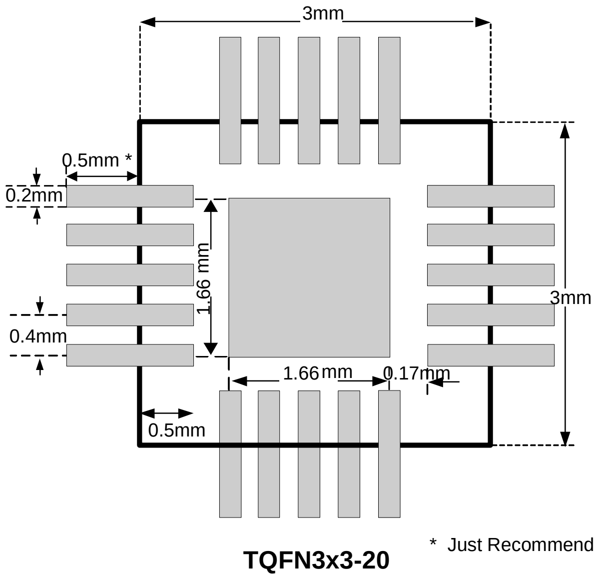
Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

Application Information (Cont.)

Layout Consideration (Cont.)

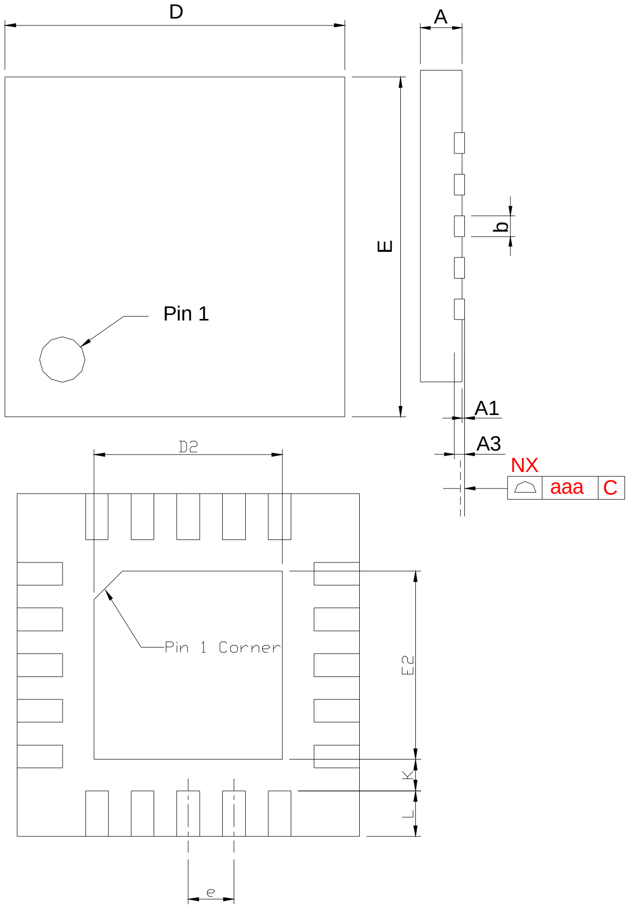
- Keep the switching nodes (UGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes (ILIMx, and FBx) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt, with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATEx and LGATEx) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current-limit stetting resistor should be close to their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placednear the drain).
- The input capacitor should be near the drain of the upper MOSFET; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASEx nodes) should be a large plane for heat sinking. And PHASEx pin traces are also the return path for UGATEx. Connect these pins to the respective converter's upper MOSFET source.
- The controller used ripple mode control. Build the resistor divider close to the FB1 pin so that the high impedance trace is shorter when the output voltage is in ad justable mode. And the FB1 pin traces can't be close to the switching signal traces (UGATEx, LGATEx, BOOTx, and PHASEx).
- The PGND trace should be a separate trace, and independently go to the source of the low-side MOSFETs for current-limit accuracy.



TQFN3x3-20

Package Information

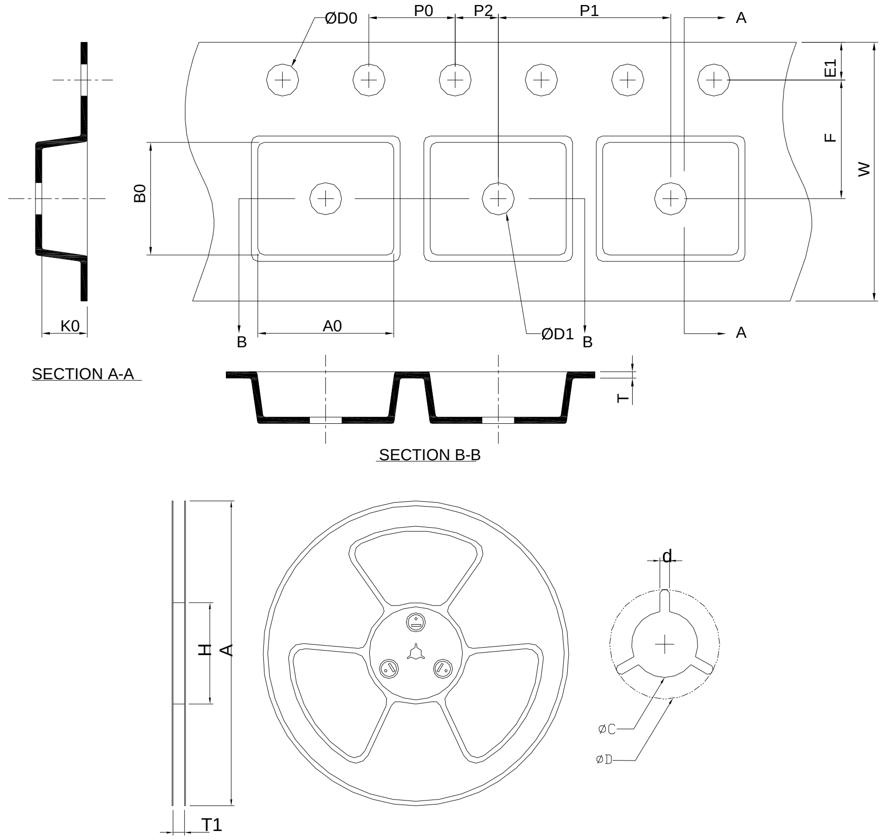
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

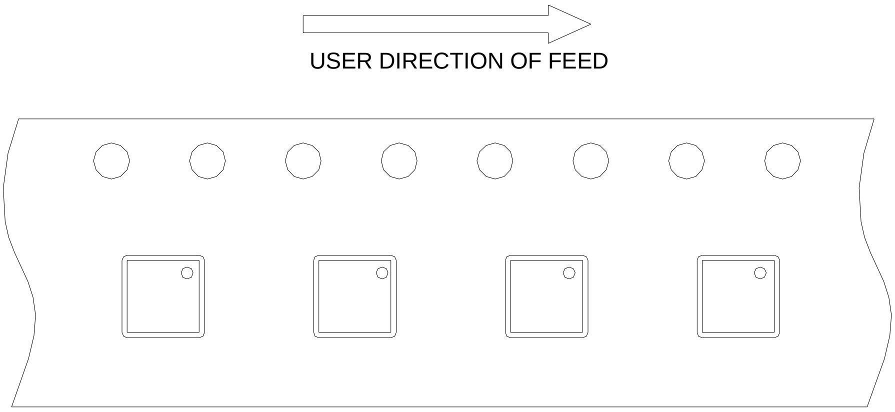
(mm)

Devices Per Unit

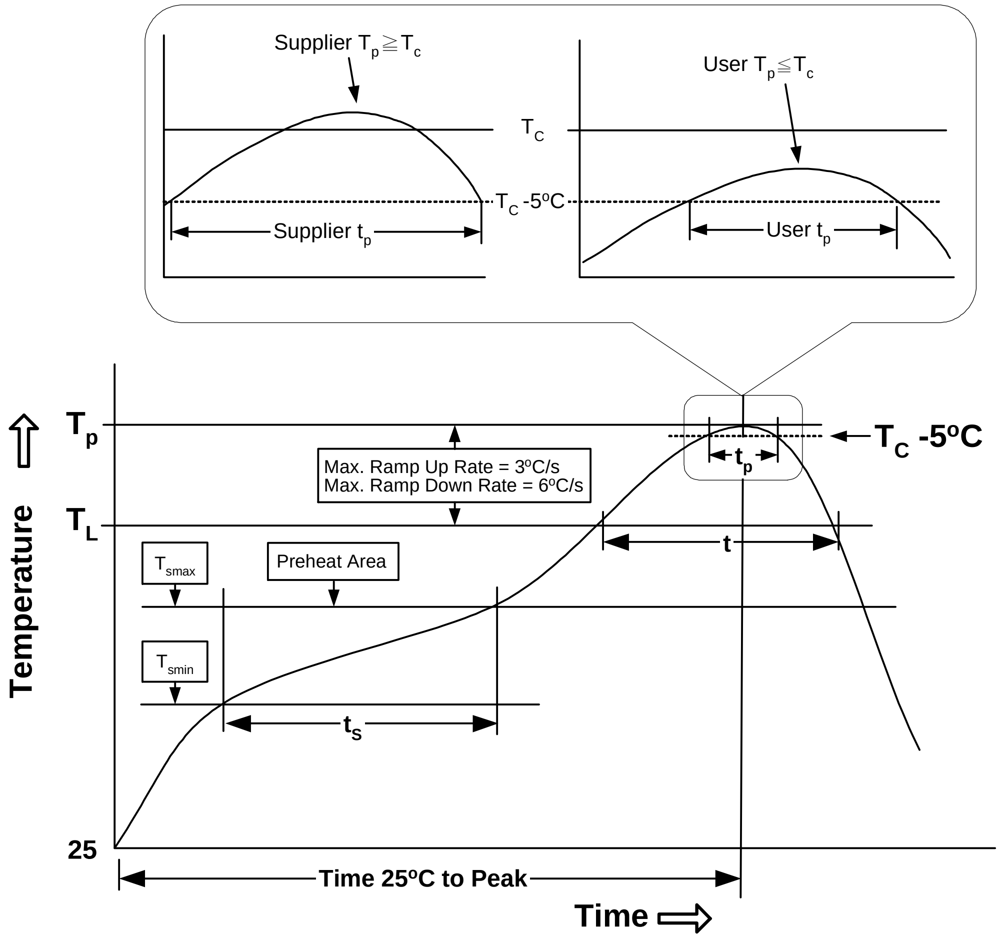
Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test Item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD-78	10ms, 1_{tr}≧100mA

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