3W Mono Class-D Audio Power Amplifier

Features

- **Operating Voltage: 2.4V-5.5V**
- **High Efficiency up to 90%**
- **Low Supply Current**
  - **– I_{DD}=2mA at V_{DD}=5V**
  - **– I_{DD}=1.6mA at V_{DD}=3.6V**
- **Low Shutdown Current**
  - **– I_{DD}=1μA at V_{DD}=5V**
- **Output Power**
  at 1% THD+N (TDFN3x3-8)
  - **– 1.3W, at V_{DD}=5V, R_L=8Ω**
  - **– 0.6W, at V_{DD}=3.6V, R_L=8Ω**
  - **– 2.4W, at V_{DD}=5V, R_L=4Ω (WLCSP-9)**
  - **– 2.1W, at V_{DD}=5V, R_L=4Ω**
  - **– 1.2W, at V_{DD}=3.6V, R_L=4Ω**

  at 10% THD+N (TDFN3x3-8)
  - **– 1.6W, at V_{DD}=5V, R_L=8Ω**
  - **– 0.8W, at V_{DD}=3.6V, R_L=8Ω**
  - **– 3.1W, at V_{DD}=5V, R_L=4Ω (WLCSP-9)**
  - **– 2.65W, at V_{DD}=5V, R_L=4Ω**
  - **– 1.3W, at V_{DD}=3.6V, R_L=4Ω**
- **Less External Components Required**
- **Fast Startup Time (4ms)**
- **High PSRR: 80 dB at 217 Hz**
- **Thermal and Over-Current Protections**
- **Space Saving Packages**
  WLCSP-9 Bump, 3mmx3mm TDFN-8,3mmx3mm DFN-8
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APA2010/2010A is a mono, filter-free Class-D audio amplifier available in WLCSP-9 and TDFN3x3-8 packages. The gain can be set by an external input resistance. High PSRR and differential architecture provide increased immunity to noise and RF rectification. In addition to these features, a fast startup time and small package size make the APA2010/2010A an ideal choice for both cellular handsets and PDAs.

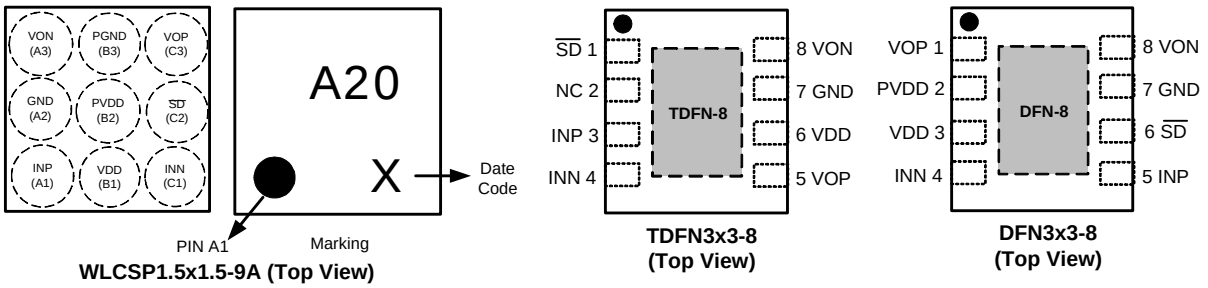
The APA2010/2010A is capable of driving 1.5W at 5V or 730mW at 3.6V into 8Ω. It is also capable of driving 4Ω. The APA2010/2010A is designed with a Class-D architecture and operating with highly efficiency compared with Class-AB amplifier. It's suitable for power sensitive application, such as battery powered devices. The filter-free architecture eliminates the output filter, reduces the external component count, board area, and system costs, and simplifies the design.

Moreover, the APA2010/2010A provides thermal and over-current protections.

Applications

- **Mobile Phones**
- **Handsets**
- **PDAs**
- **Portable multimedia devices**

Pin Configuration (Note 1)



Note 1: The marking for APA2010 is “A20” and “A21” is for APA2010A.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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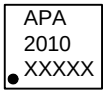
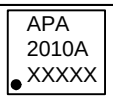
Ordering and Marking Information

APA2010 □□□-□□ □ APA2010A Assembly Material Handling Code Temperature Range Package Code	Package Code HA : WLCSP1.5x1.5-9A QB : TDFN3x3-8 QA : DFN3x3-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2010 HA: 	X - Date Code
APA2010A HA: 	X - Date Code
APA2010 QB/QA: 	XXXXX - Date Code
APA2010A QB/QA: 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 2)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (VDD, PVDD)	-0.3 to 6	V
V_{IN}, $V_{\overline{SD}}$	Input Voltage ($\overline{SD}$, INP, INN)	-0.3 to 6	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note 2 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 3) WLCSP1.5x1.5-9A TDFN3x3-8	 165 50	°C/W

Note 3 : Please refer to " Layout Recommendation", the ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		2.4	5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$	1	-	V
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$	-	0.35	V

Electrical Characteristics

V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2010/2010A			Unit
				Min.	Typ.	Max.	
I_{DD}	Supply Current			-	2	-	mA
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V		-	1	-	μA
I_i	Input current	$\overline{SD}$		-	0.1	-	μA
F_{osc}	Oscillator Frequency			200	250	310	kHz
R_{DSCON}	Static drain-source on-state resistance	V_{DD} = 5V	P-Channel MOSFET (WLCSP1.5X1.5-9A)	-	340	-	mΩ
			N-Channel MOSFET (WLCSP1.5X1.5-9A)	-	195	-	
		V_{DD} = 3.6V	P-Channel MOSFET (WLCSP1.5X1.5-9A)	-	400	-	
			N-Channel MOSFET (WLCSP1.5X1.5-9A)	-	215	-	
		V_{DD} = 2.4V	P-Channel MOSFET (WLCSP1.5X1.5-9A)	-	550	-	
			N-Channel MOSFET (WLCSP1.5X1.5-9A)	-	260	-	
V_{DD}=5V, T_A=25℃							
P_O	Output Power	THD+N = 1%, f_{in} = 1kHz	R_L = 4Ω (WLCSP1.5X1.5-9A)	-	2.45	-	W
			R_L = 4Ω	-	2.1	-	
			R_L = 8Ω (WLCSP1.5X1.5-9A)	-	1.45	-	
			R_L = 8Ω	1	1.3	-	
		THD+N = 10%, f_{in} = 1kHz	R_L = 4Ω (WLCSP1.5X1.5-9A)	-	3.1	-	
			R_L = 4Ω	-	2.65	-	
			R_L = 8Ω (WLCSP1.5X1.5-9A)	-	1.8	-	
			R_L = 8Ω	-	1.6	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	R_L = 4Ω P_O= 1.6W	-	0.3	-	%
			R_L = 8Ω P_O= 0.96W	-	0.1	-	
PSRR	Power Supply Rejection Ratio	R_L = 8Ω, f_{in} = 217Hz		-	80	-	dB
V_{OS}	Output Offset Voltage	R_L = 8Ω				25	mV

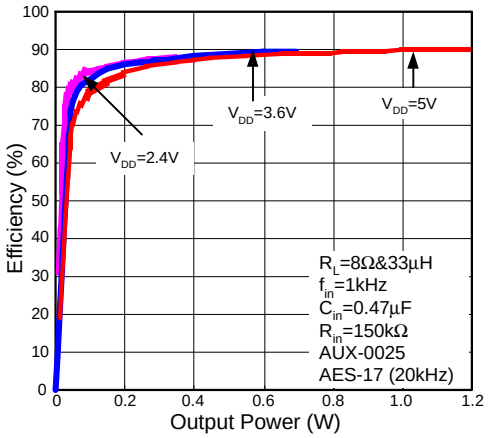
Electrical Characteristics (Cont.)

V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

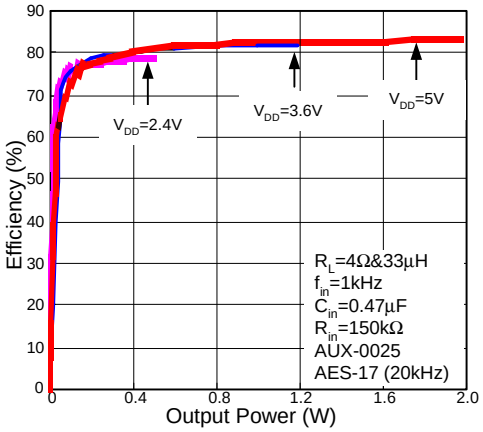
Symbol	Parameter	Test Conditions		APA2010/2010A			Unit
				Min.	Typ.	Max.	
S/N		With A-weighting Filter P_O = 0.96W, R_L = 8Ω		90	-	dB	S/N
Vn	Noise Output Voltage	With A-weighting Filter		100	-	μV (rms)	Vn
V_{DD}=3.6V, T_A=25℃							
P_O	Output Power	THD+N = 1%, f_{in} = 1kHz	R_L = 4Ω (WLCSP1.5X1.5-9A)	-	1.2	-	W
			R_L = 4Ω	-	1.1	-	
			R_L = 8Ω (WLCSP1.5X1.5-9A)	-	0.75	-	
			R_L = 8Ω	-	0.6	-	
		THD+N = 10%, f_{in} = 1kHz	R_L = 4Ω (WLCSP1.5X1.5-9A)	-	1.5	-	
			R_L = 4Ω	-	1.35	-	
			R_L = 8Ω (WLCSP1.5X1.5-9A)	-	0.95	-	
			R_L = 8Ω	-	0.8	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	R_L = 4Ω P_O = 0.82W,	-	0.35	-	%
			R_L = 8Ω P_O= 0.45W	-	0.1	-	
PSRR	Power Supply Rejection Ratio	R_L = 8Ω, f_{in} = 217Hz		-	75	-	dB
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	-	25	mV
S/N		With A-weighting Filter P_O= 0.43W, R_L = 8Ω,		-	85	-	dB
Vn	Noise Output Voltage	With A-weighting Filter		-	105	-	μV (rms)
V_{DD}=2.5V, T_A=25℃							
P_O	Output Power	THD+N = 1%, f_{in} = 1kHz	R_L = 4Ω	-	0.45	-	W
			R_L = 8Ω	-	0.3	-	
		THD+N =10%, f_{in} = 1kHz	R_L = 4Ω	-	0.55	-	
			R_L = 8Ω	-	0.35	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	P_O = 0.34W, R_L = 4Ω	-	0.35	-	%
			P_O = 0.22W, R_L = 8Ω	-	0.2	-	
PSRR	Power Supply Rejection Ratio	R_L = 8Ω, f_{in} = 217Hz		-	70	-	dB
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	-	25	mV
S/N		With A-weighting Filter P_O = 0.2W, R_L = 8Ω		-	83	-	dB
Vn	Noise Output Voltage	With A-weighting Filter		-	120	-	μV (rms)

Typical Operating Characteristics

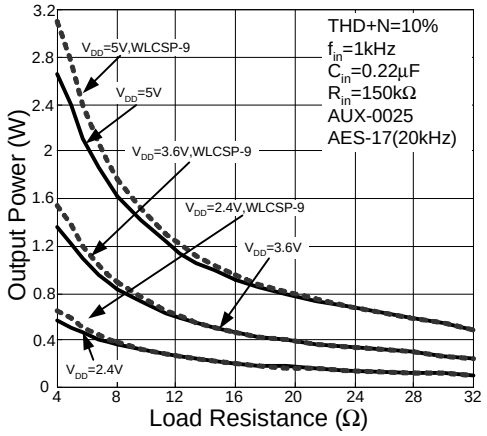
Efficiency vs. Output Power



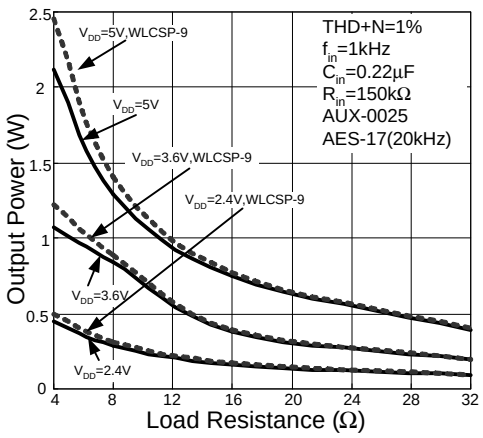
Efficiency vs. Output Power (4W)



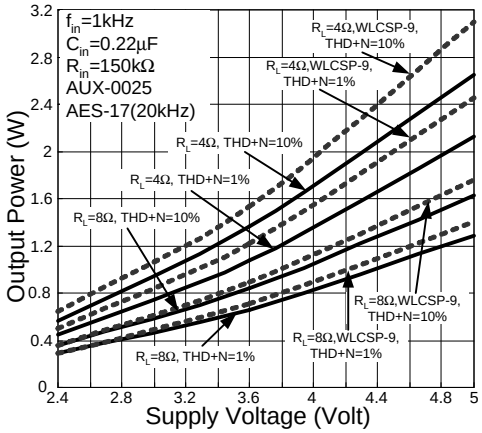
Output Power vs. Load Resistance



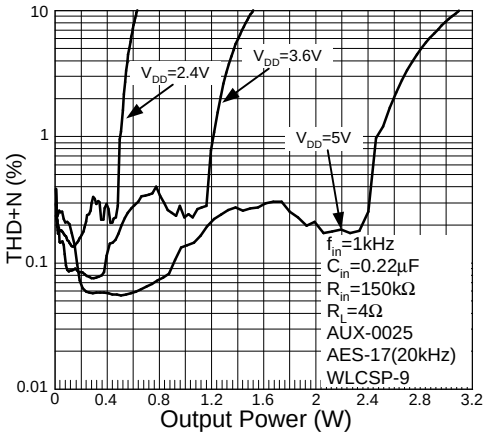
Output Power vs. Load Resistance



Output Power vs. Supply Voltage

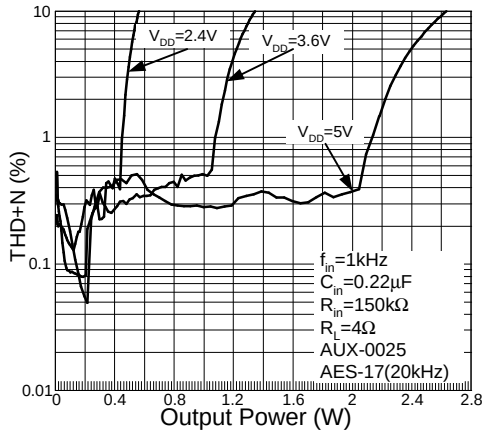


THD+N vs. Output Power

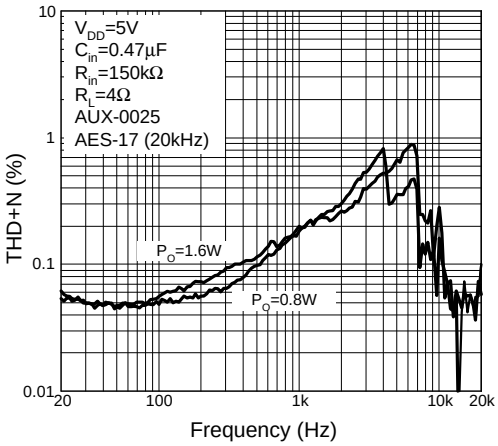


Typical Operating Characteristics (Cont.)

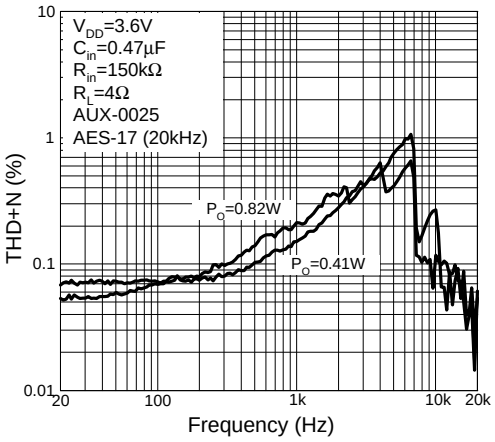
THD+N vs. Output Power



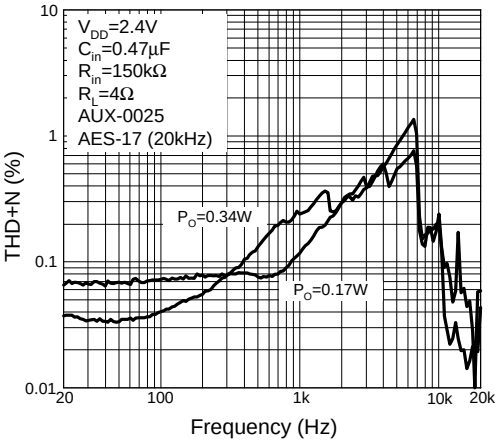
THD+N vs. Frequency



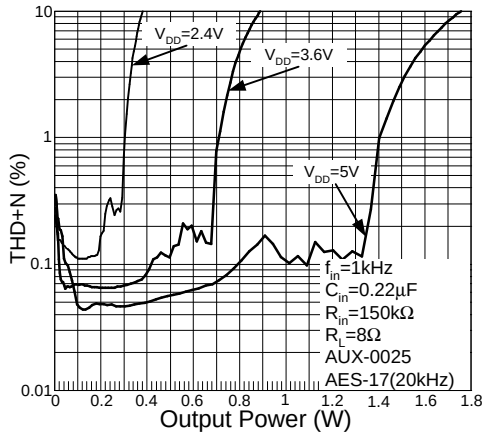
THD+N vs. Frequency



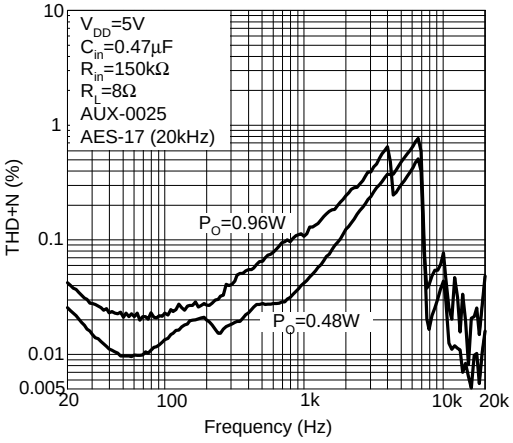
THD+N vs. Frequency



THD+N vs. Output Power

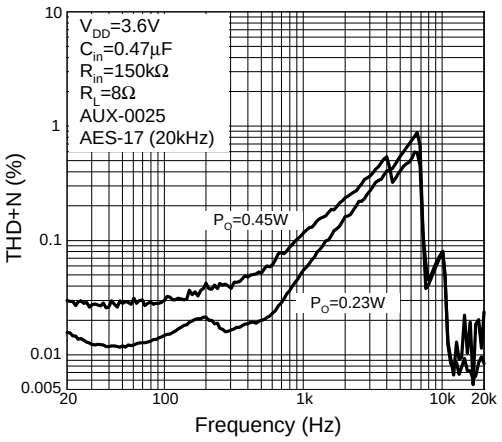


THD+N vs. Frequency

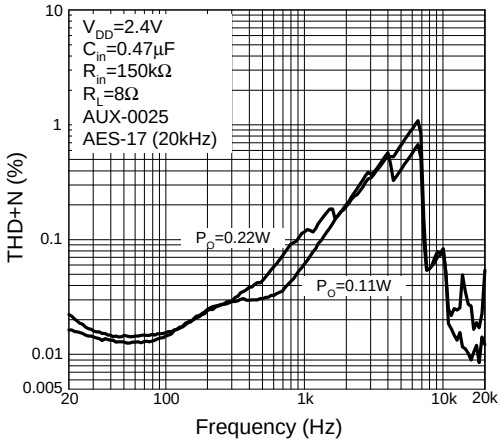


Typical Operating Characteristics (Cont.)

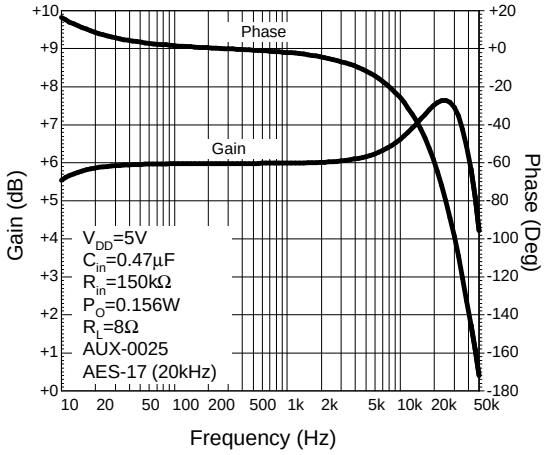
THD+N vs. Frequency



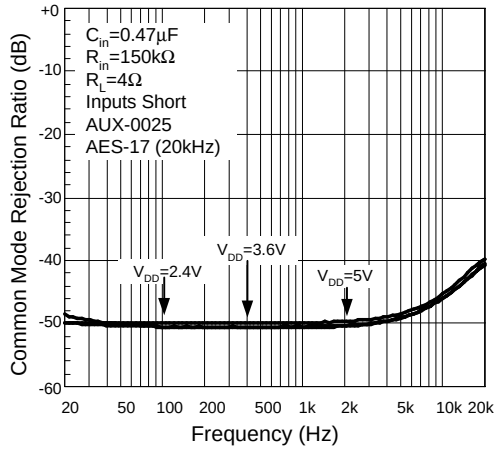
THD+N vs. Frequency



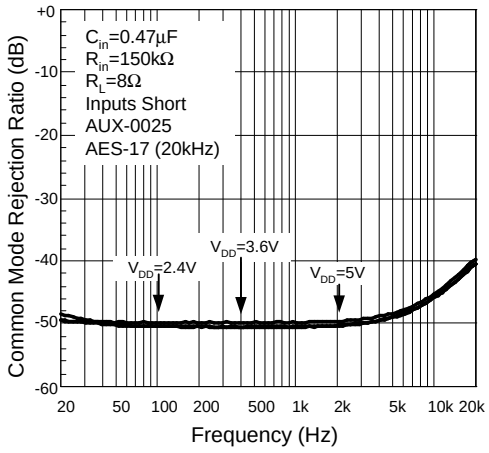
Frequency Response



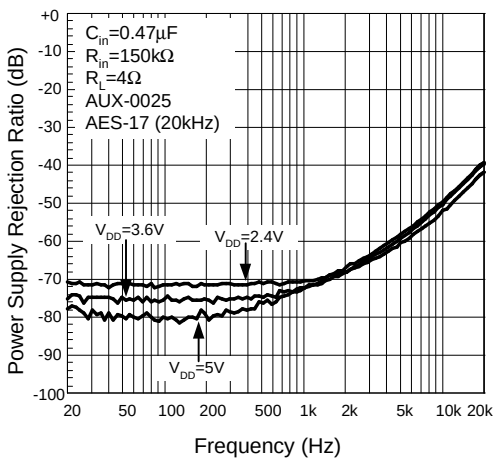
CMRR vs. Frequency



CMRR vs. Frequency

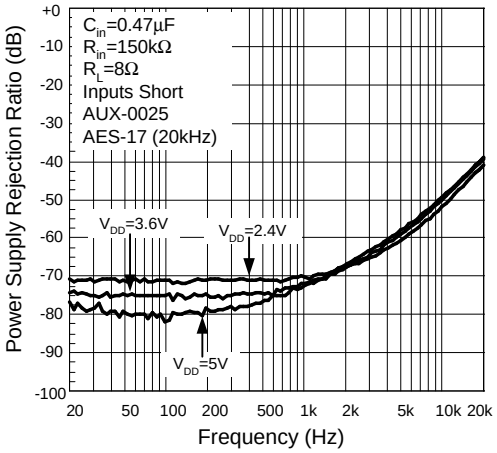


PSRR vs. Frequency

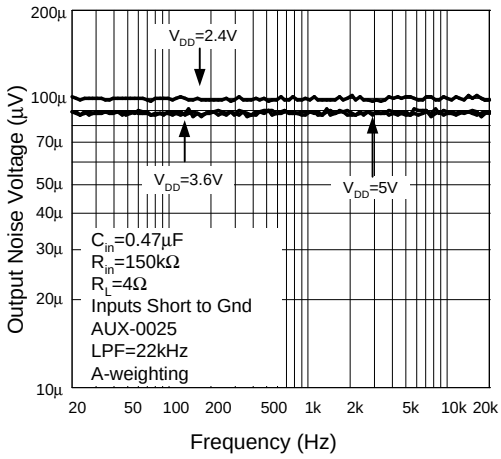


Typical Operating Characteristics (Cont.)

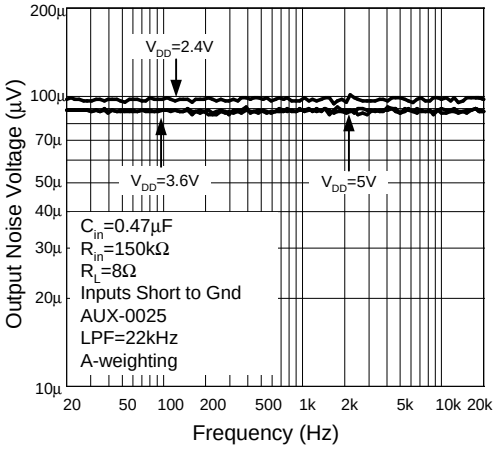
PSRR vs. Frequency



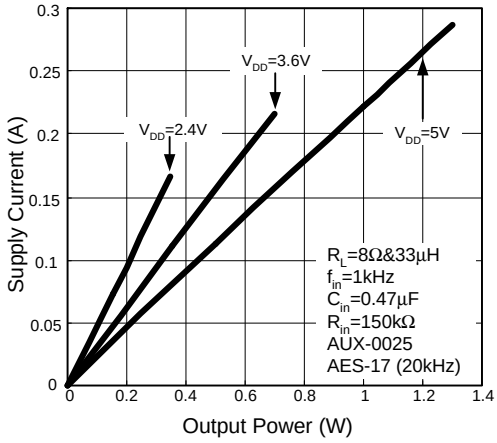
Output Noise Voltage vs. Frequency



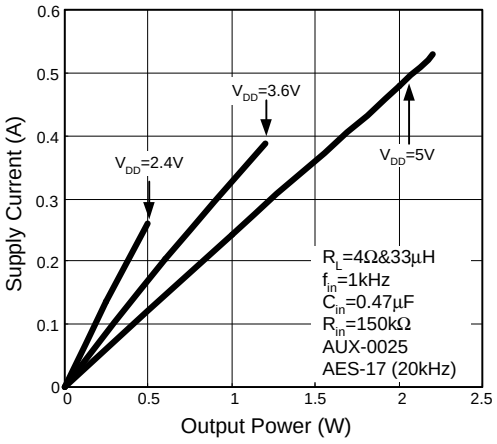
Output Noise Voltage vs. Frequency



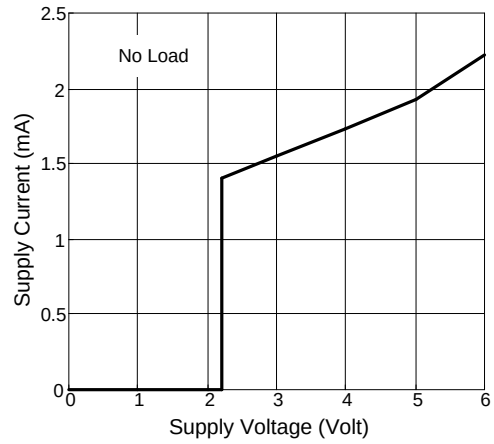
Supply Current vs. Output Power



Supply Current vs. Output Power

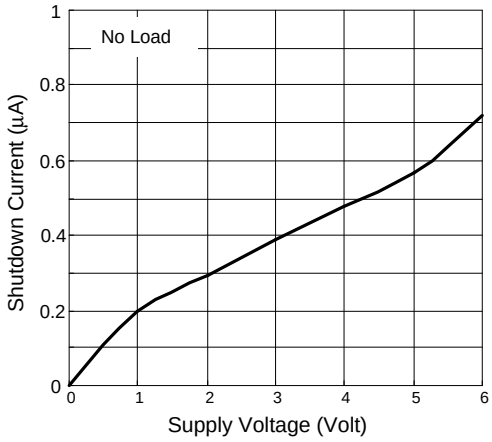


Supply Current vs. Supply Voltage

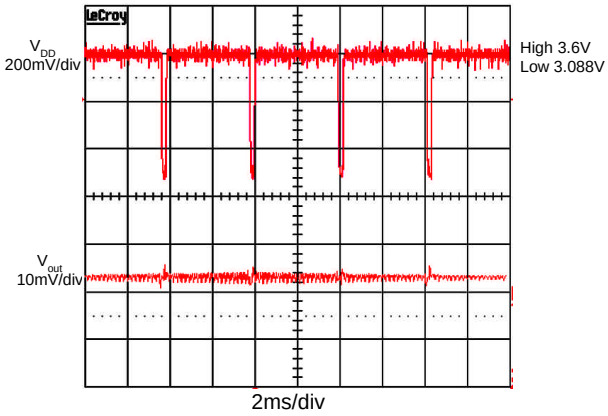


Typical Operating Characteristics (Cont.)

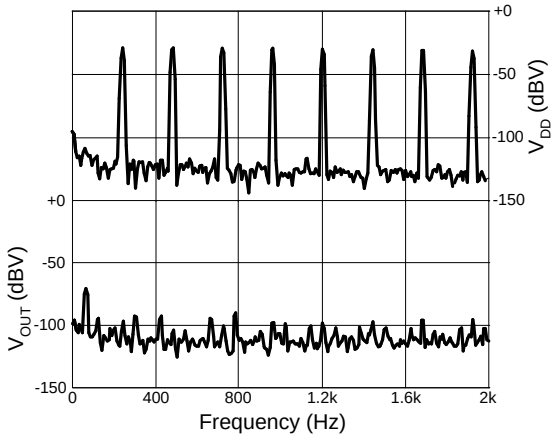
Shutdown Current vs. Supply Voltage



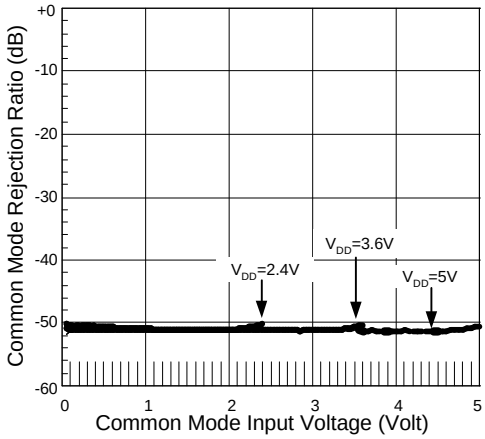
GSM Power Supply Rejection vs. Time



GSM Power Supply Rejection vs. Frequency



Common Mode Rejection ratio vs. Common Mode Input Voltage



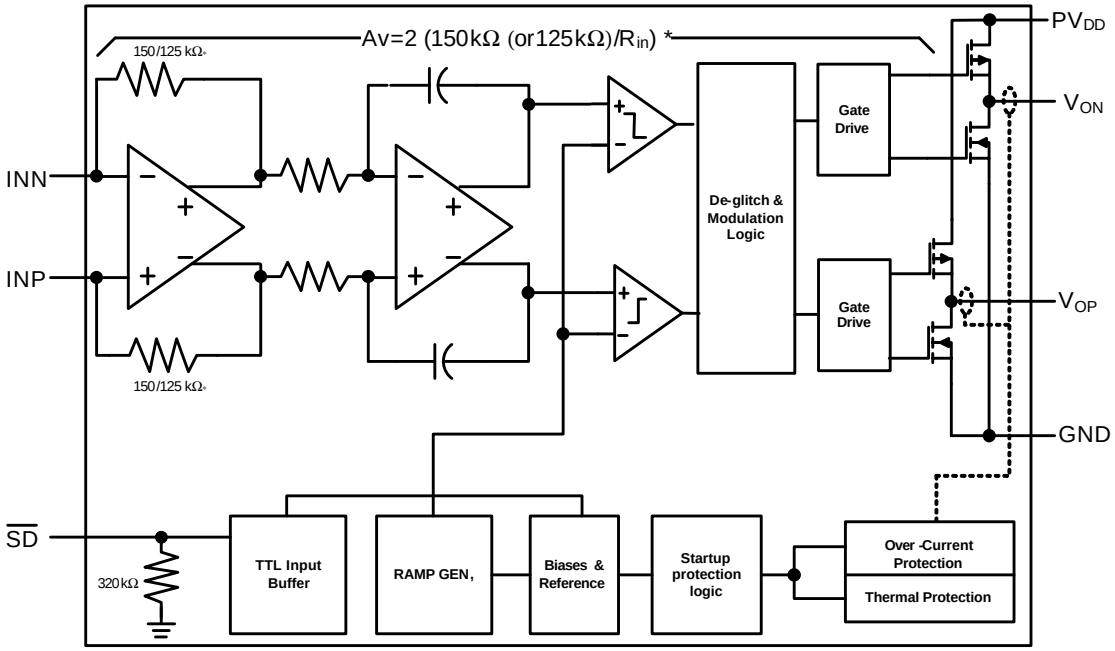
Pin Description

PIN (WLCSP1.5X1.5-9A)		I/O	FUNCTION
NO.	NAME		
A1	INP	I	The non-inverting input of amplifier. INP is connected to Gnd via a capacitor for single-end (SE) input signal.
A2	GND	-	Ground connection for circuitry.
A3	VON	O	The negative output terminal of Class-D amplifier.
B1	VDD	-	Supply voltage input pin.
B2	PVDD	-	Supply voltage only for power stage.
B3	PGND	-	Ground connection for power stage
C1	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
C2	$\overline{SD}$	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.
C3	VOP	O	The positive output terminal of Class-D amplifier.

PIN (TDFN3x3-8)		I/O	FUNCTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.
2	NC	-	No connection.
3	INP	I	The non-inverting input of amplifier. INP is connected to Gnd via a capacitor for single-end (SE) input signal.
4	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
5	VOP	O	The positive output terminal of Class-D amplifier.
6	VDD	-	Supply voltage input pin
7	GND	-	Ground connection.
8	VON	O	The negative output terminal of Class-D amplifier.

PIN (DFN3x3-8)		I/O	FUNCTION
NO.	NAME		
6	$\overline{SD}$	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.
2	PVDD	-	Supply Voltage only for power stage.
5	INP	I	The non-inverting input of amplifier. INP is connected to Gnd via a capacitor for single-end (SE) input signal.
4	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
1	VOP	O	The positive output terminal of Class-D amplifier.
3	VDD	-	Supply voltage input pin
7	GND	-	Ground connection.
8	VON	O	The negative output terminal of Class-D amplifier.

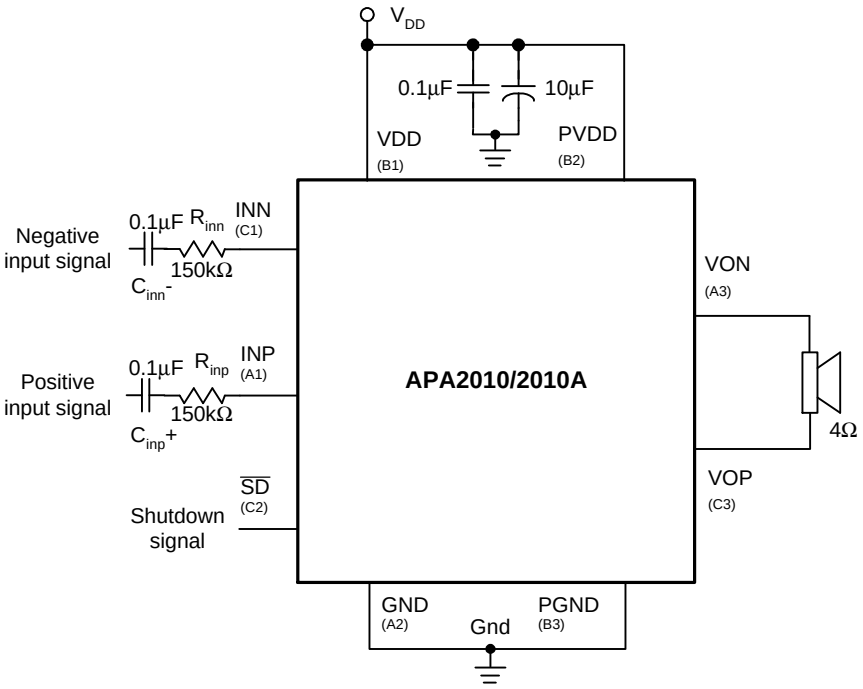
Block Diagram



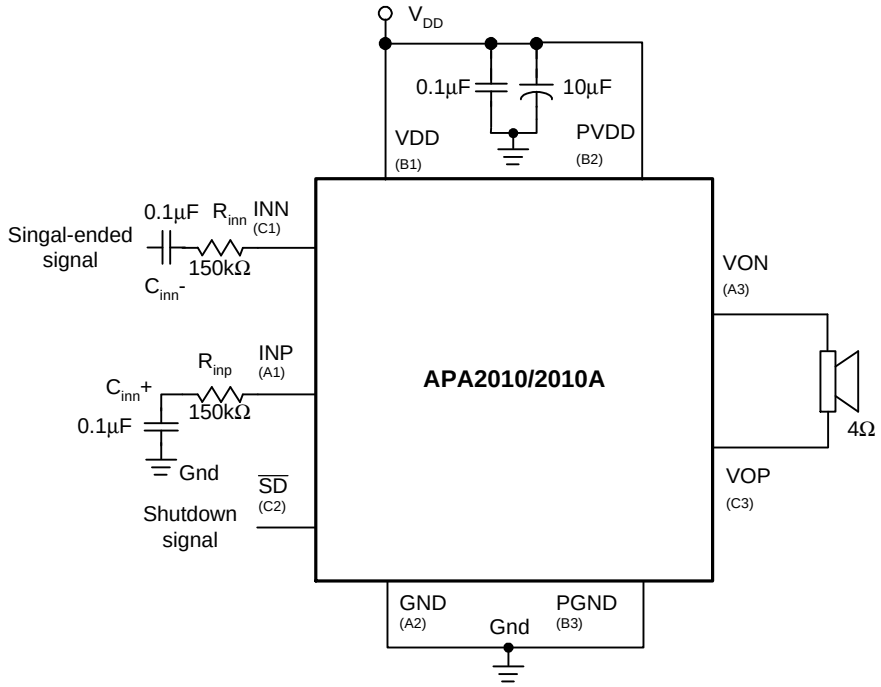
* APA2010 : 150kΩ, APA2010A : 125kΩ

Typical Application Circuit

Differential input mode (WLCSP1.5x1.5-9A)



Single-ended input mode (WLCSP1.5x1.5-9A)



Application Information

Fully Differential Amplifier

The APA2010/2010A is a fully distinctive amplifier with differential inputs and outputs. Compare with the traditional amplifiers, the fully differential amplifier has some advantages. Firstly, there is no need for the input coupling capacitors because the common-mode feedback will compensate the input bias. The inputs can be biased from 0.5V to V_{DD}-0.5V, and the outputs still be biased at mid-supply of APA2010/2010A. If the inputs are biased out of the input range, the coupling capacitors are required. Secondly, there is no need for the mid-supply capacitor (C_B) either because any shift of the mid-supply of APA2010/2010A will have the same affection on both positive & negative channel, and will cancel at the differential outputs. Thirdly, the fully differential amplifier will cancel the GSM RF transmitter's signal (217Hz).

Class-D Operation

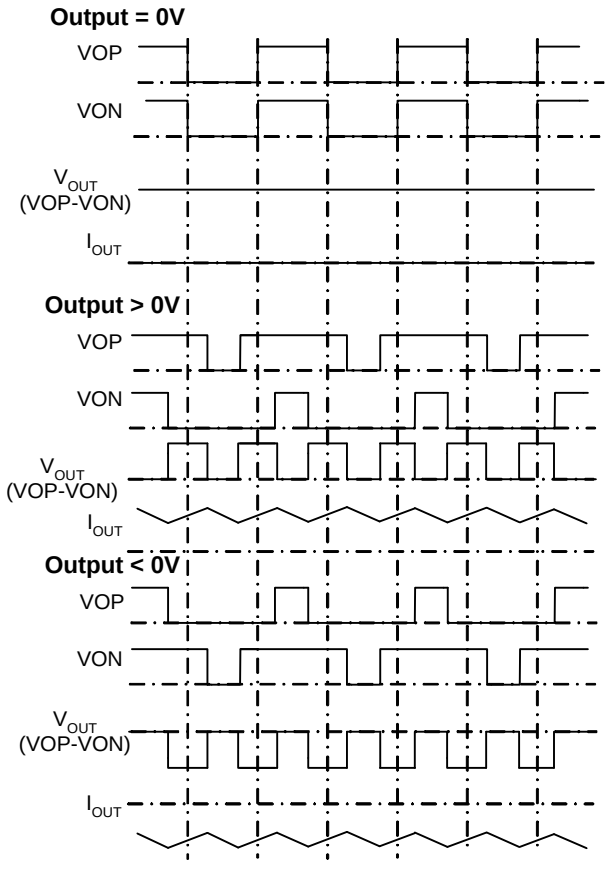


Figure 1. The Class-D Power Amplifier Output Waveform (Voltage & Current)

The APA2010/2010A modulation scheme is shown in figure 1. The outputs VOP and VON are in phase with each other when no input signals. When output > 0V, the duty cycle of VOP is greater than 50% and VON is less than 50%; on the contrary, when output <0V, the duty cycle of VOP is less than 50% and VON is greater than 50%. This method reduces the switching current across the load and the I^2R losses in the load which can improve the amplifier's efficiency.

This modulation scheme has very short pulses across the load which results in the small ripple current and very little loss on the load. Meanwhile, the LC filter can be eliminated in most applications. Adding the LC filter can increase the efficiency by filtering the ripple current.

Square Wave Into the Speaker

Applying the square wave into the speaker may cause the voice coil of speaker jumping out the air gap and defacing the voice coil. However, this depends on if the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 250kHz switching frequency, this is not an issue for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistance, R_{in}

The gain of the APA2010/2010A has been set by the external resistors (R_{in}).

$$Gain(Av) = \frac{2X150k\Omega\ (or\ 125k\Omega)}{R_{in}} \qquad (1)$$

For fully differential operating, the R_{in} match is very important for CMRR, PSRR and harmonic distortion performance. It's recommended to use 1% tolerance resistor or better. Keeping the input trace as short as possible to limit the noise injection.

The gain is recommended to set as 2V/V or lower for APA2010/2010A's optimal performance.

Input Capacitor, C_{in}

In the typical application, an input capacitor, C_{in}, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_{in} and the

Application Information (Cont.)

Input Capacitor, C_i (Cont.)

minimum input impedance R_{in} from a high-pass filter with the corner frequency are determined in the following equation:

$$F_{C(highpass)} = \frac{1}{2\pi R_{in} C_{in}} \quad (2)$$

The value of C_{in} must be considered carefully because it directly affects the low frequency performance of the circuit. For example, when R_{in} is 150kΩ and the specification calls for a flat bass response are down to 20Hz. The equation is reconfigured as below:

$$C_{in} = \frac{1}{2\pi R_{in} F_c} \quad (3)$$

When input resistance is considered, the C_{in} is 0.05µF. Therefoe, a value in the range of 0.068µF to 0.1µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_{in} + R_f, C_{in}) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' inputs are held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Output Capacitor, C_o

If the user wants to add capacitor at output without ferrite bead and inductor, please note the output capacitor should not be greater than 1nf (V_{DD}=4.2V). The high value of output capacitor maybe trigger the OCP (Over-Current Protection) of APA2010/2010A.

Power Supply Decoupling, C_s

The APA2010/2010A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device VDD pin for the best operation. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater is placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption while not in use, the APA2010/2010A contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2010/2010A. It suggests to switch to either ground or the supply voltage VDD to provide maximum device performance. By switching the $\overline{SD}$ pin to a low level, the amplifier enters a low-consumption-current state, and then the APA2010/2010A is in shutdown mode. In normal operating, APA2010/2010A's $\overline{SD}$ pin should be pulled to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Output LC Filter

If the traces from the APA2010/2010A to speaker are short, the APA2010/2010A doesn't require output filter for FCC & CE standard.

A ferrite bead may be needed if it's failing the test for FCC or CE is tested without the LC filter. The Figure 2 is the sample for adding ferrite bead; the ferrite shows when choosing high impedance in high frequency.

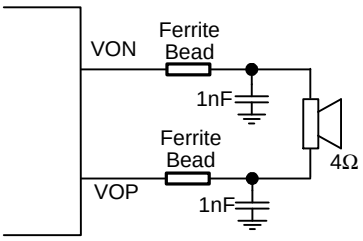


Figure 2. Ferrite bead output filter

Application Information (Cont.)

Output LC Filter (Cont.)

Figure 3 is an example for adding the LC filter. It's recommended to eliminate the radiated emission or EMI when the trace from amplifier to speaker is too long.

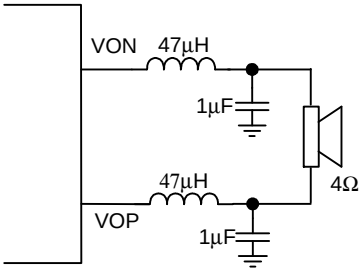


Figure 3. LC output filter

Figure 3's low pass filter cut-off frequency is F_C

$$F_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

Mixing Two Single-Ended Input Signals

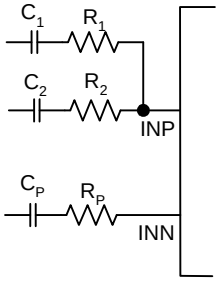


Figure 4. Mixing Two Single-Ended Input Signals

For mixing two Single-Ended (SE) input signals, please refer to Figure 4. The gains of each input can be set difference:

$$A_V(1) = \frac{2\times 150k\Omega\ (or\ 125k\Omega)}{R_1} \quad (5)$$

$$A_V(2) = \frac{2\times 150k\Omega\ (or\ 125k\Omega)}{R_2} \quad (6)$$

The corner frequency of each input high- pass-filter also can be set by R_1&C_1, and R_2&C_2.

The non-inverting input's resistor (R_P) and capacitor (C_P) need to match the impedances of invert inputs.

$$C_P = C_1 // C_2 = C_1 + C_2 \quad (7)$$

$$R_P = R_1 // R_2 = \frac{R_1\times R_2}{R_1 + R_2} \quad (8)$$

Layout Recommendation

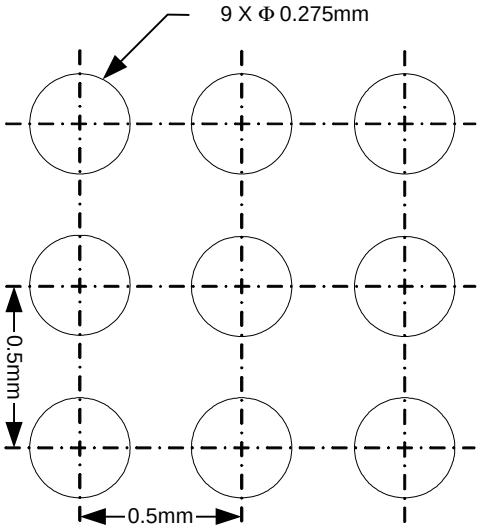


Figure 5. WLCSP-9 land pattern recommendation

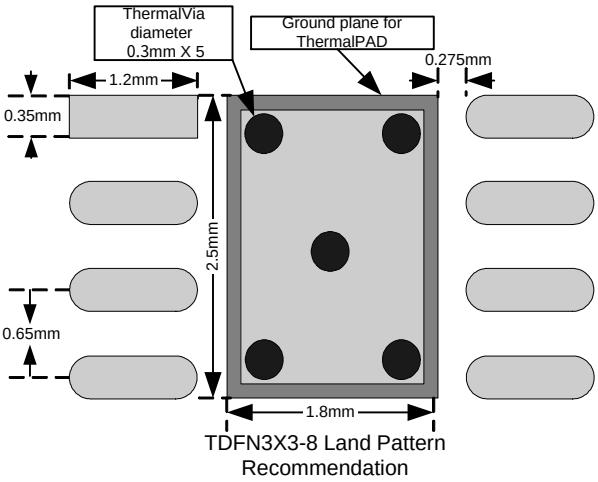


Figure 6. TDFN3x3-8 Layout Recommendation

1. All components should be placed close to the APA2010/2010A. For example, the input resistor (R_{in}) should be close to APA2010/2010A's input pins to avoid causing noise coupling to APA2010/2010A's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2010/2010A's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.

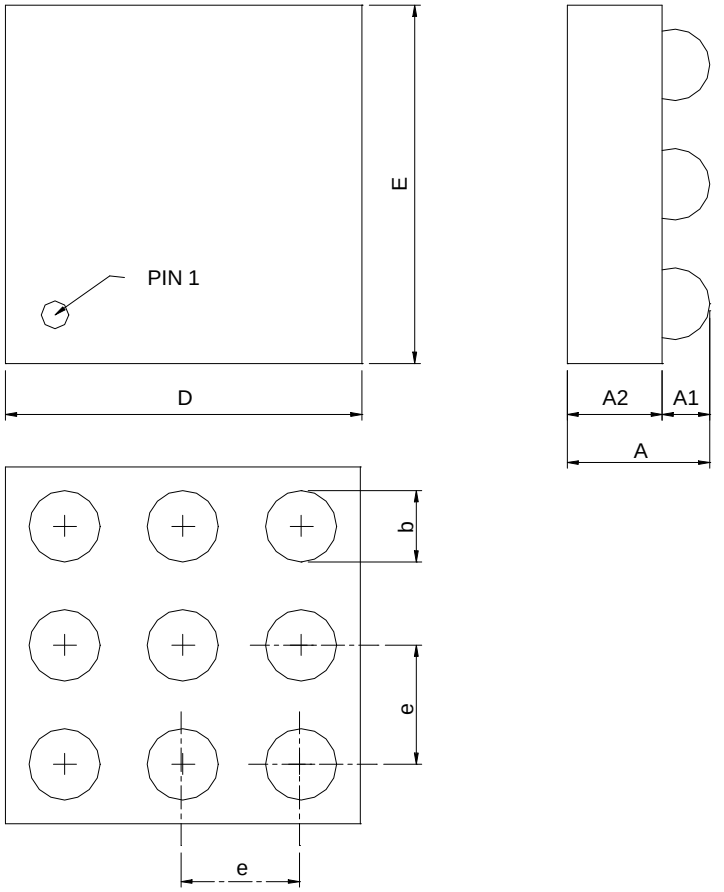
Application Information (Cont.)

Layout Recommendation (cont.)

3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The TDFN3X3-8 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

Package Information

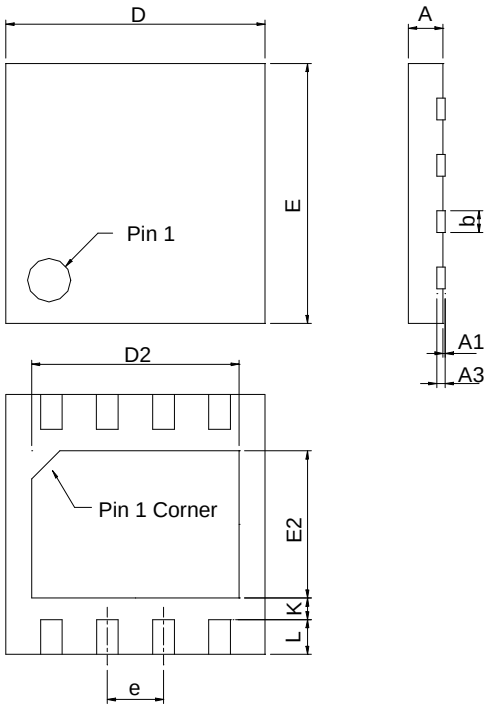
WLCSP1.5x1.5-9A



SYMBOL	WLCSP1.5x1.5-9A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.53	0.67	0.021	0.026
A1	0.20	0.24	0.008	0.009
A2	0.33	0.43	0.013	0.017
b	0.29	0.31	0.011	0.012
D	1.42	1.50	0.056	0.059
E	1.42	1.50	0.056	0.059
e	0.50 BSC		0.020 BSC	

Package Information

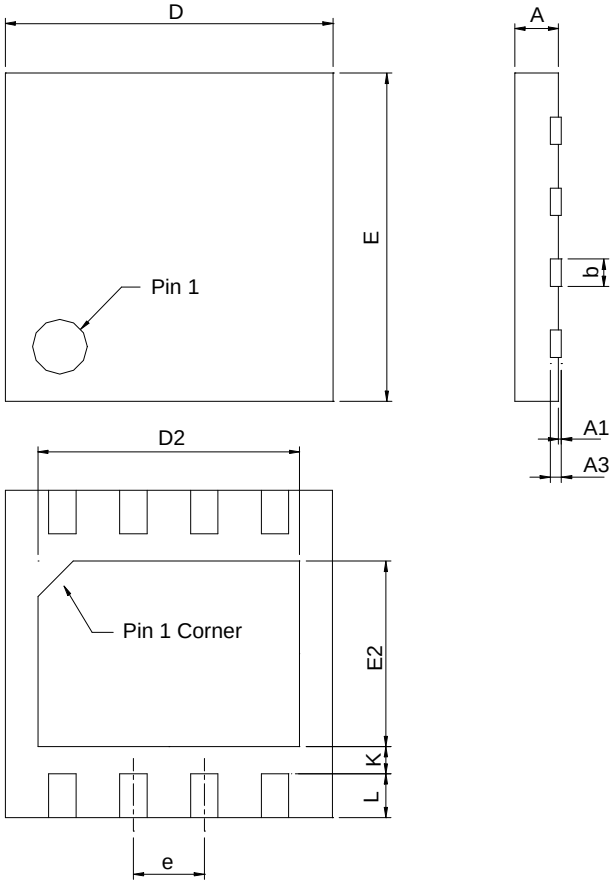
TDFN3x3-8



SYMBOL	TDFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	2.90	3.10	0.114	0.122
D2	1.90	2.40	0.075	0.094
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

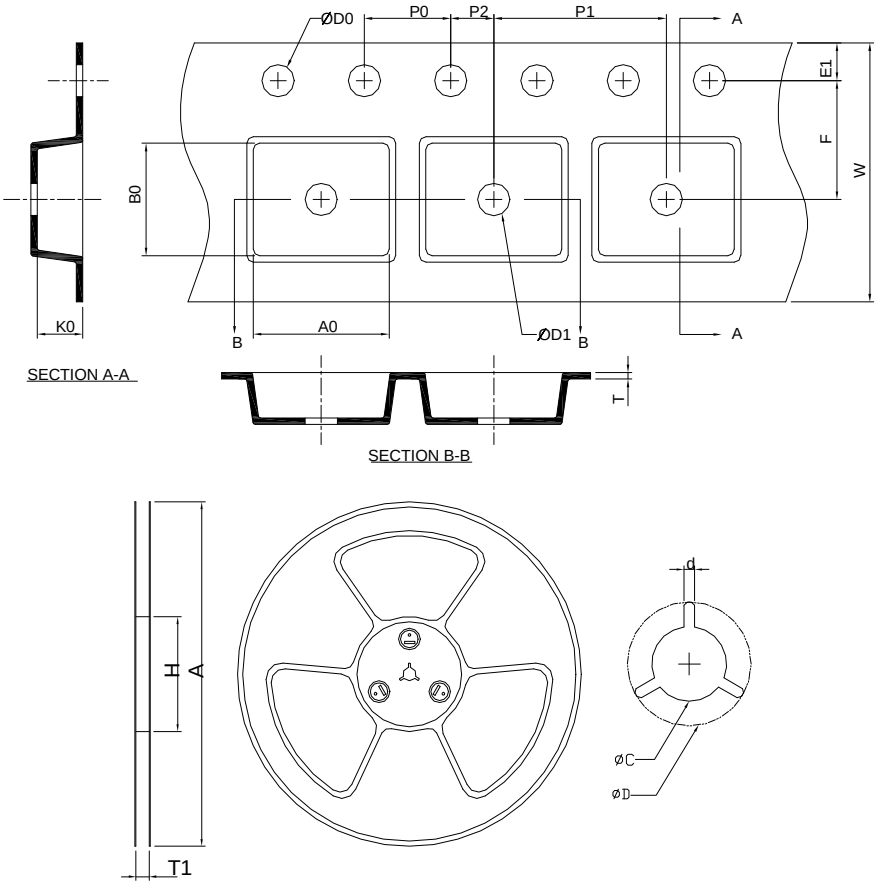
Package Information

DFN3x3-8



SYMBOL	DFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	2.90	3.10	0.114	0.122
D2	1.90	2.40	0.075	0.094
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Carrier Tape & Reel Dimensions



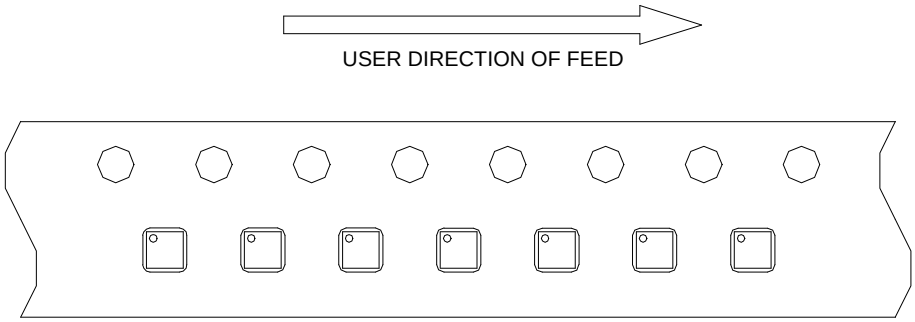
Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.5X1.5-9A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.70±0.20	1.70±0.20	0.90±0.20
Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20
Application	A	H	T1	C	d	D	W	E1	F
DFN3x3-8	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

Devices Per Unit

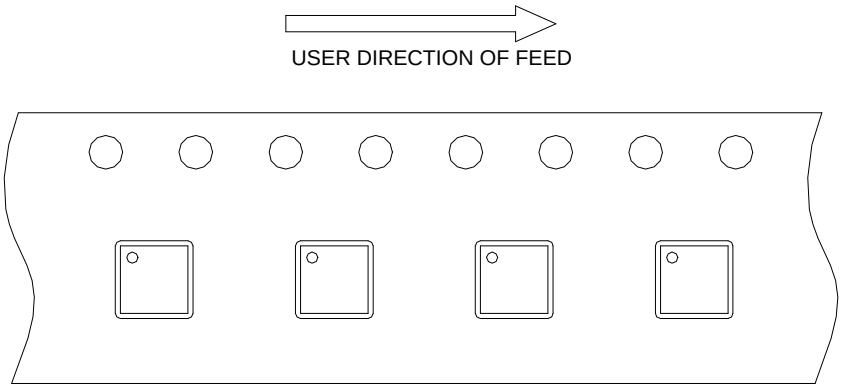
Package Type	Unit	Quantity
WLCSP1.5X1.5-9A	Tape & Reel	3000
TDFN3x3-8	Tape & Reel	3000
DFN3x3-8	Tape & Reel	3000

Taping Dircetion Information

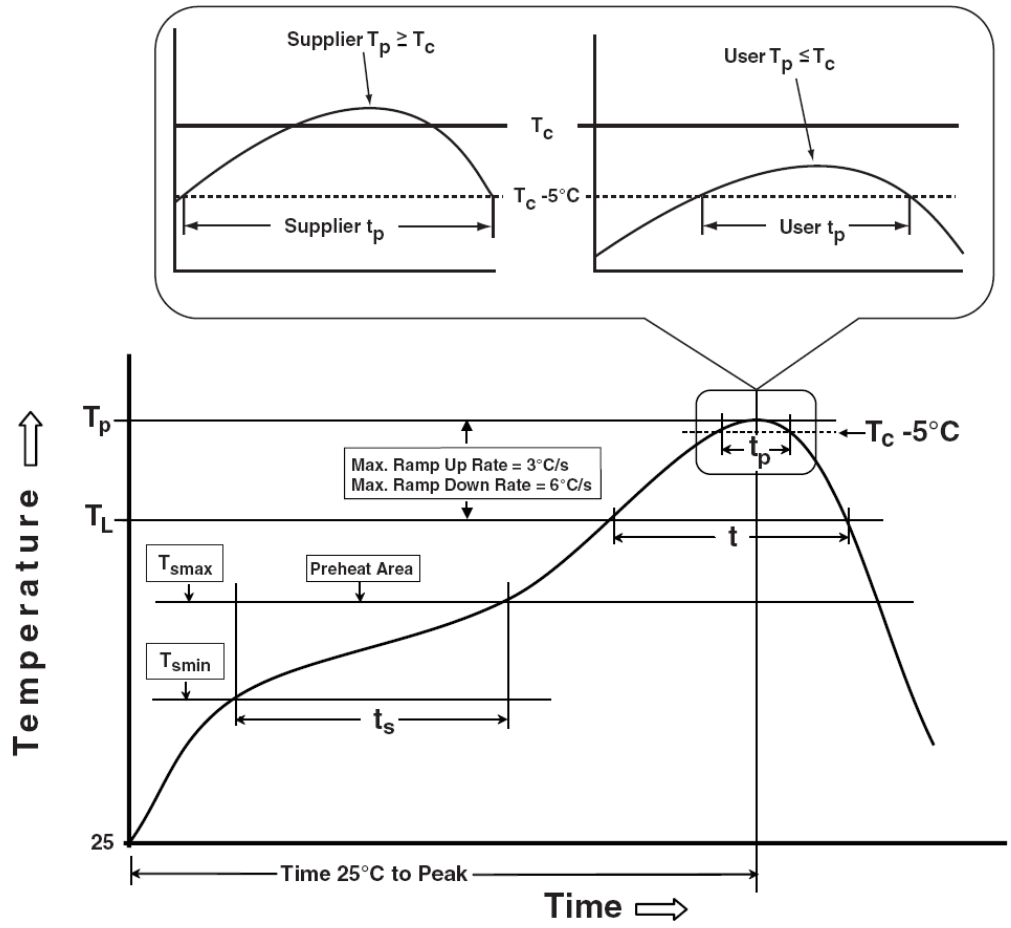
WLCSP1.5x1.5-9A



TDFN3x3-8/DFN3x3-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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