96 Channel LED Controller for LCD Backlight

Features

- **Wide range input is 4.5V to 24V**
- **High Accurate LED Current 2% Typ. (ILED = 20mA)**
- **LED current modulation method: PWM and DC mode**
- **96 Channel flexible PWM generators and independent for 14 Bits PWM Brightness**
- **Synchronization with TV Frame – VSYNC / HSYNC / Digital PLL Integrated**
- **Digital Configurable DC/DC Feedback**
- **Protection For Safety Features**
  - **- LED Short Detection**
  - **- LED Open Detection**
  - **- Temperature Shutdown detection**
  - **- UVLO**
- **PWM and DC Dimming Via SPI Interface**
- **HDR mode for LED current modulation**
- **Available In QFN 12x12-120 Package**
- **One global high accurate 10 big DAC which sets the LED current**

General Description

The APE5035 are integrates Mosfet and 96 channel LED controller for LCD backlight. It's high accurate LED current 2% (20mA LED current) and wide input voltage range.

The APE5035 has 96 Channel flexible PWM generators and independent 14 bits PWM brightness were control LED current for every channel. In addition; It's has one global high accurate 10 bit DAC which sets the LED current. It's synchronization with TV Frame including VSYNC/ HSYNC and Digital PLL method.

The APE5035 own LED current modulation method including PWM mode and DC mode. When applications have flicker frequency issue and then can using the DC mode method eliminate flicker frequency problem.

The APE5035 has two pins can be digital configurable DC/ DC feedback, that's for control DC/DC architecture. As the same time; the device using programmable via SPI interface.

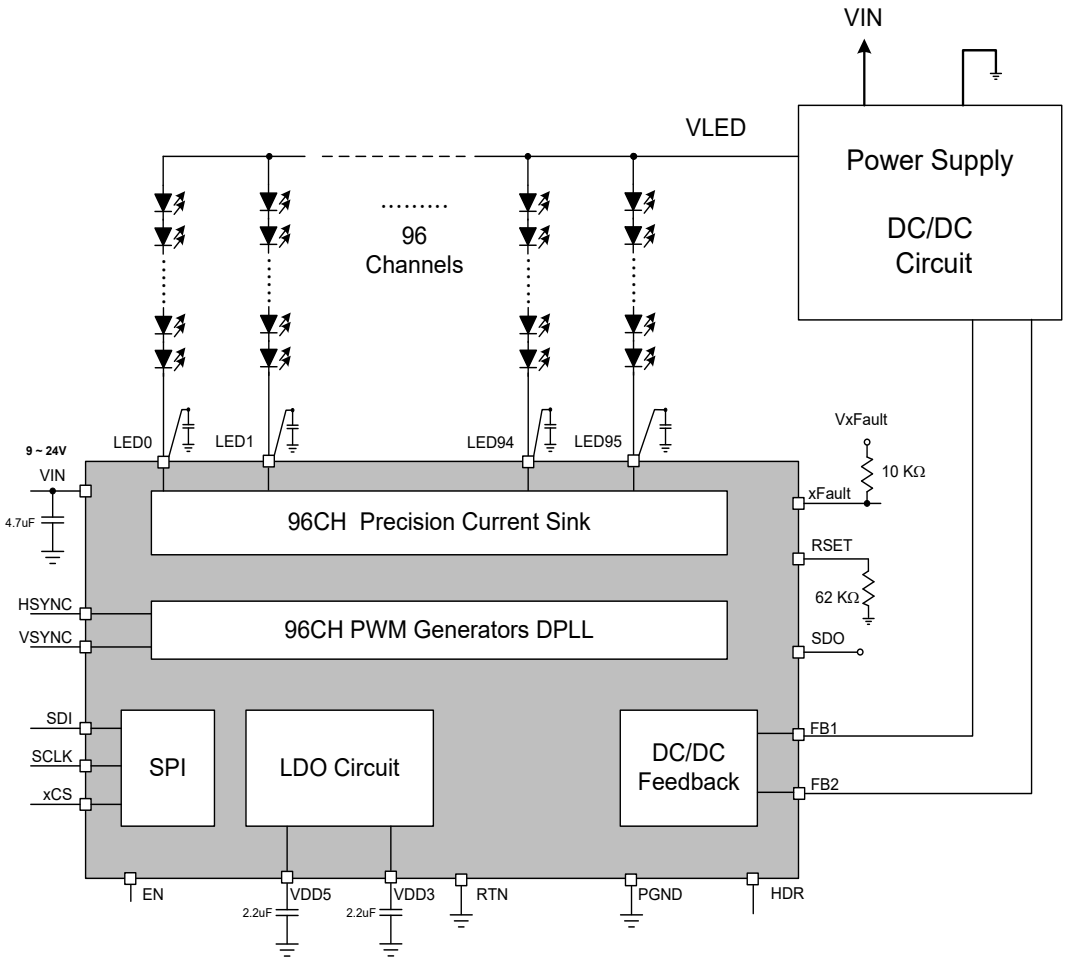
The APE5035 owns HDR mode for modulation LED current. It's build-in protection for safety; include LED short, LED Open, temperature shutdown protection and UVLO.

The APE5035 is available in QFN 12x12-120 packages.

Applications

- **Televisions**
- **Monitors**

Simplified Application Circuit

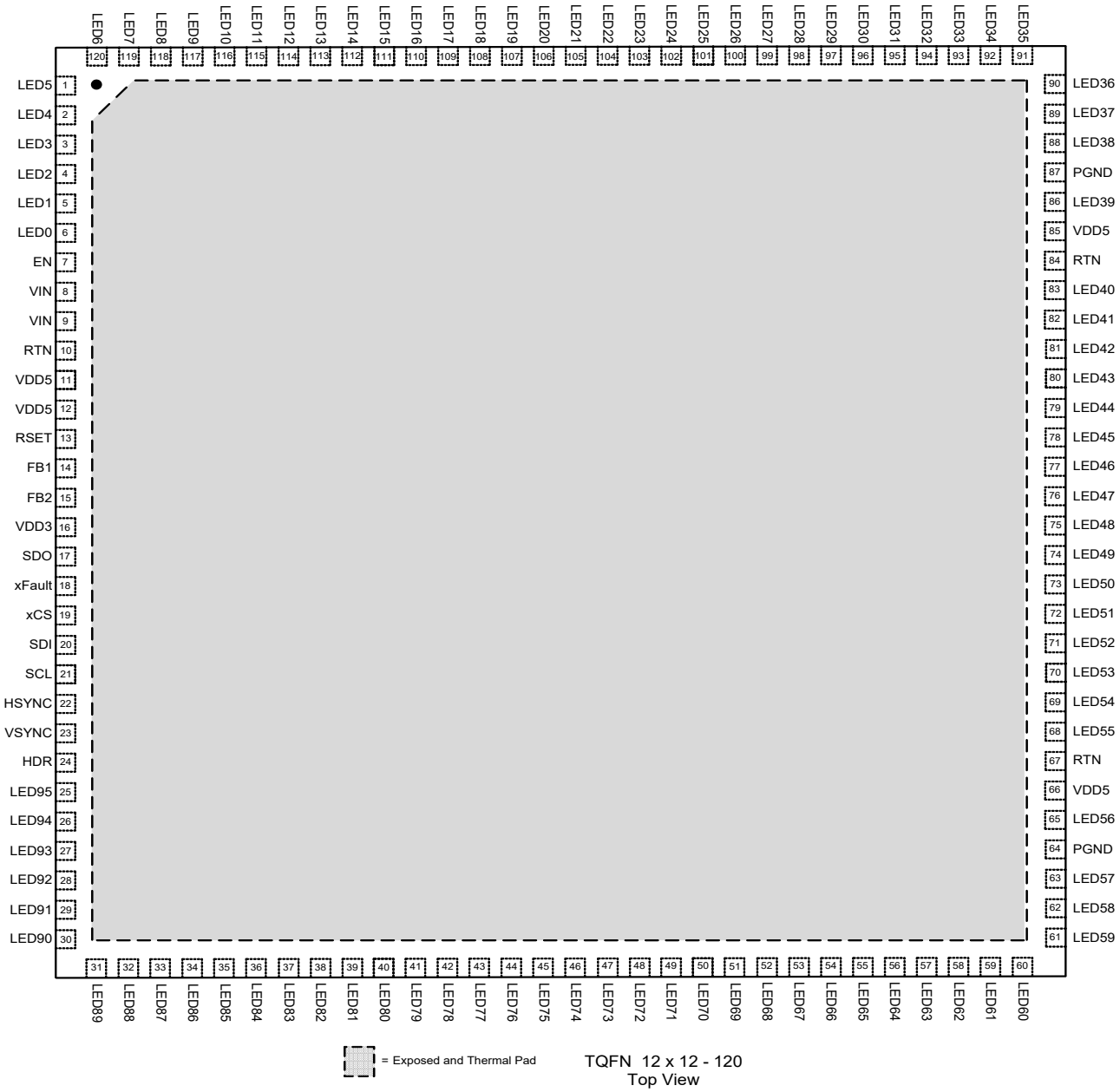


Ordering and Marking Information

APE5035 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN 12x12-120 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Green Part
APE5035 QA : APE5035 xxxxx	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configurations



TQFN 12 x 12 - 120
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to PGND)	-0.3 ~ 26	V
V_{ANALOG}	LED0 ~ LED95 to PGND EN to PGND	-0.3 ~ 18 -0.3 ~ 26	V
	VSYNC, HSYNC, FB1, FB2 and RSET to RTN	-0.3 ~ 7	V
$V_{DIGITAL}$	VDD5 and xFault to RTN SDI, SCL and xCS to RTN	-0.3 ~ 7	V
	SDO to RTN	-0.3 ~ 5	
V_{GND}	RTN to PGND	-0.3 ~ +0.3	V
T_J	Junction Temperature	180	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	25	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Input Supply Voltage	4.5 ~ 24	V
V_{LEDn}	LED String Voltage	~ 16	V
I_{LED}	LED Current	1 ~ 20 (peak 30)	mA
C_{IN}	Converter Input Capacitor (MLCC)	4.7 ~	µF
C_{VDD_5}	VDD5 Output Capacitor (MLCC)	2.2 ~	µF
C_{VDD_3}	VDD3 Output Capacitor (MLCC)	2.2 ~	µF
R_{SET}	External Setting LED Current Resistor	62 ±1%	KΩ
T_A	Ambient Temperature	-20 ~ 85	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, EN=3.3V, VSYNC=60Hz and T_A= -40 to 85°C. Typical values are at TA=25°C.

Symbol	Parameter	Test Condition	APE5035			
			Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage Range		9	-	24	V
		VIN shorted to VDD5	4.5	5	5.5	V
V_{LDO_5}	5V LDO Voltage Regulation Output	IDAC Code setting to max, V_{IN}=12V, EN=High	4.5	5	5.5	V
V_{LDO_3}	3.3V LDO Voltage Regulation Output	I_{LOAD}=20mA, V_{IN}=12V, EN=High	3	3.3	3.6	V
V_{IN-POR}	VIN Power On Reset Level	EN=High, VIN Rising	3.4	3.9	4.4	V
$V_{IN\_POR\_HYS}$	POR Hysteresis	EN=High, VIN Falling	-	0.3	-	V
	Power On Delay Time	Waiting to Command Time (V_{IN} >=4.5V and EN=high are already)	-	150	-	mS
I_Q	Quiescent Current	V_{IN}=12V, IDAC is max, duty=50%, EN=high (Normal operation)	-	-	110	mA
	Shutdown Current	EN= Low (Shutdown)	-	-	100	µA
$I_{LED\_20\_1}$	LED Current Accuracy	I_{LED}=978.024uA, REG_Code[9:0]=33, 25°C (Note: It's not include RSET)	958.46352	978.024	997.58448	µA
$I_{LED\_20\_20}$	LED Current Accuracy	I_{LED}=20.005mA, REG_Code[9:0]=675, 25°C (Note: It's not include RSET)	19.6049	20.005	20.4051	mA
$I_{LED\_20\_1}$	LED Current Accuracy to All Temperature	I_{LED}=978.024uA, REG_Code[9:0]=33, -25 ~ 85°C (Note: It's not included RSET)	-3	-	3	%
$I_{LED\_20\_20}$		I_{LED}=20.005mA, REG_Code[9:0]=675, -25 ~ 85°C (Note: It's not included RSET)	-3	-	3	%
I_{LED_CH}	Channel to channel current matching	I_{LED}=20.005mA, REG_Code[9:0]=675, 25°C (Note: It's not included RSET)	-2	-	2	%
I_{FB_MAX}	Feedback Current Maximum	V_{FB}_X > 0.25V, T_A=25°C	251	255	270	µA
FB_{IDAC_LSB}	FB_DAC_LSB		-	1	-	µA
T_{OTP}	Over-temperature	Temperature rising	150	165	180	°C
T_{OTP_HYS}	Temperature hysteresis		-	20	-	°C
T_{SHORT_MIN}	Minimum PWM on time to detect shorted LEDs		-	3	-	µS
F_{OSC}	Internal Clock	For OSC	22.413	23.59	24.772	MHz
F_{HSYNC}	HSYNC Frequency	For PWM Clock	22.413	23.59	24.772	MHz
F_{VSYNC}	VSYNC Frequency (No VRR Mode)	For DPLL	48.5	50	51.5	Hz
			58.2	60	61.8	Hz
			116.4	120	123.6	Hz
			139.68	144	148.32	Hz
			160.05	165	169.95	Hz
			232.8	240	247.2	Hz
			465.6	480	494.4	Hz
	VSYNC Frequency (VRR Mode): OSC	For internal OSC: 1Hz (resolution)	40	-	240	Hz

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V, EN=3.3V, VSYNC=60Hz and T_A= -40 to 85°C. Typical values are at TA=25°C.

Symbol	Parameter	Test Condition	APE5035			
			Min.	Typ.	Max.	Unit
F_{PWM}	LED output Frequency (No VRR mode)	23.04KHz/ 11.52KHz/ 5.76KHz/ 2.88KHz/ 1.44KHz (For Register select)	1.44	-	23.04	KHz
			20.736	23.04	25.344	KHz
V_{IH}	High Level Input Voltage	Input PIN (VSYNC, HSYNC, xCS, SCL, SDI, EN, HDR)	1.7	-	VDD5+0.3	V
V_{IL}	Low Level Input Voltage	Input PIN (VSYNC, HSYNC, xCS, SCL, SDI, EN, HDR)	-0.3	-	0.7	V
V_{OH}	High Level Output Voltage	Output PIN (SDO), I=2mA	VDD3-0.3	-	-	V
V_{OL}	Low Level Output Voltage	Output PIN (SDO), I=2mA	-	-	0.3	V
V_{OL_PD}	Low Level Output Voltage Open Drain Outputs	Output PIN (xFault), I=2mA	-	-	0.3	V
R_{PU}	Input Resistance Pull-up	V_{IN}=12V, xCS=GND	-	300	-	KΩ
R_{PD}	Input Resistance Pull-down	V_{IN}=12V, VSYNC, HSYNC, SCL, SDI, HDR and EN=5V	-	300	-	KΩ
I_{LEK}	Leakage Current	V_{IN}=12V, For xFault, FB1, FB2	-	-	1	μA
I_{LEDX_LEK}	Leakage Current for LEDx	V_{IN}=12V, V_{LEDx}=16V	-	-	1	μA
I_{SPI_CLK}	SCL Frequency		-	-	26	MHz
I_{EN}	EN input current	V_{IN}=24V, EN=24V	-	-	30	μA

Pin Description

PIN		FUNCTION
NO.	NAME	
1	LED5	LED Cathode Connection For LED String5.
2	LED4	LED Cathode Connection For LED String4.
3	LED3	LED Cathode Connection For LED String3.
4	LED2	LED Cathode Connection For LED String2.
5	LED1	LED Cathode Connection For LED String1.
6	LED0	LED Cathode Connection For LED String0.
7	EN	Enable control input. Forcing this pin above 1.7V enables the device or forcing this pin below 0.7V to shut it down. In shutdown, all function is disabled to decrease the supply current below 100uA. This pin is not floating (suggestion connector to 100K to ground).
8, 9	VIN	Input Supply Voltage.
10, 67, 84	RTN	Analog Ground.
11, 12, 66, 85	VDD5	Internal 5V LDO Regulation. Connect 2.2uF capacitor to GND.
13	RSET	External Setting Iset Current Resistor, RSET to GND connection 62K. (±0.5%)
14	FB1	DC/DC Power supply feedback output 1.
15	FB2	DC/DC Power supply feedback output 2.
16	VDD3	Internal 3.3V LDO Regulation. Connect 2.2uF capacitor to GND.
17	SDO	SPI interface data output. Tristate output.
18	xFault	Open drain fault output.
19	xCS	SPI interface chip selects.
20	SDI	SPI interface data input.
21	SCL	SPI interface clock.
22	HSYNC	Vertical sync frequency. PWM generator reset.
23	VSYNC	Clock input for PWM generators.
24	HDR	PWM signal input for adjustment LED current.
25	LED95	LED Cathode Connection For LED String95.
26	LED94	LED Cathode Connection For LED String94.
27	LED93	LED Cathode Connection For LED String93.
28	LED92	LED Cathode Connection For LED String92.
29	LED91	LED Cathode Connection For LED String91.
30	LED90	LED Cathode Connection For LED String90.
31	LED89	LED Cathode Connection For LED String89.
32	LED88	LED Cathode Connection For LED String88.
33	LED87	LED Cathode Connection For LED String87.
34	LED86	LED Cathode Connection For LED String86.
35	LED85	LED Cathode Connection For LED String85.
36	LED84	LED Cathode Connection For LED String84.
37	LED83	LED Cathode Connection For LED String83.
38	LED82	LED Cathode Connection For LED String82.
39	LED81	LED Cathode Connection For LED String81.
40	LED80	LED Cathode Connection For LED String80.

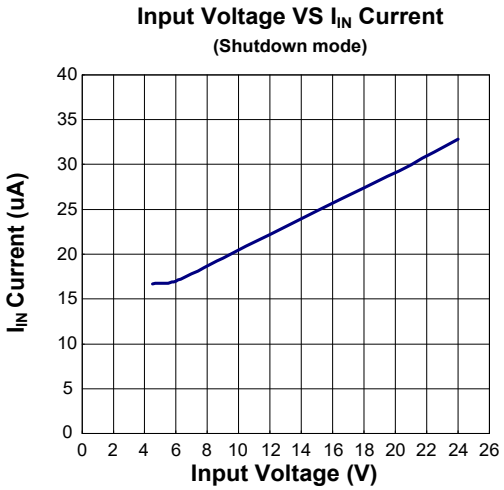
Pin Description (Cont.)

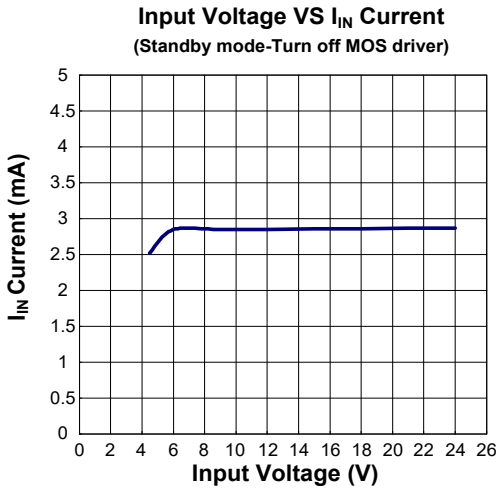
PIN		FUNCTION
NO.	NAME	
41	LED79	LED Cathode Connection For LED String79.
42	LED78	LED Cathode Connection For LED String78.
43	LED77	LED Cathode Connection For LED String77.
44	LED76	LED Cathode Connection For LED String76.
45	LED75	LED Cathode Connection For LED String75.
46	LED74	LED Cathode Connection For LED String74.
47	LED73	LED Cathode Connection For LED String73.
48	LED72	LED Cathode Connection For LED String72.
49	LED71	LED Cathode Connection For LED String71.
50	LED70	LED Cathode Connection For LED String70.
51	LED69	LED Cathode Connection For LED String69.
52	LED68	LED Cathode Connection For LED String68.
53	LED67	LED Cathode Connection For LED String67.
54	LED66	LED Cathode Connection For LED String66.
55	LED65	LED Cathode Connection For LED String65.
56	LED64	LED Cathode Connection For LED String64.
57	LED63	LED Cathode Connection For LED String63.
58	LED62	LED Cathode Connection For LED String62.
59	LED61	LED Cathode Connection For LED String61.
60	LED60	LED Cathode Connection For LED String60.
61	LED59	LED Cathode Connection For LED String59.
62	LED58	LED Cathode Connection For LED String58.
63	LED57	LED Cathode Connection For LED String57.
64, 87	PGND	Power Ground For LED Current return path.
65	LED56	LED Cathode Connection For LED String56.
68	LED55	LED Cathode Connection For LED String55.
69	LED54	LED Cathode Connection For LED String54.
70	LED53	LED Cathode Connection For LED String53.
71	LED52	LED Cathode Connection For LED String52.
72	LED51	LED Cathode Connection For LED String51.
73	LED50	LED Cathode Connection For LED String50.
74	LED49	LED Cathode Connection For LED String49.
75	LED48	LED Cathode Connection For LED String48.
76	LED47	LED Cathode Connection For LED String47.
77	LED46	LED Cathode Connection For LED String46.
78	LED45	LED Cathode Connection For LED String45.
79	LED44	LED Cathode Connection For LED String44.
80	LED43	LED Cathode Connection For LED String43.

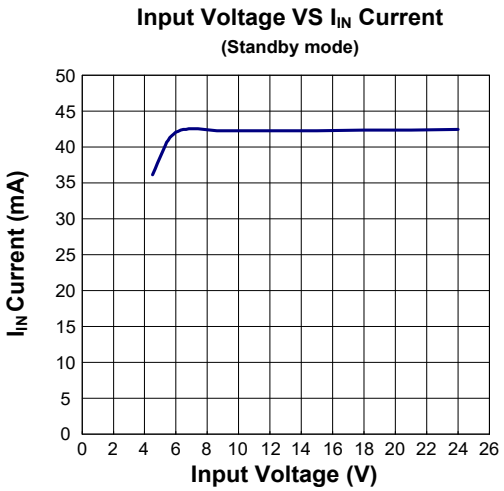
Pin Description (Cont.)

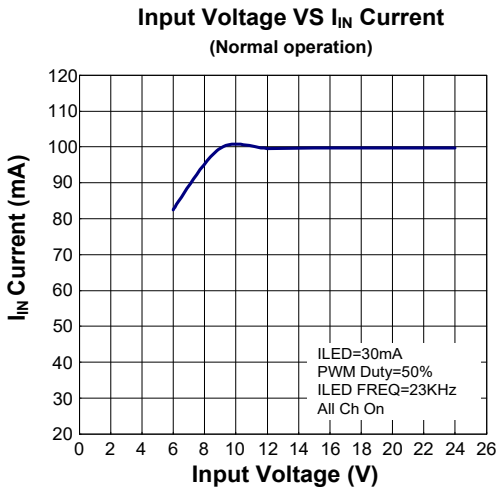
PIN		FUNCTION
NO.	NAME	
81	LED42	LED Cathode Connection For LED String42.
82	LED41	LED Cathode Connection For LED String41.
83	LED40	LED Cathode Connection For LED String40.
86	LED39	LED Cathode Connection For LED String39.
88	LED38	LED Cathode Connection For LED String38.
89	LED37	LED Cathode Connection For LED String37.
90	LED36	LED Cathode Connection For LED String36.
91	LED35	LED Cathode Connection For LED String35.
92	LED34	LED Cathode Connection For LED String34.
93	LED33	LED Cathode Connection For LED String33.
94	LED32	LED Cathode Connection For LED String32.
95	LED31	LED Cathode Connection For LED String31.
96	LED30	LED Cathode Connection For LED String30.
97	LED29	LED Cathode Connection For LED String29.
98	LED28	LED Cathode Connection For LED String28.
99	LED27	LED Cathode Connection For LED String27.
100	LED26	LED Cathode Connection For LED String26.
101	LED25	LED Cathode Connection For LED String25.
102	LED24	LED Cathode Connection For LED String24.
103	LED23	LED Cathode Connection For LED String23.
104	LED22	LED Cathode Connection For LED String22.
105	LED21	LED Cathode Connection For LED String21.
106	LED20	LED Cathode Connection For LED String20.
107	LED19	LED Cathode Connection For LED String19.
108	LED18	LED Cathode Connection For LED String18.
109	LED17	LED Cathode Connection For LED String17.
110	LED16	LED Cathode Connection For LED String16.
111	LED15	LED Cathode Connection For LED String15.
112	LED14	LED Cathode Connection For LED String14.
113	LED13	LED Cathode Connection For LED String13.
114	LED12	LED Cathode Connection For LED String12.
115	LED11	LED Cathode Connection For LED String11.
116	LED10	LED Cathode Connection For LED String10.
117	LED9	LED Cathode Connection For LED String9.
118	LED8	LED Cathode Connection For LED String8.
119	LED7	LED Cathode Connection For LED String7.
120	LED6	LED Cathode Connection For LED String6.
-	Exposed	Power Ground For LED Current Return Path.

Typical Operating Characteristics



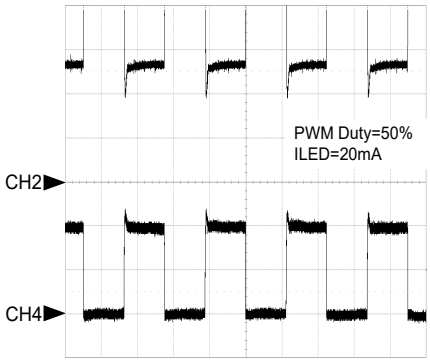






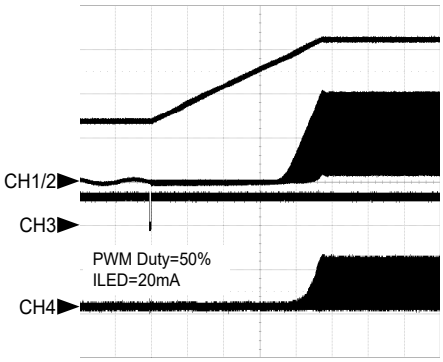
Operating Waveforms

Normal Operation



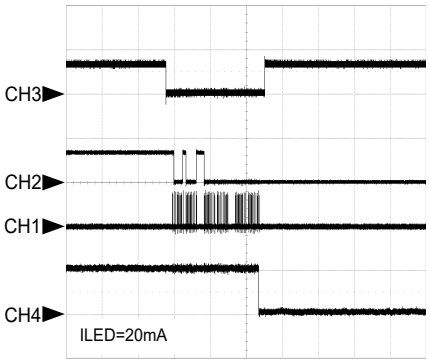
CH1: -
CH2: LEDx V_{Drain}-200mV/div
CH3: -
CH4: I_{LEDx}-10mA/div
Time: 20us/div

Start up - Current on enable



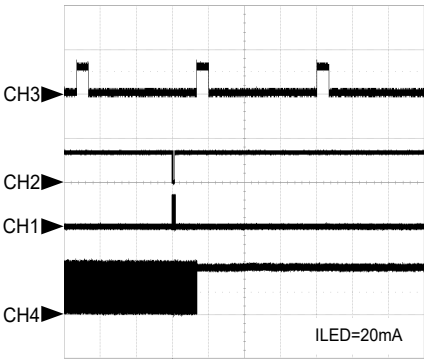
CH1: V_{OUT}-10V/div
CH2: V_{drain}-2V/div
CH3: V_{xCS}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 10ms/div

Update Mode (xCS)
PWM duty 100% to 0%



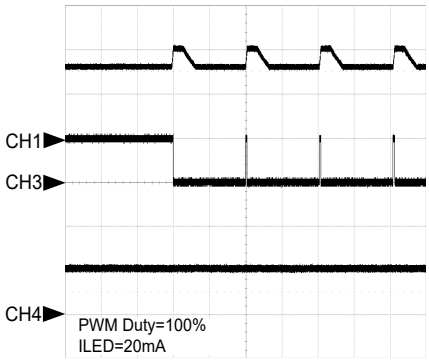
CH1: V_{SCL}-5V/div
CH2: V_{SDI}-5V/div
CH3: V_{xCS}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 200us/div

Update Mode (Vsync)
PWM duty 50% to 100%



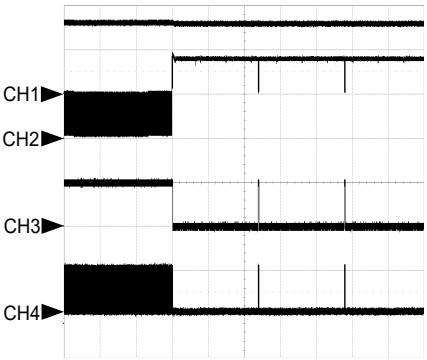
CH1: V_{SCL}-5V/div
CH2: V_{SDI}-5V/div
CH3: V_{SYNC}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 5ms/div

Open LED - Retrial



CH1: V_{OUT}-20V/div
CH2: -
CH3: V_{xFAULT}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 500ms/div

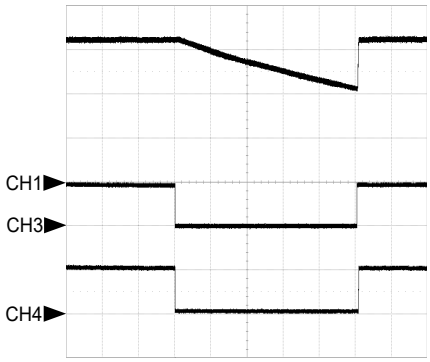
Short LED - Retrial



CH1: V_{OUT}-20V/div
CH2: $V_{LED\ Drain}$-5V/div
CH3: V_{xFAULT}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 200ms/div

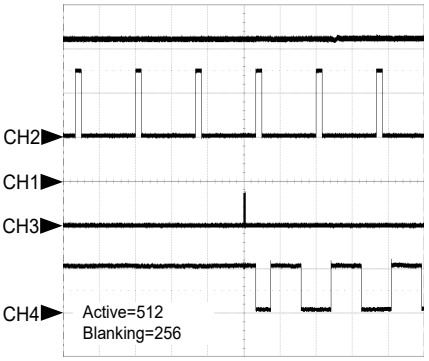
Operating Waveforms (Cont.)

OTW



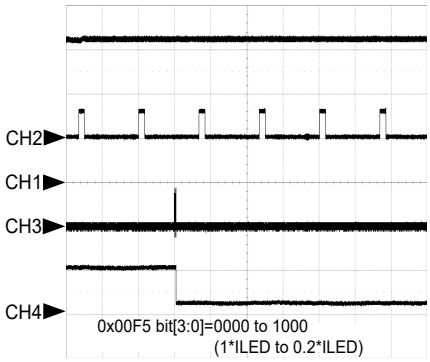
CH1: V_{OUT}-10V/div
CH2: -
CH3: V_{xFAULT}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 1s/div

MPRT
Disable to enable



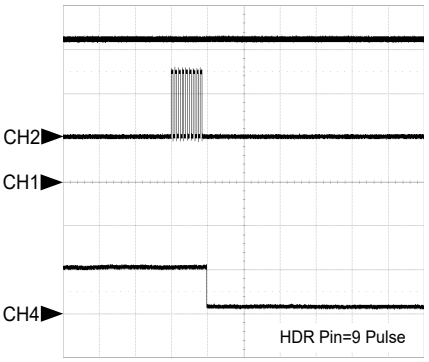
CH1: V_{OUT}-10V/div
CH2: V_{VSYNC}-2V/div
CH3: V_{SDI}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 10ms/div

HDR (Software Control)



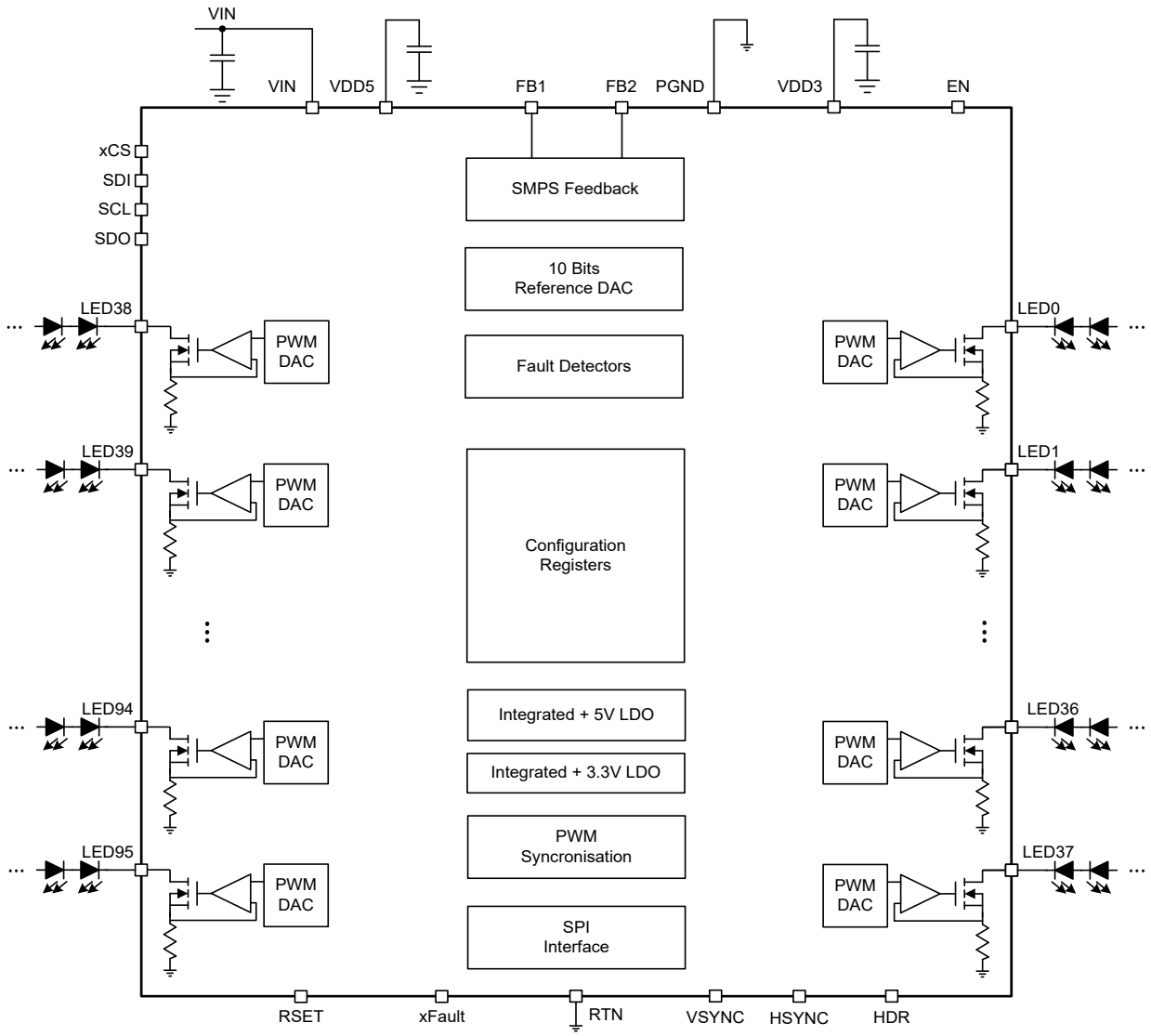
CH1: V_{OUT}-10V/div
CH2: V_{VSYNC}-5V/div
CH3: V_{SCL}-5V/div
CH4: I_{LEDx}-20mA/div
Time: 10ms/div

HDR (Hardware Control)

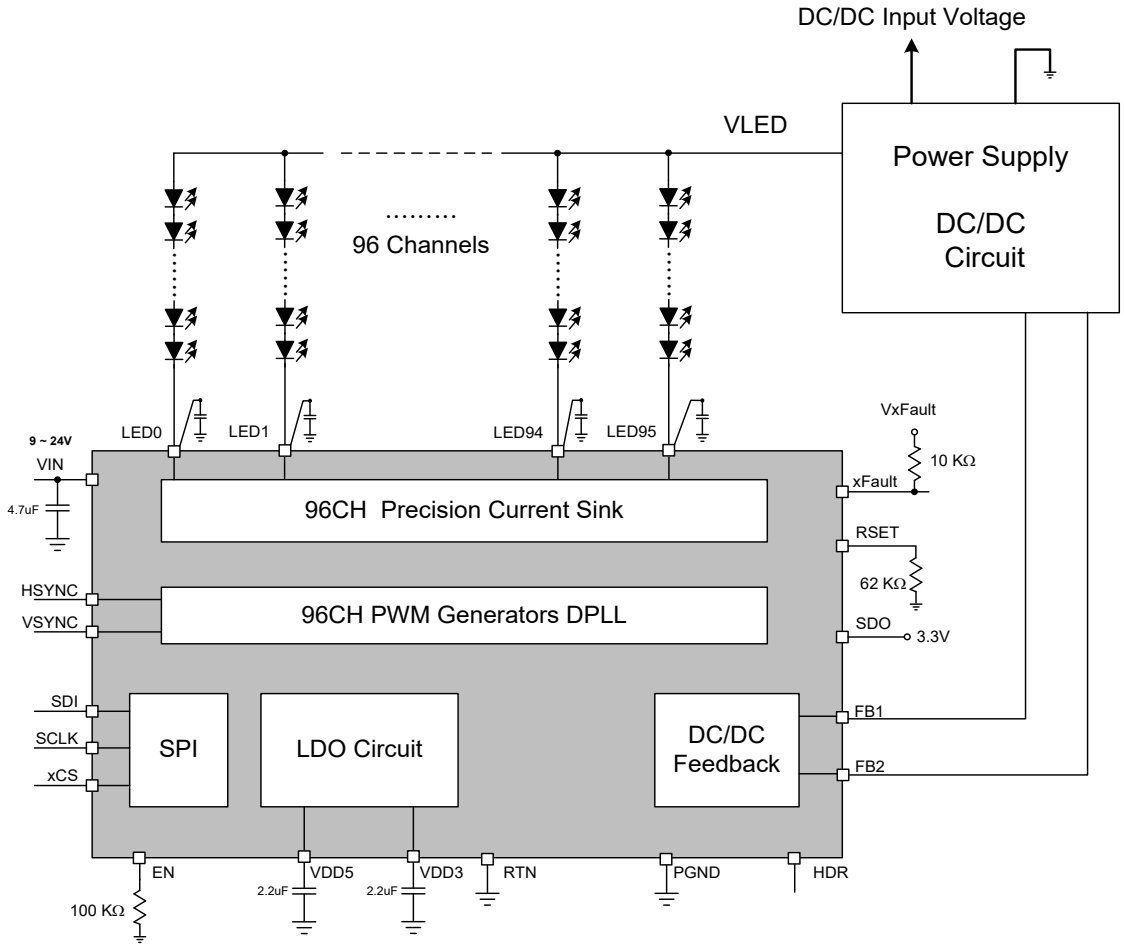


CH1: V_{OUT}-10V/div
CH2: V_{HDR}-2V/div
CH3: -
CH4: I_{LEDx}-20mA/div
Time: 2ms/div

Block Diagram



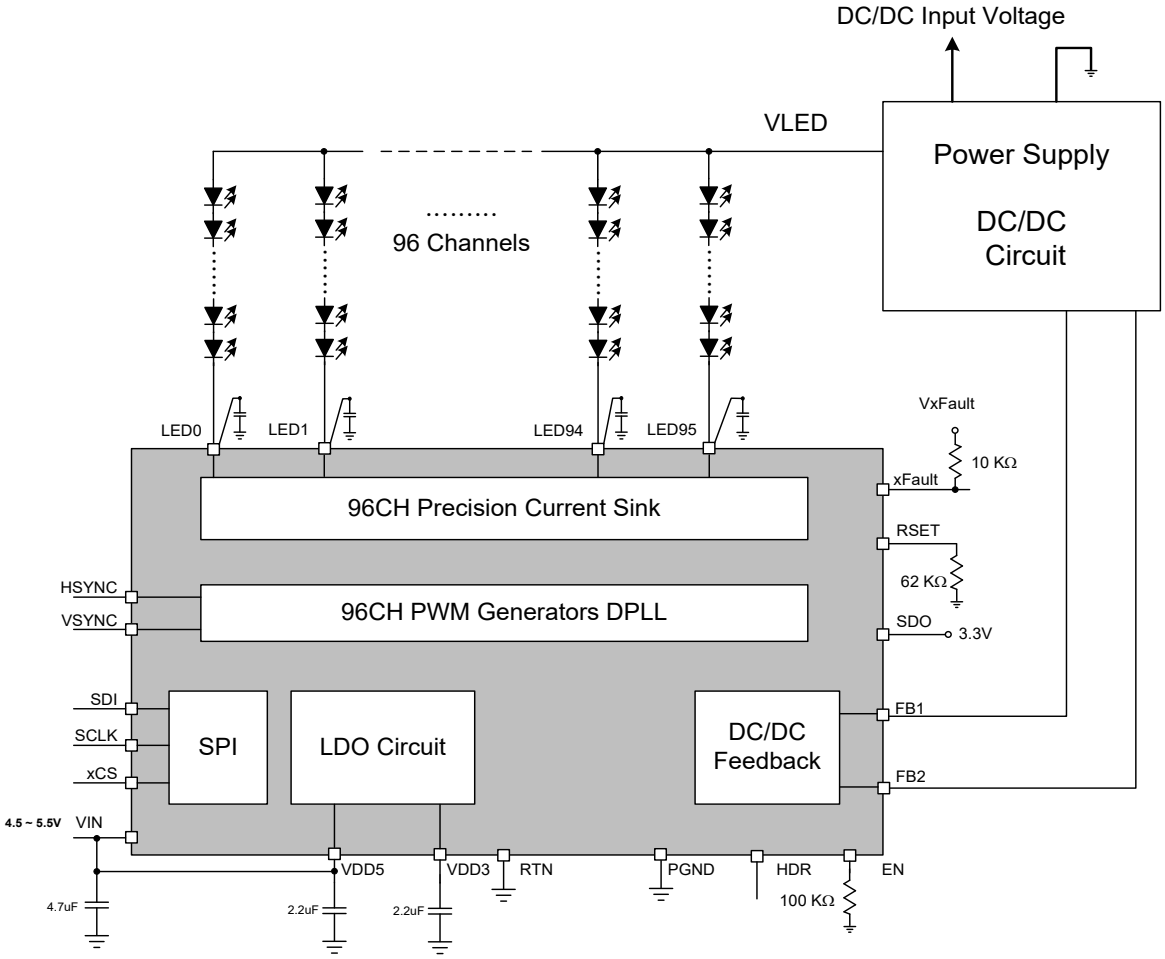
Typical Application Circuit 1:



Note 4: When LED0 to 95 of APE5035 pin-out location to External LED string cathode location has exceed 1uH wire inductance, suggestion add the MLCC capacitors for holdout interference.

Typical Application Circuit 2:

For VIN shorted to VDD5 application.



Note 5: When LED0 to 95 of APE5035 pin-out location to External LED string cathode location has exceed 1uH wire inductance, suggestion add the MLCC capacitors for holdout interference.

Function Description

Power Sequence and UVLO

The APE5035 are integrates Mosfet and 96 channel LED controller for LCD backlight. Its high accurate LED current 2% (20mA LED current) and wide input voltage range.

The APE5035 Using power sequence as below figure 1 and 2:

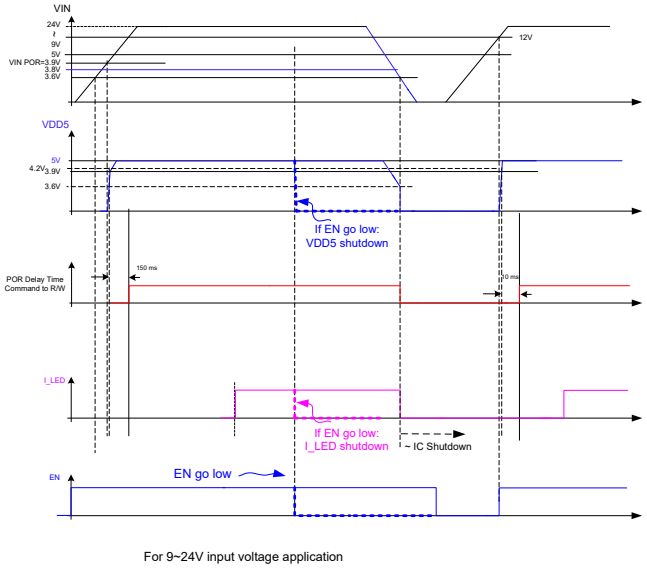


Figure 1: Power Sequence

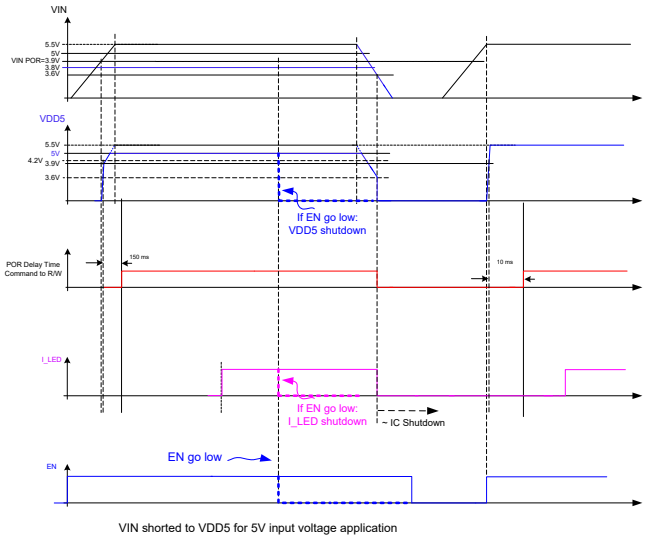


Figure 2: Power Sequence

When VIN supply power voltage exceeds input POR level (the EN pin must to be high level), the APE5035 will be standby mode status. At this time, the SPI commend can be reading / writing after must waiting 150ms.
If the VIN supply power voltage was continuous falling down to UVLO=3.6V (falling) then the APE5035 is shutdown mode (or EN pin was pull to low level).

LED Short Detection

The APE5035 has LED short detection function, when LED string happen short conditions then APE5035 can detection the abnormal condition. The register address 0x00D6 bits[12:10] are setting LED string short condition, it's from 3V adjustment to 12V for different LED string application.

Table 1: Short LED Function Register

Address	Bit	Name	Description
0x00D6h	[12:10]	Short_level[2:0]	Note 6

Note 6:
Short detection voltage based on drain.
Bits[12:10]=000 … 3V.
Bits[12:10]=001 … 4V.
…
Bits[12:10]=110 … 9V.
Bits[12:10]=111 … 12V.

Table 2: Short LED Function Register

Address	Bit	Name	Description
0x00D6h	[13]	LED_short_en	Note 7

Note 7:
Bit[13]=0 … Short LED detection disabled.
Bit[13]=1 … Short LED detection enable.

APE5035 LED short detection function is wanted to enable must using register address 0x00D6 bit[13]=1 then LED short detection will be enabled. On the contrary; the LED short function will be disabling.

Table 3: Short LED Function Register

Address	Bit	Name	Description
0x00D6h	[15]	Short_Retrial	Note 8
0x00D6h	[14]	Short_auto_off	Note 9

Note 8:
Bit[15]=0 … short retrial function disable.
Bit[15]=1 … short retrial function enable.

Note 9:
Bit[14]=0 … short auto-off function disable.
Bit[14]=1 … short auto-off function enable.

APE5035 short LED function has retrial and auto-off behavior. If APE5035 want to enable auto-off function then register address 0x00D6 bit[13] must is 1 and register address 0x00D6 bit[15]=1, at this time; the LED0 to LED95 voltage was exceed setting short_level [2:0] then LED channels will be turn off. On the contrary; the LED channels was normal operation.

Function Description (Cont.)

If short LED function behavior is retrial function then register address 0x00D6 bit[13], 0x00D6 bit[14] and 0x00D6 bit[15] are setting 1, when LED0 to LED95 voltage was exceed short_level [2:0] then LED channels will be on-off phenomenon, on the contrary; the LED channels were normal operation.

Table 4: Retrial Time Setting Register

Address	Bit	Name	Description
0x00FCh	[10:0]	Retrial_Time	Note 10

Note 10:
The address 0x00FC bits[10:0] are setting LED open and short LED retrial time, the resolution is per 1ms/LSB.
0x00FC Bits[10:0]=00000000000 … no retrial time.
0x00FC Bits[10:0]=00000000001 … 1ms.
0x00FC Bits[10:0]=00000000010 … 2ms.
…
0x00FC Bits[10:0]=011111001110 … 1998ms.
0x00FC Bits[10:0]=011111001111 … 1999ms.

When short LED function was happened and short LED is retrial behavior, the retrial time can be setting and fault times also can be setting by register, see the table 4 and 5.

Table 5: Short LED Function Register

Address	Bit	Name	Description
0x00D6h	[9:8]	Short_debouncer	00: 1 fault 01: 6 faults 10: 11 faults 11: 15 faults

Suggestion the APE5035 using the LED short detection must the address register current_on can to 1 after the address 0x00D6 bits[15:13] is setting finished first. If the registers were setting; the registers value should not be adjusted.

LED Open Detection

The APE5035 has LED open detection function, when LED string or any LED happen open condition then the APE5035 can detection that abnormal operation.

Table 6: LED Open Function Register

Address	Bit	Name	Description
0x00D6h	[6]	LED_Open_EN	Note 11

Note 11:
Bit[6]=0 … LED Open detection disabled.
Bit[6]=1 … LED Open detection enable.

APE5035 LED open detection function is wanted to enable must use register address 0x00D6 bit[6]=1 then LED open detection will be enabled. On the contrary; the LED short function will be disabling.

Table 7: LED Open Function Register

Address	Bit	Name	Description
0x00D6h	[7]	Retrial_Open	Note 12
0x00D6h	[5]	Auto_Off_Open	Note 13

Note 12:
Bit[7]=0 … retrial open function disable.
Bit[7]=1 … retrial open function enable.

Note 13:
Bit[5]=0 … auto-off open function disable.
Bit[5]=1 … auto-off open function enable.

APE5035 LED open detection function has retrial open and auto-off open behavior. If APE5035 want to enable auto-off open function then register address 0x00D6 bit [6] must is 1 and register address 0x00D6 bit[5]=1, at this time; the LEDx voltage was lower than then internal threshold then LEDx channels will be turn off and latch. Even if the LED open failure was eliminating then LEDx channels are not work properly. The auto-off open function sees the figure 3-1 as below.

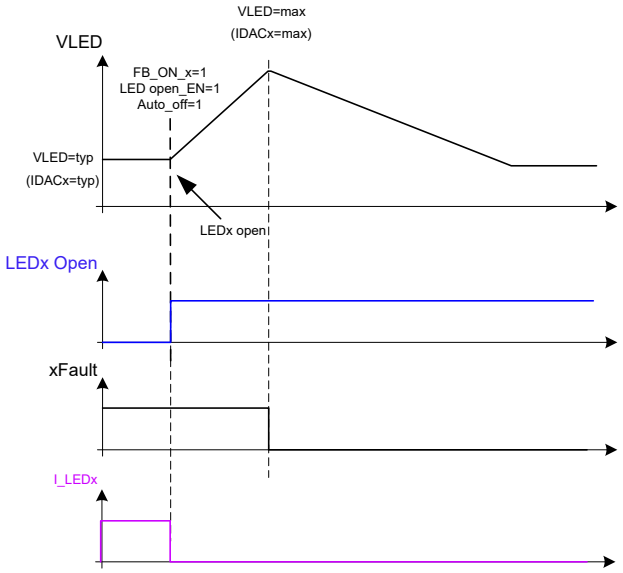


Figure 3-1: LED open - auto off

Function Description (Cont.)

If the LED open function is wanted to retrial behavior, the register address 0x00D6 bit[6] and 0x00D6 bit[7] setting to 1. When any LEDx channels are open then IDACx will be increase to max value until to LED open is still existence. The detail LED open retrial behavior sees the figure 3-2 as below:

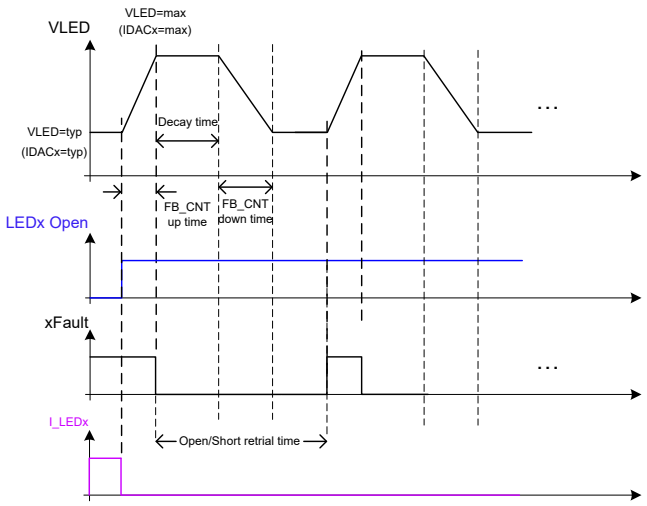


Figure 3-2: LED open - retrial

OTW and OTP

The APE5035 has OTW and OTP protection function, when APE5035 happen any abnormal operation causes to over temperature until to reach OTP then the xfault pin will be turn low.

Table 8: Auto-off OTP Register

Address	Bit	Name	Description
0x00D6h	[3]	Auto_off_OTP	Note 14

Note 14:
Bit[3]=0 … temperature shutdown disabled.
Bit[3]=1 … temperature shutdown enable.

The table 8 is setting auto-off OTP, when this bit is setting to 1 then LED current will be turn off when happen OTP condition. On the contrary; the OTP function will be disabling. By the way; when the auto-off OTW and OTW selection was setting then auto-off OTP was not setting to 1 still can be turn off LED current.
Secondly; the address 0x00DB bit[4] is detection the OTP fault register. If this bit was written to 1 then OTP happen, On the contrary; the OTP condition is not happened. The same detection function address 0x00DB bit[6] is detection OTW function; the function is the same OTP. The address 0x00DB bit[6] must cooperate address 0x00D6 bits[1:0] was setting to 00 to 10 then this bit can be response.

Table 9: OTW Selection Function Register

Address	Bit	Name	Description
0x00D6h	[1:0]	OTW Selection	Note 15

Note 15:
Bits[1:0]=00 … 110°C.
Bits[1:0]=01 … 120°C.
Bits[1:0]=10 … 140°C.
Bits[1:0]=11 … Disable.

The table 9 is setting OTW selection register; it does can be setting different OTW point and OTW function disable.

Table 10: Auto-off OTW Register

Address	Bit	Name	Description
0x00D6h	[4]	Auto_off_OTW	Note 16

Note 16:
Bit[4]=0 … Warning temperature (OTW) shutdown disabled.
Bit[4]=1 … Warning temperature (OTW) shutdown enabled.

The table 10 is setting auto_off OTW function, when this bit is setting to 1 then the temperature is reaction to OTW point, the LED current will be turn off, on the contrary; then LED current is not turn off.
To sum it up the OTW and OTP function; the as below table 11 has OTW and OTP true table can see overall behavior.

Table 11: OTW and OTP True Table

Temperature	OTW SEL	OTW	OTP	OTW Fault register	OTP Fault register	LED Current	xFault PIN
Temp >110°C	0	0	0	x	x	x	High
Temp >160°C	0	0	0	x	fault	x	Low
Temp >110°C	0	0	1	x	x	x	High
Temp >160°C	0	0	1	x	fault	shutdown	Low
Temp >110°C	0	1	0	x	x	x	High
Temp >160°C	0	1	0	x	fault	x	Low
Temp >110°C	0	1	1	x	x	x	High
Temp >160°C	0	1	1	x	fault	shutdown	Low
Temp >110°C	1	0	0	fault	x	x	Low
Temp >160°C	1	0	0	fault	fault	x	Low
Temp >110°C	1	0	1	fault	x	x	Low
Temp >160°C	1	0	1	fault	fault	shutdown	Low
Temp >110°C	1	1	0	fault	x	shutdown	Low
Temp >160°C	1	1	0	fault	fault	shutdown	Low
Temp >110°C	1	1	1	fault	x	shutdown	Low
Temp >160°C	1	1	1	fault	fault	shutdown	Low

Function Description (Cont.)

Dither PWM mode and Normal PWM mode

The Dither PWM mode is shown in the figure below.
When the code will increase, the output current conduction time will also increase at the same time. The method of increase is the red waveform in the figure. It is cycled every 16 times. For example; the PWM output current frequency was around 23KHz, when the output current conduction time was increase 1 code value then conduction time was increase around 43 ns. If the code increases, the red waveform will have more values until it reaches the maximum value.
The conduction time can adjustment 0x0000 register (local mode) of CH0 or 0x00C0 register (global mode).
See the register table.
the register 0x0000 bits[13:0] is setting dither PWM duty.
It's adjustment range is from 0% to 100% and every ~0.0061%/LSB.

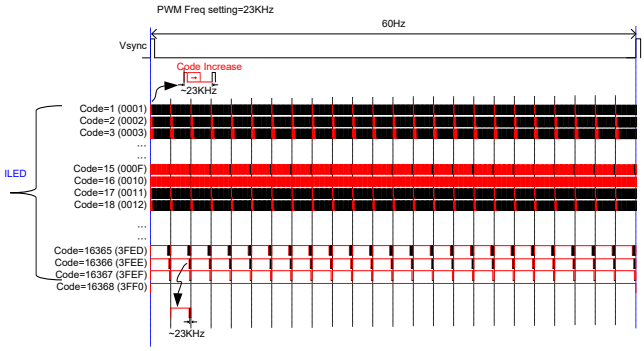


Figure 4: LED current of Dither PWM mode

The Normal PWM mode was shown in the figure 5 below.
The code is increasing, the output current conduction time will also increase at the same time. The increasing method is every PWM pulse conduction time was increased.
the register 0x0000 bits[9:0] is setting normal PWM duty.
It's adjustment range is from 0% to 100% and every ~0.097656%/LSB.

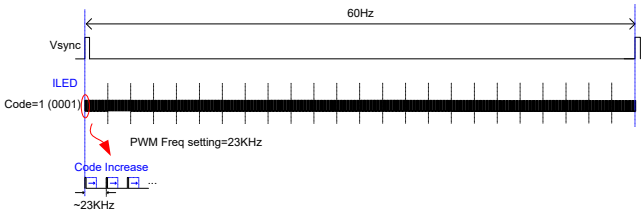


Figure 5: LED current of Normal PWM mode

Because the output frequency around 23KHz of LED current to limit minimum on application wherefore the PWM duty suggest setting to more than 7% (on time more than 3us). For the application using have better in minimum on.

LEDx channels on/off

The APE5035 has 96 LED channels that can be individually control on/off, see then table 12.

Table 12: LEDx channels on/off Register

Address	Bit	Name	Description
0x00C2h	[15:0]	Curr_15 – Curr_0	Note 17
0x00C3h	[15:0]	Curr_31 – Curr_16	Note 18
0x00C4h	[15:0]	Curr_47 – Curr_32	Note 19
0x00C5h	[15:0]	Curr_63 – Curr_48	Note 20
0x00C6h	[15:0]	Curr_79 – Curr_64	Note 21
0x00C7h	[15:0]	Curr_95 – Curr_80	Note 22

Note 17:
Bits[15:0]=0000000000000000 … LED15 to LED0 turn off.
Bits[15:0]=0000000000000001 … LED0 turn on.
Bits[15:0]=0000000000000010 … LED1 turn on.
…
Bits[15:0]=0100000000000000 … LED14 turn on.
Bits[15:0]=1000000000000000 … LED15 turn on.
Every bit is control individually LED channel on/off.

Note 18:
Bits[15:0]=0000000000000000 … LED31 to LED16 turn off.
Bits[15:0]=0000000000000001 … LED16 turn on.
Bits[15:0]=0000000000000010 … LED17 turn on.
…
Bits[15:0]=0100000000000000 … LED30 turn on.
Bits[15:0]=1000000000000000 … LED31 turn on.
Every bit is control individually LED channel on/off.

Note 19:
Bits[15:0]=0000000000000000 … LED47 to LED32 turn off.
Bits[15:0]=0000000000000001 … LED32 turn on.
Bits[15:0]=0000000000000010 … LED33 turn on.
…
Bits[15:0]=0100000000000000 … LED46 turn on.
Bits[15:0]=1000000000000000 … LED47 turn on.
Every bit is control individually LED channel on/off.

Note 20:
Bits[15:0]=0000000000000000 … LED63 to LED48 turn off.
Bits[15:0]=0000000000000001 … LED48 turn on.
Bits[15:0]=0000000000000010 … LED49 turn on.
…
Bits[15:0]=0100000000000000 … LED62 turn on.
Bits[15:0]=1000000000000000 … LED63 turn on.
Every bit is control individually LED channel on/off.

Function Description (Cont.)

Note 21:
Bits[15:0]=0000000000000000 … LED79 to LED64 turn off.
Bits[15:0]=0000000000000001 … LED64 turn on.
Bits[15:0]=0000000000000010 … LED65 turn on.
…
Bits[15:0]=0100000000000000 … LED78 turn on.
Bits[15:0]=1000000000000000 … LED79 turn on.
Every bit is control individually LED channel on/off.

Note 22:
Bits[15:0]=0000000000000000 … LED95 to LED80 turn off.
Bits[15:0]=0000000000000001 … LED80 turn on.
Bits[15:0]=0000000000000010 … LED81 turn on.
…
Bits[15:0]=0100000000000000 … LED94 turn on.
Bits[15:0]=1000000000000000 … LED95 turn on.
Every bit is control individually LED channel on/off.

IDAC Adjustment

The APE5035 include 10 bits IDAC code, it's provided user can be adjustment LED current. Every bit corresponds IDAC code adjustment LED current as below table 13:

Table 13: IDAC Correspondence Table

Bit (dec)	LED current (mA)	Note
1	~ 0.0296371	-
2	~ 0.0592742	-
338	~ 10.017338	default
704	~ 20.864516	-
1022	~ 30.28911	-
1023	~ 30.31875	-

In addition; the address 0x0060 to 0x00BF are CH0 to CH95 adjustment IDAC registers for LED current control. 0x00C0 is setting LED current for global control all channels. See the table14.

Table 14: IDAC Register

Address	Bit	Name	Description
0x0060h	[9:0]	IDAC_CH0	-
0x0061h	[9:0]	IDAC_CH1	-
….. ….. …..			
0x00BEh	[9:0]	IDAC_CH94	-
0x00BFh	[9:0]	IDAC_CH95	-
0x00C1h	[9:0]	GDAC	For all channels

This is a simple calculation formula for IDAC (mA).

PWM mode current:
ILED (mA) = ~0.0296371mA*IDAC_Code (1~1023)

As above formula calculate by RSET 62KOhm.

PWM Delay and PWM Brightness

The address 0x0100 to 0x015F is setting PWM delay time. It's has 10 bits resolution can adjustment LED0 to LED95. The register sees the register map. The PWM delay time can adjustment range is from 0 to 1023 code base-on LED current frequency reciprocals.
The address 0x0000 to 0x005F is setting PWM brightness. It's has 14 bits resolution can adjustment LED0 to LED95. the resolution is approximate 0.0061%/LSB for dither mode. On the contrary; it's the normal mode then 10 bits resolution can adjustment.

Decay Time

In order to auto adjustment optima output voltage by external circuit, it need to detect time and function. The table 15 is setting detection enable/disable. The detect time can be adjustment range from 16ms change to 128ms.
Suggestion the registers were setting; the registers value should not be adjusted.

Table 15: FB decay enable/disable Register

Address	Bit	Name	Description
0x00D5h	[1]	Fb2_decay_off	Note 23
0x00D5h	[0]	Fb1_decay_off	Note 24

Note 23:
Bit[1]=0 … FB counter2 decay time is enable and defined by register decay_time.
Bit[1]=1 … FB counter2 decay time is disable.

Note 24:
Bit[0]=0 … FB counter1 decay time is enable and defined by register decay_time.
Bit[0]=1 … FB counter1 decay time is disable.

Table 16: FB decay enable/disable Register

Address	Bit	Name	Description
0x00D5h	[3:2]	Fbcount_decay_time[1:0]	Note 25

Note 25:
Bits[3:2]=00 … 16ms.
Bits[3:2]=01 … 32ms.
Bits[3:2]=10 … 64ms.
Bits[3:2]=11 … 128ms.

Function Description (Cont.)

HDR Control

The APE5035 has HDR mode function, it mainly control LED current by software or hardware mechanism.
When address 0x00F5 bit[15] is setting software or hardware control.

Table 17: HDR Control Register

Address	Bit	Name	Description
0x00F5h	[15]	HDR_HW_EN	Note 26

Note 26:
Bit[15]=0 … Hardware control.
Bit[15]=1 … Software control. (base-on 0x00F5 bits[3:0])

When HDR control is setting to software control then LED current value by register 0x00F5 bits[3:0].

Table 18: HDR Current Level Register

Address	Bit	Name	Description
0x00F5h	[3:0]	HDR_Level	Note 27

Note 27:
Bits[3:0]=0000 … 1xIDAC.
Bits[3:0]=0001 … 0.9xIDAC.
…
Bits[3:0]=1001 … 0.1xIDAC.
Bits[3:0]=1010 … 1xIDAC.
Bits[3:0]=1011 … 0xIDAC.
…
Bits[3:0]=1111 … 0xIDAC.

The register 0x00F5 bit[15] is setting to 0 then ILED value by hardware control of HDR pin. Register 0x00F5 bits [14:8] and 0x00F5 bits[7:4] is setting hardware control by application condition.

Table 19: HDR Timeout Register

Address	Bit	Name	Description
0x00F5h	[14:8]	HDR_Tout	Note 28

Note 28:
Bits[14:8]=0000001 … 8us.
Bits[14:8]=0000010 … 16us.
…
Bits[14:8]=0011010 … 208us.

The tout setting resolution is 8us/LSB.

The register 0x00F5 bits[7:4] is setting hardware pin high level time.

Table 20: HDR Timeout Register

Address	Bit	Name	Description
0x00F5h	[7:4]	HDR_DB	Note 29

Note 29:
Bits[7:4]=0001 … HDR High time >8us.
Bits[7:4]=0010 … HDR High time >16us.
…
Bits[7:4]=1111 … 248us.

The HDR pin is setting hardware control ILED current, this pin can input 5KHz to 20KHz pulse range and cooperation register 0x00F5 bits[14:8] and bits[7:4] until to optima control application condition.

ILED Output Mode

The APE5035 has selection ILED output mode by register 0x00D4 bit[6], it's control ILED current output type.

Table 21: ILED Output Control Register

Address	Bit	Name	Description
0x00D4h	[6]	DC_mode	Note 30

Note 30:
Bit[6]=0 … channels output current – PWM mode.
Bit[6]=1 … channels output current – DC mode.

Global Mode Control

The APE5035 has global/local mode, the register 0x00D5 bits[11:4], 0x00C1 bits[9:0] and 0x00C0 bits[13:0] are control global mode behavior.

Function Description (Cont.)

Table 22: Global Mode Control

Address	Bit	Name	Description
0x00D5h	[11]	gfb_on	Note 31
0x00D5h	[10]	gfb_on_ctrl_en	Note 32
0x00D5h	[9]	gfb_sel	Note 33
0x00D5h	[8]	gfb_sel_ctrl_en	Note 34
0x00D5h	[7]	gcuron	Note 35
0x00D5h	[6]	gcuron_ctrl_en	Note 36
0x00D5h	[5]	gdac_ctrl_en	Note 37
0x00D5h	[4]	gbri_ctrl_en	Note 38

Note 31:
All channel (0-95) FB_ON (Enables feedback) control:
Bit[11]=0 … feedback function of all channel disabled.
Bit[11]=1 … feedback function of all channel enabled.

Note 32:
All channel (0-95) FB_ON (Enables feedback) control by "gfb_on (REG: 0x00D5[11])" or every channel FB_ON (Enables feedback) control by specific brightness "FB_ONx (REG 0x00CE - 0x00D3)"
Bit[10]=0 …FB_ON control by FB_ONx.
Bit[10]=1 … FB_ON control by gfb_on.

Note 33:
All channel select FB for current outputs:
Bit[9]=0 … select FB pin FB1.
Bit[9]=1 … select FB pin FB2.

Note 34:
All channel (0-95) FB_SEL (select FB) control by "gfb_sel (REG: 0x00D5[9])" or every channel brightness control by specific brightness "FB_SELx (REG 0x00C8 - 0x00CD)"
Bit[8]=0 … FB_SEL control by FB_SELx.
Bit[8]=1 … FB_SEL control by gfb_sel.

Note 35:
All Channel current output driver control:
Bit[7]=0 … output driver disabled.
Bit[7]=1 … output driver enabled.

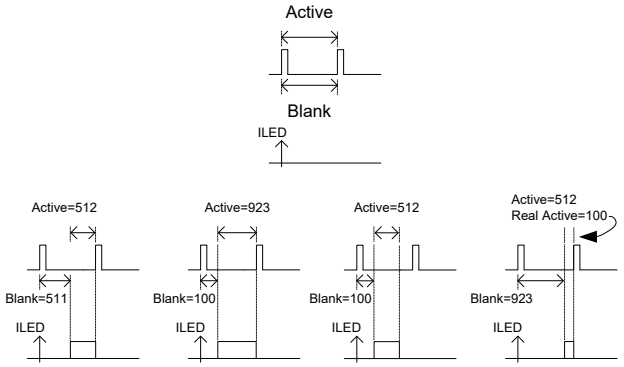
Note 36:
All channel (0-95) CUR_ON control by "gcuron (REG: 0x00D5[7])" or every channel brightness control by specific brightness "CUR_ONx (REG 0x00C2 - 0x00C7)"
Bit[6]=0 … CUR_ON control by CUR_ONx.
Bit[6]=1 … CUR_ON control by gcuron.

Note 37:
All channel (0-95) IDAC_CH (maximum current) control by "GDAC (REG: 0x00C1)" or every channel IDAC_CH (maximum current) control by specific dac "IDAC_CHx (REG 0x0060 - 0x00BF)"
Bit[5]=0 … MAX current control by IDAC_CHx.
Bit[5]=1 … MAX current control by GDAC.

Note 38:
All channel (0-95) BR_CH (Brightness) control by "GBRI (REG: 0x00C0)" or every channel BR_CH (Brightness) control by specific brightness "BR_CHx (REG 0x0000 - 0x005F)"
Bit[4]=0 … MAX current control by BR_CHx.
Bit[4]=1 … MAX current control by GBRI.

MPRT

APE5035 has MPRT function to insert black picture. It's provide the blank time and active time to adjustment.
the blank time is main decided to insert black picture time. the blank start time was from Vsync rising edge until that's time was stop and then the active time will continue to blank stop time to LED current conduction time to stop. by the way; the active time is main decide LED current conduction time.
the register 0x00D4 bit[11] is setting this function enable or disable. That bit is setting to 1 then MPRT function will be enable, on the contrary; it's will be disable.
the register 0x00F6 bits[9:0] and 0x00F7 bits[9:0] are setting blank time and active time. The both adjustment range is from 0 to 1023 and every 1/LSB. For the application using. The sum of blank time and active time were not over than 1023. If blank and active total time was more than 1023, then real active time will be change to (1023 minus active), otherwise; active time was keeping to original time. The waveform is shown the figure 6 as below.



$$ILED = ILED_{SETTING} * \frac{Active\ (real\ active)}{1023}$$

Figure 6: MPRT

Function Description (Cont.)

VSYNC Detection

The APE5035 has VSYNC detection function, the register 0x00D4 bit[2] is setting to 1 then detect VSYNC signal. If VSYNC is not exist then ILED current will be turn off, on the contrary; then ILED current is exist.

Table 23: ILED Output Control Register

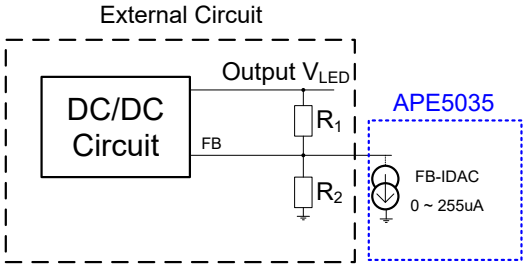
Address	Bit	Name	Description
0x00D4h	[2]	VSYNC_detect	Note 39

Note 39:
Bit[2]=0 … VSYNC detection disabled.
Bit[2]=1 … VSYNC detection enabled.

All outputs are turned off if VSYNC signal is missing for 100ms.

Dynamic Feedback Control

The APE5035 has FB1 and FB2 terminal can be connect to feedback pin of external DC/DC circuit and control output voltage (V_{LED}) for optimal power efficiency.
The dynamic control mechanism is according to output voltage is not enough condition and then increasing the FB-IDAC value, at the same time; output voltage also increase until to LED current achieve target.
In order to simplify design step, a few process step provide calculate and design as below:



Step 1: Calculate R1
The output voltage is depending on min to max range of LED. Design the R1 value according to with max IDAC value 255uA as below formula:

$$R_1 = \frac{V_{LED(MAX)} - V_{LED(MIN)}}{255uA}$$

Suggestion the R1 value multiply by IDAC current max value is not more than over voltage protection point of external DC/DC circuit. Otherwise; when the IDAC value is increasing to max value then happen protection of external DC/DC circuit. Secondly; the LED output voltage max to min range must according to actual LED specification.

Step 2: Calculate R2
The R2 value calculates as below formula:

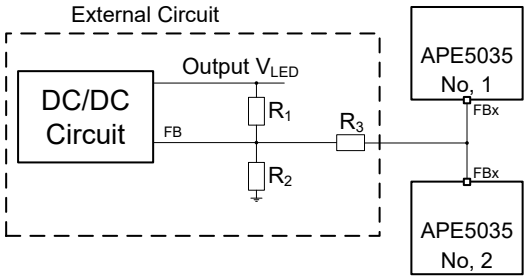
$$R_2 = \frac{R_1}{(\frac{V_{LED(MIN)}}{V_{FB}} - 1)}$$

The APE5035 using automatic mode and manual mode can be adjustment FB-IDAC current. If adjustment mode is choosing the manual mode, then using address 0x00D7 bit[5] and bit[4] setting to 1 and increasing the address 0x00D8 bits[15:8] and 0x00D8 bits[7:0] value so that increasing output voltage.
According to formula as below:

$$V_{LED(MAX)} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB} + R_1 \times FB\_IDAC_{(COUNTER)} \times 1uA$$

If one DC/DC converter is connected 2 or more than APE5035 structure suggest series resistor between FBx terminal and DC/DC circuit feedback terminal let FBx current can up to 255uA. The R3 value calculates as below:

$$R_3 = \frac{V_{FB}}{255uA}$$



If possible; try to let FBx pin terminal keep to 0.25V and it's not less than 0.25V.

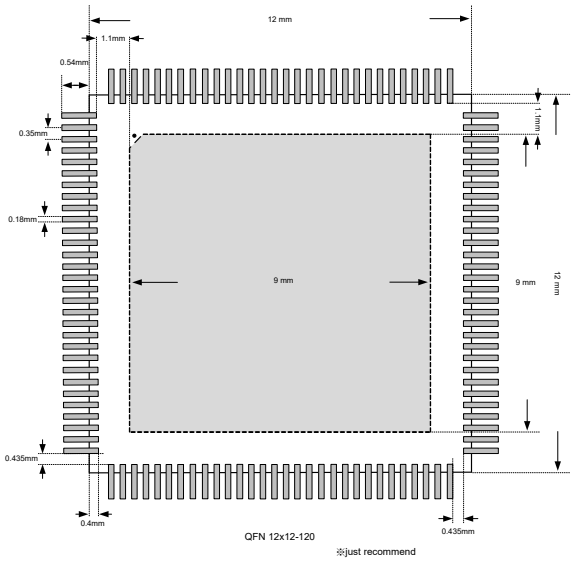
Application Information

Layout Consideration

The APE5035 was using less external components. Suggestion the RSET, input capacitor and VDD5/VDD3 capacitor are as possible closed to IC terminal.
If using APE5035 the layout consideration can be seen as below figure. When LED current was larges can cause to thermal issue, suggestion using to via then solve the thermal issue.
The holes and via numbers can be effect to thermal, if using holes and via are more, the thermal issue will be decreasing. Thermal problem can using as below points can decrease the thermal issue:

1. Increasing the PCB dimension and add the copper plating of ground side areas.
2. If possible, the PCB layers suggest using 4 layers or more than layer is better.
3. Using the holes size and via connect to all layers and then decrease the thermal issue. To sum it up, according to as be above points, the thermal issue will be effective decreasing and solution.

Minimum Footprint



Register Map

Register Address (hex)	Name	BIT	Label	Default	Description
0x0000	BR_CH0	[13:0]	BR_CH_0[13:0]	00_0000_0000_0000	Channel 0 output current=br_ch_0 x idac Channel 0 brightness control (0.0061% per step) Dither Mode (data width 14bit) 0x0000: 0% (default) 0x0001: 0.10375977% (17/1024*16) 0x0002: 0.10986328% (18/1024*16) 0x0003: 0.11596678% (19/1024*16) 0x0004: 0.12207031% (20/1024*16) 0x0005: 0.12817382% (21/1024*16) 0x0006: 0.13427734% (22/1024*16) 0x0007: 0.14038086% (23/1024*16) … 0x0011: 0.20141602% (33/1024*16) ... 0x00A4: 1.09863281% (180/1024*16) ... 0x0657: 10.00366211% (1639/1024*16) ... 0x1FF0: 50.00000000% (8192/1024*16) ... 0x3FEE: 99.98779297% (16382/1024*16) 0x3FEF: 99.99389648% (16383/1024*16) 0x3FF0: 100.00000000% (16384/1024*16) 0x3FF1: 100.00000000% (16384/1024*16) ... 0x3FFF: 100.00000000% (16384/1024*16) ---------- Normal Mode (data width 10bit) (0.09765625% per step) 0x0000: 0% (default) 0x0001: 0.19531250% (2/1024) 0x0002: 0.29296875% (3/1024) 0x0003: 0.39062500% (4/1024) 0x0004: 0.48828125% (5/1024) 0x0005: 0.58593750% (6/1024) 0x0006: 0.68389375% (7/1024) 0x0007: 0.78125000% (8/1024) … 0x01FF: 50.00000000% (511/1024) ... 0x03FE: 99.90234375% (1023/1024) 0x03FF: 100.00000000% (1024/1024)

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0001	BR_CH1	[13:0]	BR_CH_1[13:0]	00_0000_0000_0000	CH1 PWM Brightness
0x0002	BR_CH2	[13:0]	BR_CH_2[13:0]	00_0000_0000_0000	CH2 PWM Brightness
0x0003	BR_CH3	[13:0]	BR_CH_3[13:0]	00_0000_0000_0000	CH3 PWM Brightness
0x0004	BR_CH4	[13:0]	BR_CH_4[13:0]	00_0000_0000_0000	CH4 PWM Brightness
0x0005	BR_CH5	[13:0]	BR_CH_5[13:0]	00_0000_0000_0000	CH5 PWM Brightness
0x0006	BR_CH6	[13:0]	BR_CH_6[13:0]	00_0000_0000_0000	CH6 PWM Brightness
0x0007	BR_CH7	[13:0]	BR_CH_7[13:0]	00_0000_0000_0000	CH7 PWM Brightness
0x0008	BR_CH8	[13:0]	BR_CH_8[13:0]	00_0000_0000_0000	CH8 PWM Brightness
0x0009	BR_CH9	[13:0]	BR_CH_9[13:0]	00_0000_0000_0000	CH9 PWM Brightness
0x000A	BR_CH10	[13:0]	BR_CH_10[13:0]	00_0000_0000_0000	CH10 PWM Brightness
0x000B	BR_CH11	[13:0]	BR_CH_11[13:0]	00_0000_0000_0000	CH11 PWM Brightness
0x000C	BR_CH12	[13:0]	BR_CH_12[13:0]	00_0000_0000_0000	CH12 PWM Brightness
0x000D	BR_CH13	[13:0]	BR_CH_13[13:0]	00_0000_0000_0000	CH13 PWM Brightness
0x000E	BR_CH14	[13:0]	BR_CH_14[13:0]	00_0000_0000_0000	CH14 PWM Brightness
0x000F	BR_CH15	[13:0]	BR_CH_15[13:0]	00_0000_0000_0000	CH15 PWM Brightness
0x0010	BR_CH16	[13:0]	BR_CH_16[13:0]	00_0000_0000_0000	CH16 PWM Brightness
0x0011	BR_CH17	[13:0]	BR_CH_17[13:0]	00_0000_0000_0000	CH17 PWM Brightness
0x0012	BR_CH18	[13:0]	BR_CH_18[13:0]	00_0000_0000_0000	CH18 PWM Brightness
0x0013	BR_CH19	[13:0]	BR_CH_19[13:0]	00_0000_0000_0000	CH19 PWM Brightness
0x0014	BR_CH20	[13:0]	BR_CH_20[13:0]	00_0000_0000_0000	CH20 PWM Brightness
0x0015	BR_CH21	[13:0]	BR_CH_21[13:0]	00_0000_0000_0000	CH21 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0016	BR_CH22	[13:0]	BR_CH_22[13:0]	00_0000_0000_0000	CH22 PWM Brightness
0x0017	BR_CH23	[13:0]	BR_CH_23[13:0]	00_0000_0000_0000	CH23 PWM Brightness
0x0018	BR_CH24	[13:0]	BR_CH_24[13:0]	00_0000_0000_0000	CH24 PWM Brightness
0x0019	BR_CH25	[13:0]	BR_CH_25[13:0]	00_0000_0000_0000	CH25 PWM Brightness
0x001A	BR_CH26	[13:0]	BR_CH_26[13:0]	00_0000_0000_0000	CH26 PWM Brightness
0x001B	BR_CH27	[13:0]	BR_CH_27[13:0]	00_0000_0000_0000	CH27 PWM Brightness
0x001C	BR_CH28	[13:0]	BR_CH_28[13:0]	00_0000_0000_0000	CH28 PWM Brightness
0x001D	BR_CH29	[13:0]	BR_CH_29[13:0]	00_0000_0000_0000	CH29 PWM Brightness
0x001E	BR_CH30	[13:0]	BR_CH_30[13:0]	00_0000_0000_0000	CH30 PWM Brightness
0x001F	BR_CH31	[13:0]	BR_CH_31[13:0]	00_0000_0000_0000	CH31 PWM Brightness
0x0020	BR_CH32	[13:0]	BR_CH_32[13:0]	00_0000_0000_0000	CH32 PWM Brightness
0x0021	BR_CH33	[13:0]	BR_CH_33[13:0]	00_0000_0000_0000	CH33 PWM Brightness
0x0022	BR_CH34	[13:0]	BR_CH_34[13:0]	00_0000_0000_0000	CH34 PWM Brightness
0x0023	BR_CH35	[13:0]	BR_CH_35[13:0]	00_0000_0000_0000	CH35 PWM Brightness
0x0024	BR_CH36	[13:0]	BR_CH_36[13:0]	00_0000_0000_0000	CH36 PWM Brightness
0x0025	BR_CH37	[13:0]	BR_CH_37[13:0]	00_0000_0000_0000	CH37 PWM Brightness
0x0026	BR_CH38	[13:0]	BR_CH_38[13:0]	00_0000_0000_0000	CH38 PWM Brightness
0x0027	BR_CH39	[13:0]	BR_CH_39[13:0]	00_0000_0000_0000	CH39 PWM Brightness
0x0028	BR_CH40	[13:0]	BR_CH_40[13:0]	00_0000_0000_0000	CH40 PWM Brightness
0x0029	BR_CH41	[13:0]	BR_CH_41[13:0]	00_0000_0000_0000	CH41 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x002A	BR_CH42	[13:0]	BR_CH_42[13:0]	00_0000_0000_0000	CH42 PWM Brightness
0x002B	BR_CH43	[13:0]	BR_CH_43[13:0]	00_0000_0000_0000	CH43 PWM Brightness
0x002C	BR_CH44	[13:0]	BR_CH_44[13:0]	00_0000_0000_0000	CH44 PWM Brightness
0x002D	BR_CH45	[13:0]	BR_CH_45[13:0]	00_0000_0000_0000	CH45 PWM Brightness
0x002E	BR_CH46	[13:0]	BR_CH_46[13:0]	00_0000_0000_0000	CH46 PWM Brightness
0x002F	BR_CH47	[13:0]	BR_CH_47[13:0]	00_0000_0000_0000	CH47 PWM Brightness
0x0030	BR_CH48	[13:0]	BR_CH_48[13:0]	00_0000_0000_0000	CH48 PWM Brightness
0x0031	BR_CH49	[13:0]	BR_CH_49[13:0]	00_0000_0000_0000	CH49 PWM Brightness
0x0032	BR_CH50	[13:0]	BR_CH_50[13:0]	00_0000_0000_0000	CH50 PWM Brightness
0x0033	BR_CH51	[13:0]	BR_CH_51[13:0]	00_0000_0000_0000	CH51 PWM Brightness
0x0034	BR_CH52	[13:0]	BR_CH_52[13:0]	00_0000_0000_0000	CH52 PWM Brightness
0x0035	BR_CH53	[13:0]	BR_CH_53[13:0]	00_0000_0000_0000	CH53 PWM Brightness
0x0036	BR_CH54	[13:0]	BR_CH_54[13:0]	00_0000_0000_0000	CH54 PWM Brightness
0x0037	BR_CH55	[13:0]	BR_CH_55[13:0]	00_0000_0000_0000	CH55 PWM Brightness
0x0038	BR_CH56	[13:0]	BR_CH_56[13:0]	00_0000_0000_0000	CH56 PWM Brightness
0x0039	BR_CH57	[13:0]	BR_CH_57[13:0]	00_0000_0000_0000	CH57 PWM Brightness
0x003A	BR_CH58	[13:0]	BR_CH_58[13:0]	00_0000_0000_0000	CH58 PWM Brightness
0x003B	BR_CH59	[13:0]	BR_CH_59[13:0]	00_0000_0000_0000	CH59 PWM Brightness
0x003C	BR_CH60	[13:0]	BR_CH_60[13:0]	00_0000_0000_0000	CH60 PWM Brightness
0x003D	BR_CH61	[13:0]	BR_CH_61[13:0]	00_0000_0000_0000	CH61 PWM Brightness
0x003E	BR_CH62	[13:0]	BR_CH_62[13:0]	00_0000_0000_0000	CH62 PWM Brightness
0x003F	BR_CH63	[13:0]	BR_CH_63[13:0]	00_0000_0000_0000	CH63 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0040	BR_CH64	[13:0]	BR_CH_64[13:0]	00_0000_0000_0000	CH64 PWM Brightness
0x0041	BR_CH65	[13:0]	BR_CH_65[13:0]	00_0000_0000_0000	CH65 PWM Brightness
0x0042	BR_CH66	[13:0]	BR_CH_66[13:0]	00_0000_0000_0000	CH66 PWM Brightness
0x0043	BR_CH67	[13:0]	BR_CH_67[13:0]	00_0000_0000_0000	CH67 PWM Brightness
0x0044	BR_CH68	[13:0]	BR_CH_68[13:0]	00_0000_0000_0000	CH68 PWM Brightness
0x0045	BR_CH69	[13:0]	BR_CH_69[13:0]	00_0000_0000_0000	CH69 PWM Brightness
0x0046	BR_CH70	[13:0]	BR_CH_70[13:0]	00_0000_0000_0000	CH70 PWM Brightness
0x0047	BR_CH71	[13:0]	BR_CH_71[13:0]	00_0000_0000_0000	CH71 PWM Brightness
0x0048	BR_CH72	[13:0]	BR_CH_72[13:0]	00_0000_0000_0000	CH72 PWM Brightness
0x0049	BR_CH73	[13:0]	BR_CH_73[13:0]	00_0000_0000_0000	CH73 PWM Brightness
0x004A	BR_CH74	[13:0]	BR_CH_74[13:0]	00_0000_0000_0000	CH74 PWM Brightness
0x004B	BR_CH75	[13:0]	BR_CH_75[13:0]	00_0000_0000_0000	CH75 PWM Brightness
0x004C	BR_CH76	[13:0]	BR_CH_76[13:0]	00_0000_0000_0000	CH76 PWM Brightness
0x004D	BR_CH77	[13:0]	BR_CH_77[13:0]	00_0000_0000_0000	CH77 PWM Brightness
0x004E	BR_CH78	[13:0]	BR_CH_78[13:0]	00_0000_0000_0000	CH78 PWM Brightness
0x004F	BR_CH79	[13:0]	BR_CH_79[13:0]	00_0000_0000_0000	CH79 PWM Brightness
0x0050	BR_CH80	[13:0]	BR_CH_80[13:0]	00_0000_0000_0000	CH80 PWM Brightness
0x0051	BR_CH81	[13:0]	BR_CH_81[13:0]	00_0000_0000_0000	CH81 PWM Brightness
0x0052	BR_CH82	[13:0]	BR_CH_82[13:0]	00_0000_0000_0000	CH82 PWM Brightness
0x0053	BR_CH83	[13:0]	BR_CH_83[13:0]	00_0000_0000_0000	CH83 PWM Brightness
0x0054	BR_CH84	[13:0]	BR_CH_84[13:0]	00_0000_0000_0000	CH84 PWM Brightness
0x0055	BR_CH85	[13:0]	BR_CH_85[13:0]	00_0000_0000_0000	CH85 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0056	BR_CH86	[13:0]	BR_CH_86[13:0]	00_0000_0000_0000	CH86 PWM Brightness
0x0057	BR_CH87	[13:0]	BR_CH_87[13:0]	00_0000_0000_0000	CH87 PWM Brightness
0x0058	BR_CH88	[13:0]	BR_CH_88[13:0]	00_0000_0000_0000	CH88 PWM Brightness
0x0059	BR_CH89	[13:0]	BR_CH_89[13:0]	00_0000_0000_0000	CH89 PWM Brightness
0x005A	BR_CH90	[13:0]	BR_CH_90[13:0]	00_0000_0000_0000	CH90 PWM Brightness
0x005B	BR_CH91	[13:0]	BR_CH_91[13:0]	00_0000_0000_0000	CH91 PWM Brightness
0x005C	BR_CH92	[13:0]	BR_CH_92[13:0]	00_0000_0000_0000	CH92 PWM Brightness
0x005D	BR_CH93	[13:0]	BR_CH_93[13:0]	00_0000_0000_0000	CH93 PWM Brightness
0x005E	BR_CH94	[13:0]	BR_CH_94[13:0]	00_0000_0000_0000	CH94 PWM Brightness
0x005F	BR_CH95	[13:0]	BR_CH_95[13:0]	00_0000_0000_0000	CH95 PWM Brightness
0x0060	IDAC_CH0	[9:0]	IDAC_CH_0[9:0]	01_0101_0010	IDAC: single channel maximum current control (29.637uA per step), setting active 0x000: 0mA 0x001: 0.029636mA 0x002: 0.059273mA 0x003: 0.088909mA 0x004: 0.118545mA 0x005: 0.148182mA 0x006: 0.177818mA 0x007: 0.207455mA … 0x047: 2.104182mA ... 0x11A: 8.357455mA ... **0x152: 10.017mA (default)** ... 0x1A6: 12.506545mA ... 0x2C0: 20.86400mA ... 0x3FF: 30.318mA
0x0061	IDAC_CH1	[9:0]	IDAC_CH_1[9:0]	01_0101_0010	CH1 IDAC current
0x0062	IDAC_CH2	[9:0]	IDAC_CH_2[9:0]	01_0101_0010	CH2 IDAC current
0x0063	IDAC_CH3	[9:0]	IDAC_CH_3[9:0]	01_0101_0010	CH3 IDAC current
0x0064	IDAC_CH4	[9:0]	IDAC_CH_4[9:0]	01_0101_0010	CH4 IDAC current
0x0065	IDAC_CH5	[9:0]	IDAC_CH_5[9:0]	01_0101_0010	CH5 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0066	IDAC_CH6	[9:0]	IDAC_CH_6[9:0]	01_0101_0010	CH6 IDAC current
0x0067	IDAC_CH7	[9:0]	IDAC_CH_7[9:0]	01_0101_0010	CH7 IDAC current
0x0068	IDAC_CH8	[9:0]	IDAC_CH_8[9:0]	01_0101_0010	CH8 IDAC current
0x0069	IDAC_CH9	[9:0]	IDAC_CH_9[9:0]	01_0101_0010	CH9 IDAC current
0x006A	IDAC_CH10	[9:0]	IDAC_CH_10[9:0]	01_0101_0010	CH10 IDAC current
0x006B	IDAC_CH11	[9:0]	IDAC_CH_11[9:0]	01_0101_0010	CH11 IDAC current
0x006C	IDAC_CH12	[9:0]	IDAC_CH_12[9:0]	01_0101_0010	CH12 IDAC current
0x006D	IDAC_CH13	[9:0]	IDAC_CH_13[9:0]	01_0101_0010	CH13 IDAC current
0x006E	IDAC_CH14	[9:0]	IDAC_CH_14[9:0]	01_0101_0010	CH14 IDAC current
0x006F	IDAC_CH15	[9:0]	IDAC_CH_15[9:0]	01_0101_0010	CH15 IDAC current
0x0070	IDAC_CH16	[9:0]	IDAC_CH_16[9:0]	01_0101_0010	CH16 IDAC current
0x0071	IDAC_CH17	[9:0]	IDAC_CH_17[9:0]	01_0101_0010	CH17 IDAC current
0x0072	IDAC_CH18	[9:0]	IDAC_CH_18[9:0]	01_0101_0010	CH18 IDAC current
0x0073	IDAC_CH19	[9:0]	IDAC_CH_19[9:0]	01_0101_0010	CH19 IDAC current
0x0074	IDAC_CH20	[9:0]	IDAC_CH_20[9:0]	01_0101_0010	CH20 IDAC current
0x0075	IDAC_CH21	[9:0]	IDAC_CH_21[9:0]	01_0101_0010	CH21 IDAC current
0x0076	IDAC_CH22	[9:0]	IDAC_CH_22[9:0]	01_0101_0010	CH22 IDAC current
0x0077	IDAC_CH23	[9:0]	IDAC_CH_23[9:0]	01_0101_0010	CH23 IDAC current
0x0078	IDAC_CH24	[9:0]	IDAC_CH_24[9:0]	01_0101_0010	CH24 IDAC current
0x0079	IDAC_CH25	[9:0]	IDAC_CH_25[9:0]	01_0101_0010	CH25 IDAC current
0x007A	IDAC_CH26	[9:0]	IDAC_CH_26[9:0]	01_0101_0010	CH26 IDAC current
0x007B	IDAC_CH27	[9:0]	IDAC_CH_27[9:0]	01_0101_0010	CH27 IDAC current
0x007C	IDAC_CH28	[9:0]	IDAC_CH_28[9:0]	01_0101_0010	CH28 IDAC current
0x007D	IDAC_CH29	[9:0]	IDAC_CH_29[9:0]	01_0101_0010	CH29 IDAC current
0x007E	IDAC_CH30	[9:0]	IDAC_CH_30[9:0]	01_0101_0010	CH30 IDAC current
0x007F	IDAC_CH31	[9:0]	IDAC_CH_31[9:0]	01_0101_0010	CH31 IDAC current
0x0080	IDAC_CH32	[9:0]	IDAC_CH_32[9:0]	01_0101_0010	CH32 IDAC current
0x0081	IDAC_CH33	[9:0]	IDAC_CH_33[9:0]	01_0101_0010	CH33 IDAC current
0x0082	IDAC_CH34	[9:0]	IDAC_CH_34[9:0]	01_0101_0010	CH34 IDAC current
0x0083	IDAC_CH35	[9:0]	IDAC_CH_35[9:0]	01_0101_0010	CH35 IDAC current
0x0084	IDAC_CH36	[9:0]	IDAC_CH_36[9:0]	01_0101_0010	CH36 IDAC current
0x0085	IDAC_CH37	[9:0]	IDAC_CH_37[9:0]	01_0101_0010	CH37 IDAC current
0x0086	IDAC_CH38	[9:0]	IDAC_CH_38[9:0]	01_0101_0010	CH38 IDAC current
0x0087	IDAC_CH39	[9:0]	IDAC_CH_39[9:0]	01_0101_0010	CH39 IDAC current
0x0088	IDAC_CH40	[9:0]	IDAC_CH_40[9:0]	01_0101_0010	CH40 IDAC current
0x0089	IDAC_CH41	[9:0]	IDAC_CH_41[9:0]	01_0101_0010	CH41 IDAC current
0x008A	IDAC_CH42	[9:0]	IDAC_CH_42[9:0]	01_0101_0010	CH42 IDAC current
0x008B	IDAC_CH43	[9:0]	IDAC_CH_43[9:0]	01_0101_0010	CH43 IDAC current
0x008C	IDAC_CH44	[9:0]	IDAC_CH_44[9:0]	01_0101_0010	CH44 IDAC current
0x008D	IDAC_CH45	[9:0]	IDAC_CH_45[9:0]	01_0101_0010	CH45 IDAC current
0x008E	IDAC_CH46	[9:0]	IDAC_CH_46[9:0]	01_0101_0010	CH46 IDAC current
0x008F	IDAC_CH47	[9:0]	IDAC_CH_47[9:0]	01_0101_0010	CH47 IDAC current
0x0090	IDAC_CH48	[9:0]	IDAC_CH_48[9:0]	01_0101_0010	CH48 IDAC current
0x0091	IDAC_CH49	[9:0]	IDAC_CH_49[9:0]	01_0101_0010	CH49 IDAC current
0x0092	IDAC_CH50	[9:0]	IDAC_CH_50[9:0]	01_0101_0010	CH50 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0093	IDAC_CH51	[9:0]	IDAC_CH_51[9:0]	01_0101_0010	CH51 IDAC current
0x0094	IDAC_CH52	[9:0]	IDAC_CH_52[9:0]	01_0101_0010	CH52 IDAC current
0x0095	IDAC_CH53	[9:0]	IDAC_CH_53[9:0]	01_0101_0010	CH53 IDAC current
0x0096	IDAC_CH54	[9:0]	IDAC_CH_54[9:0]	01_0101_0010	CH54 IDAC current
0x0097	IDAC_CH55	[9:0]	IDAC_CH_55[9:0]	01_0101_0010	CH55 IDAC current
0x0098	IDAC_CH56	[9:0]	IDAC_CH_56[9:0]	01_0101_0010	CH56 IDAC current
0x0099	IDAC_CH57	[9:0]	IDAC_CH_57[9:0]	01_0101_0010	CH57 IDAC current
0x009A	IDAC_CH58	[9:0]	IDAC_CH_58[9:0]	01_0101_0010	CH58 IDAC current
0x009B	IDAC_CH59	[9:0]	IDAC_CH_59[9:0]	01_0101_0010	CH59 IDAC current
0x009C	IDAC_CH60	[9:0]	IDAC_CH_60[9:0]	01_0101_0010	CH60 IDAC current
0x009D	IDAC_CH61	[9:0]	IDAC_CH_61[9:0]	01_0101_0010	CH61 IDAC current
0x009E	IDAC_CH62	[9:0]	IDAC_CH_62[9:0]	01_0101_0010	CH62 IDAC current
0x009F	IDAC_CH63	[9:0]	IDAC_CH_63[9:0]	01_0101_0010	CH63 IDAC current
0x00A0	IDAC_CH64	[9:0]	IDAC_CH_64[9:0]	01_0101_0010	CH64 IDAC current
0x00A1	IDAC_CH65	[9:0]	IDAC_CH_65[9:0]	01_0101_0010	CH65 IDAC current
0x00A2	IDAC_CH66	[9:0]	IDAC_CH_66[9:0]	01_0101_0010	CH66 IDAC current
0x00A3	IDAC_CH67	[9:0]	IDAC_CH_67[9:0]	01_0101_0010	CH67 IDAC current
0x00A4	IDAC_CH68	[9:0]	IDAC_CH_68[9:0]	01_0101_0010	CH68 IDAC current
0x00A5	IDAC_CH69	[9:0]	IDAC_CH_69[9:0]	01_0101_0010	CH69 IDAC current
0x00A6	IDAC_CH70	[9:0]	IDAC_CH_70[9:0]	01_0101_0010	CH70 IDAC current
0x00A7	IDAC_CH71	[9:0]	IDAC_CH_71[9:0]	01_0101_0010	CH71 IDAC current
0x00A8	IDAC_CH72	[9:0]	IDAC_CH_72[9:0]	01_0101_0010	CH72 IDAC current
0x00A9	IDAC_CH73	[9:0]	IDAC_CH_73[9:0]	01_0101_0010	CH73 IDAC current
0x00AA	IDAC_CH74	[9:0]	IDAC_CH_74[9:0]	01_0101_0010	CH74 IDAC current
0x00AB	IDAC_CH75	[9:0]	IDAC_CH_75[9:0]	01_0101_0010	CH75 IDAC current
0x00AC	IDAC_CH76	[9:0]	IDAC_CH_76[9:0]	01_0101_0010	CH76 IDAC current
0x00AD	IDAC_CH77	[9:0]	IDAC_CH_77[9:0]	01_0101_0010	CH77 IDAC current
0x00AE	IDAC_CH78	[9:0]	IDAC_CH_78[9:0]	01_0101_0010	CH78 IDAC current
0x00AF	IDAC_CH79	[9:0]	IDAC_CH_79[9:0]	01_0101_0010	CH79 IDAC current
0x00B0	IDAC_CH80	[9:0]	IDAC_CH_80[9:0]	01_0101_0010	CH80 IDAC current
0x00B1	IDAC_CH81	[9:0]	IDAC_CH_81[9:0]	01_0101_0010	CH81 IDAC current
0x00B2	IDAC_CH82	[9:0]	IDAC_CH_82[9:0]	01_0101_0010	CH82 IDAC current
0x00B3	IDAC_CH83	[9:0]	IDAC_CH_83[9:0]	01_0101_0010	CH83 IDAC current
0x00B4	IDAC_CH84	[9:0]	IDAC_CH_84[9:0]	01_0101_0010	CH84 IDAC current
0x00B5	IDAC_CH85	[9:0]	IDAC_CH_85[9:0]	01_0101_0010	CH85 IDAC current
0x00B6	IDAC_CH86	[9:0]	IDAC_CH_86[9:0]	01_0101_0010	CH86 IDAC current
0x00B7	IDAC_CH87	[9:0]	IDAC_CH_87[9:0]	01_0101_0010	CH87 IDAC current
0x00B8	IDAC_CH88	[9:0]	IDAC_CH_88[9:0]	01_0101_0010	CH88 IDAC current
0x00B9	IDAC_CH89	[9:0]	IDAC_CH_89[9:0]	01_0101_0010	CH89 IDAC current
0x00BA	IDAC_CH90	[9:0]	IDAC_CH_90[9:0]	01_0101_0010	CH90 IDAC current
0x00BB	IDAC_CH91	[9:0]	IDAC_CH_91[9:0]	01_0101_0010	CH91 IDAC current
0x00BC	IDAC_CH92	[9:0]	IDAC_CH_92[9:0]	01_0101_0010	CH92 IDAC current
0x00BD	IDAC_CH93	[9:0]	IDAC_CH_93[9:0]	01_0101_0010	CH93 IDAC current
0x00BE	IDAC_CH94	[9:0]	IDAC_CH_94[9:0]	01_0101_0010	CH94 IDAC current
0x00BF	IDAC_CH95	[9:0]	IDAC_CH_95[9:0]	01_0101_0010	CH95 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00C0	GBRI	[13:0]	GBRI[13:0]	00_0000_0000_0000	See register 0x0000 description
0x00C1	GDAC	[9:0]	GDAC[9:0]	01_0101_0010	See register 0x0060 description
0x00C2	CUR_ON_1	[15]	CUR_ON_CH15	0	Channel 15 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[14]	CUR_ON_CH14	0	Channel 14 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[13]	CUR_ON_CH13	0	Channel 13 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[12]	CUR_ON_CH12	0	Channel 12 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[11]	CUR_ON_CH11	0	Channel 11 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[10]	CUR_ON_CH10	0	Channel 10 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[9]	CUR_ON_CH9	0	Channel 9 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[8]	CUR_ON_CH8	0	Channel 8 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[7]	CUR_ON_CH7	0	Channel 7 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[6]	CUR_ON_CH6	0	Channel 6 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[5]	CUR_ON_CH5	0	Channel 5 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[4]	CUR_ON_CH4	0	Channel 4 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[3]	CUR_ON_CH3	0	Channel 3 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[2]	CUR_ON_CH2	0	Channel 2 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[1]	CUR_ON_CH1	0	Channel 1 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[0]	CUR_ON_CH0	0	Channel 0 current output driver control: **0: output driver disabled (default)** 1: output driver enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00C3	CUR_ON_2	[15:0]	CURR_ON_CH31 - CURR_ON_CH16	0000_0000_0000_0000	Channel 31 - 16 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x00C4	CUR_ON_3	[15:0]	CURR_ON_CH47 - CURR_ON_CH32	0000_0000_0000_0000	Channel 47 - 32 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x00C5	CUR_ON_4	[15:0]	CURR_ON_CH63 - CURR_ON_CH48	0000_0000_0000_0000	Channel 63 - 48 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x00C6	CUR_ON_5	[15:0]	CURR_ON_CH79 - CURR_ON_CH64	0000_0000_0000_0000	Channel 79 - 64 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x00C7	CUR_ON_6	[15:0]	CURR_ON_CH95 - CURR_ON_CH80	0000_0000_0000_0000	Channel 95 - 80 current output driver control: **0: output driver disabled (default)** 1: output driver enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00C8	FB_SEL_1	[15]	FB_SEL_15	0	Select FB channel 15 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[14]	FB_SEL_14	0	Select FB channel 14 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB3
		[13]	FB_SEL_13	0	Select FB channel 13 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB4
		[12]	FB_SEL_12	0	Select FB channel 12 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB5
		[11]	FB_SEL_11	0	Select FB channel 11 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB6
		[10]	FB_SEL_10	0	Select FB channel 10 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB7
		[9]	FB_SEL_9	0	Select FB channel 9 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB8
		[8]	FB_SEL_8	0	Select FB channel 8 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB9
		[7]	FB_SEL_7	0	Select FB channel 7 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[6]	FB_SEL_6	0	Select FB channel 6 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[5]	FB_SEL_5	0	Select FB channel 5 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[4]	FB_SEL_4	0	Select FB channel 4 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[3]	FB_SEL_3	0	Select FB channel 3 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[2]	FB_SEL_2	0	Select FB channel 2 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[1]	FB_SEL_1	0	Select FB channel 1 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[0]	FB_SEL_0	0	Select FB channel 0 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00C9	FB_SEL_2	[15:0]	FB_SEL_31 - FB_SEL_16	0000_0000_0000_0000	Select FB channel 31 - 16 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x00CA	FB_SEL_3	[15:0]	FB_SEL_47 - FB_SEL_32	0000_0000_0000_0000	Select FB channel 47 - 32 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x00CB	FB_SEL_4	[15:0]	FB_SEL_63 - FB_SEL_48	0000_0000_0000_0000	Select FB channel 63 - 48 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x00CC	FB_SEL_5	[15:0]	FB_SEL_79 - FB_SEL_64	0000_0000_0000_0000	Select FB channel 79 - 64 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x00CD	FB_SEL_6	[15:0]	FB_SEL_95 - FB_SEL_80	0000_0000_0000_0000	Select FB channel 95 - 80 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x00CE	FB_ON_1	[15]	FB_ON_15	0	Enables feedback function of output channel 15: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[14]	FB_ON_14	0	Enables feedback function of output channel 14: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[13]	FB_ON_13	0	Enables feedback function of output channel 13: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[12]	FB_ON_12	0	Enables feedback function of output channel 12: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[11]	FB_ON_11	0	Enables feedback function of output channel 11: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[10]	FB_ON_10	0	Enables feedback function of output channel 10: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[9]	FB_ON_9	0	Enables feedback function of output channel 9: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[8]	FB_ON_8	0	Enables feedback function of output channel 8: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[7]	FB_ON_7	0	Enables feedback function of output channel 7: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00CE	FB_ON_1	[6]	FB_ON_6	0	Enables feedback function of output channel 6: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[5]	FB_ON_5	0	Enables feedback function of output channel 5: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[4]	FB_ON_4	0	Enables feedback function of output channel 4: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[3]	FB_ON_3	0	Enables feedback function of output channel 3: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[2]	FB_ON_2	0	Enables feedback function of output channel 2: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[1]	FB_ON_1	0	Enables feedback function of output channel 1: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[0]	FB_ON_0	0	Enables feedback function of output channel 0: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00CF	FB_ON_2	[15:0]	FB_ON_31 - FB_ON_16	0000_0000_0000_0000	Enables feedback function of output channels 31 - 16: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x00D0	FB_ON_3	[15:0]	FB_ON_47 - FB_ON_32	0000_0000_0000_0000	Enables feedback function of output channels 47 - 32: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x00D1	FB_ON_4	[15:0]	FB_ON_63 - FB_ON_48	0000_0000_0000_0000	Enables feedback function of output channels 63 - 48: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x00D2	FB_ON_5	[15:0]	FB_ON_79 - FB_ON_64	0000_0000_0000_0000	Enables feedback function of output channels 79 - 64: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x00D3	FB_ON_6	[15:0]	FB_ON_95 - FB_ON_80	0000_0000_0000_0000	Enables feedback function of output channels 95 - 80: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x00D4	CTRL	[15]	sw_reset	0	Software reset: **0: normal operation (default)** 1: software reset bit (resets all registers to default)
		[14:12]	pwm_freq_sel [2:0]	000	PWM output frequence selection: **000: 23KHz (default)** 001: 23KHz/2 010: 23KHz/4 011: 23KHz/8 100: 23KHz/16
		[11]	mprt_en	0	MPRT enable/disable: **0: Disable (default)** 1: Enable
		[10:8]	cgate_compensation [2:0]	000	Current output precharge compensation: **000: Off (default)** 001: Compensate 1 step for PWM output 010: Compensate 2 step for PWM output 011: Compensate 3 step for PWM output 100: Compensate 4 step for PWM output 101: Compensate 5 step for PWM output 110: Compensate 6 step for PWM output 111: Compensate 7 step for PWM output
		[7]	dither_en	1	Dither mode enable/disable: 0: Disable (Brightness resolution 10bit) **1: Enable (Brightness resolution 14bit) (default)**

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00D4	CTRL	[6]	dc_mode	0	PWM/DC Output current control: **0: channels output current - PWM (default)** 1: channels output current - DC (100% duty) Note. dc_mode=1, channels output current type is DC.
		[5]	clk_sel1	0	Clock source for internal PWM generators: **0: internal RC oscillator or HSYNC (depending on ClockSrc0) (default)** 1: DPLL output
		[4]	clk_sel0	0	Clock source for internal PWM generators: **0: internal RC oscillator (default)** 1: external pin HSYNC This bit only takes effect when clk_sel1=0
		[3]	pwm_inv	0	PWM control invert: **0: normal PWM operation (default)** 1: PWM signals are inverted Note: High time becomes Low Time
		[2]	vsync_detect	0	VSYNC detection: **0: VSYNC detection disabled (default)** 1: VSYNC detection enabled All outputs are turned off if VSYNC signal is missing for 100ms
		[1]	vsync_edge	0	Defines VSYNC trigger edge: **0: trigger on rising edge of VSYNC (default)** 1: trigger on falling edge of VSYNC
		[0]	update_mode	0	Defines when registers (brightness control) are updated: **0: Registers updated with rising edge of xCS (default)** 1: Registers updated with next VSYNC-edge
0x00D5	GLOBAL_CTRL	[15]	Standby	0	Standby mode - save power: **0: normal operation (default)** 1: Analog circuit power off (MOS) Digital circuit gating clock
		[14]	pwm_vsync_rst	0	PMW reset by VSYNC: **0: PWM continuous output** 1: PWM re-start after VSYNC edge
		[13:12]	pwm_mode [2:0]	00	PWM output type mode: **00: left-side mode (default)** 01: center mode 10: right-side mode
		[11]	gfb_on	0	All channel (0 - 95) FB_ON (Enables feedback) control: **0: feedback function of all channel disabled (default)** 1: feedback function of all channel enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00D5	GLOBAL_CTRL	[10]	gfb_on_ctrl_en	0	All channel (0 - 95) FB_ON (Enables feedback) control by "gfb_on (REG: 0x00D5[13])" or every channel FB_ON (Enables feedback) control by specific brightness "FB_ONx (REG 0x00CE - 0x00D3)" **0: FB_ON control by FB_ONx (default)** 1: FB_ON control by gfb_on
		[9]	gfb_sel	0	All channel select FB for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[8]	gfb_sel_ctrl_en	0	All channel (0 - 95) FB_SEL (select FB) control by "gfb_sel (REG: 0x00D5[11])" or every channel brightness control by specific brightness "FB_SELx (REG 0x00C8 - 0x00CD)" **0: FB_SEL control by FB_SELx (default)** 1: FB_SEL control by gfb_sel
		[7]	gcuron	0	All Channel current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[6]	gcuron_ctrl_en	0	All channel (0 - 95) CUR_ON control by "gcuron (REG: 0x00D5[9])" or every channel brightness control by specific brightness "CUR_ONx (REG 0x00C2 - 0x00C7)" **0: CUR_ON control by CUR_ONx (default)** 1: CUR_ON control by gcuron
		[5]	gdac_ctrl_en	0	All channel (0 - 95) IDAC_CH (maximum current) control by "GDAC (REG: 0x00C1)" or every channel IDAC_CH (maximum current) control by specific dac "IDAC_CHx (REG 0x0060 - 0x00BF)" **0: MAX current control by IDAC_CHx (default)** 1: MAX current control by GDAC
		[4]	gbri_ctrl_en	0	All channel (0 - 95) BR_CH (Brightness) control by "GBRI (REG: 0x00C0)" or every channel BR_CH (Brightness) control by specific brightness "BR_CHx (REG 0x0000 - 0x005F)" **0: MAX current control by BR_CHx (default)** 1: MAX current control by GBRI
		[3:2]	decay_time [1:0]	11	Decay time for power feedback control: 00: 16ms 01: 32ms 10: 64ms **11: 128ms (default)**
		[1]	fb2_decay_off	0	**0: FB counter 2 decay time is defined by register decay_time** 1: FB counter 2 decay time is infinite as long all high times in FB group 2 are 0
		[0]	fb1_decay_off	0	**0: FB counter 1 decay time is defined by register decay_time** 1: FB counter 1 decay time is infinite as long all high times in FB group 1 are 0

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00D6	FAULT_1	[15]	short_retrial	0	**0: retrial function disabled** 1: retrial function enabled Note: channels turned on every second.
		[14]	short_auto_off	0	**0: automatic turn off function disabled** 1: automatic turn off channels of shorted group
		[13]	LED_short_en	0	**0: short LED detection disabled** 1: short LED detection for all channels enabled
		[12:10]	short_level [2:0]	011	Short detection voltage: 000…3V 001…4V 010…5V **011…6V** 100…7V 101…8V 110…9V 111…12V
		[9:8]	short_debouncer [1:0]	11	00: 1 fault 01: 6 faults 10: 11 faults **11: 15 faults**
		[7]	open_retrial	0	**0: open LED retrial function disabled** 1: open LED retrial function enabled
		[6]	open_en	0	**0: open LED detection disabled** 1: open LED detection for all channels enabled
		[5]	open_auto_off	0	Automatic feedback turn off in case of open LED: **0: feedback function of open LED channel disabled** 1: feedback function of open LED channel automatically enabled
		[4]	otw_auto_off	0	**0: Warning temperature (OTW) shutdown disabled** 1: Warning temperature (OTW) shutdown enabled
		[3]	ovtemp_auto_off	1	0: temperature shutdown disabled **1: temperature shutdown enabled**
		[2]	-	-	-
		[1:0]	otw_sel [1:0]	11	OTW pin configuration: 00: 110°C 01: 120°C 10: 140°C **11: disable**

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00D7	IO_CTRL	[15:10]	-	-	-
		[9:8]	fault_io_config [1:0]	00	xFault pin configuration: **00: Open Drain / Pulldown** 01: Push - Pull 10: Disabled (HIZ) 11: not used
		[7:6]	sdo_io_config [1:0]	01	SDO output pin configuration: 00: Open Drain / Pulldown **01: Push - Pull** 10: Disabled (HIZ) 11: not used
		[5]	fbcounter_man_fb2	0	**0: FB2 counter in automatic mode** 1: FB2 counter is set manually
		[4]	fbcounter_man_fb1	0	**0: FB1 counter in automatic mode** 1: FB1 counter is set manually
		[3:2]	fbcounter_dn_time [1:0]	01	FB1 and FB2 down counting step time: 00: 512μs **01: 2048μs** 10: 4096μs 11: 8192μs
		[1:0]	fbcounter_up_time [1:0]	01	FB1 and FB2 up counting step time: 00: 1024μs **01: 256μs** 10: 64μs 11: 16μs
0x00D8	IDAC_FB_ COUNTER	[15:8]	idac_fb2_counter [7:0]	0000_0000	Feedback counter (IDAC) 2 value: **0x00: FB-current 0μA** 0xFF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb2=1
		[7:0]	idac_fb1_counter [7:0]	0000_0000	Feedback counter (IDAC) 1 value: **0x00: FB-current 0μA** 0xFF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb1=1
0x00D9	BIST_ CONTROL1	[15:6]	-	-	-
		[5]	short_bist_enable2	0	Short BIST enable for FB2: **0: BIST disabled (default)** 1: Start shortled BIST2 test
		[4]	short_bist_enable1	0	Short BIST enable for FB1: **0: BIST disabled (default)** 1: Start shortled BIST1 test
		[3]	bist_fast_time	0	Short BIST up/down time step: **0: 64μs (default)** 1: 128μs
		[2]	bist_select_time	0	**0: use bist_fast_time register value (default)** 1: use fbcounter_up_time / fbcounter_dn_time register values
		[1:0]	wait_sync_pulses [1:0]	10	Wait after BIST target has been reached: 0: no wait 01: wait 1 VSYNC pulse **10: wait 2 VSYNC pulses (default)** 11: wait 3 VSYNC pulses

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00DA	BIST_IDAC1	[7:0]	bist_idac1_val [7:0]	1111_1111	Defines the IDAC1 target value for BIST
	BIST_IDAC2	[7:0]	bist_idac2_val [7:0]	1111_1111	Defines the IDAC2 target value for BIST
0x00DB	STATUS	[15:8]	-	-	-
		[7]	CLKDCO_LOCK	0	1: notify Clock DCO frequency lock
		[6]	STAT OTW	0	1: notify over temperature warning
		[5]	STAT novsync	0	1: notify VSYNC is missing > 100ms
		[4]	STAT ov_temp	0	1: notify over temperature fault
		[3]	STAT open	0	1: notify open LED fault
		[2]	Short LED	0	1: notify short LED fault
		[1]	Short BIST	0	1: notify short BIST fault
		[0]	Power_good	0	0: no power supply (por or res=active) 1: device ok
0x00DC	SHORTLED_1	[15]	shortled_15	0	Notify shorted LED detected on output ch 15: Read: **0: No shorted LED detected** 1: Shorted LED detected Write: 1: clear fault
		[14]	shortled_14	0	Notify shorted LED detected on output ch 14
		[13]	shortled_13	0	Notify shorted LED detected on output ch 13
		[12]	shortled_12	0	Notify shorted LED detected on output ch 12
		[11]	shortled_11	0	Notify shorted LED detected on output ch 11
		[10]	shortled_10	0	Notify shorted LED detected on output ch 10
		[9]	shortled_9	0	Notify shorted LED detected on output ch 9
		[8]	shortled_8	0	Notify shorted LED detected on output ch 8
		[7]	shortled_7	0	Notify shorted LED detected on output ch 7
		[6]	shortled_6	0	Notify shorted LED detected on output ch 6
		[5]	shortled_5	0	Notify shorted LED detected on output ch 5
		[4]	shortled_4	0	Notify shorted LED detected on output ch 4
		[3]	shortled_3	0	Notify shorted LED detected on output ch 3
		[2]	shortled_2	0	Notify shorted LED detected on output ch 2
		[1]	shortled_1	0	Notify shorted LED detected on output ch 1
		[0]	shortled_0	0	Notify shorted LED detected on output ch 0
0x00DD	SHORTLED_2	[15:0]	shortled_31 - shortled_16	0000_0000_0000_0000	Notify shorted LED detected on output ch 31 - 16
0x00DE	SHORTLED_3	[15:0]	shortled_47 - shortled_32	0000_0000_0000_0000	Notify shorted LED detected on output ch 47 - 32
0x00DF	SHORTLED_4	[15:0]	shortled_63 - shortled_48	0000_0000_0000_0000	Notify shorted LED detected on output ch 63 - 48
0x00E0	SHORTLED_5	[15:0]	shortled_79 - shortled_64	0000_0000_0000_0000	Notify shorted LED detected on output ch 79 - 64
0x00E1	SHORTLED_6	[15:0]	shortled_95 - shortled_80	0000_0000_0000_0000	Notify shorted LED detected on output ch 95 - 80

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00E2	OPENLED_1	[15]	open_15	0	Notify open LED detected on output ch 15: Read: **0: No open LED detected** 1: Open LED detected Write: 1: clear fault
		[14]	open_14	0	Notify open LED detected on output ch 14
		[13]	open_13	0	Notify open LED detected on output ch 13
		[12]	open_12	0	Notify open LED detected on output ch 12
		[11]	open_11	0	Notify open LED detected on output ch 11
		[10]	open_10	0	Notify open LED detected on output ch 10
		[9]	open_9	0	Notify open LED detected on output ch 9
		[8]	open_8	0	Notify open LED detected on output ch 8
		[7]	open_7	0	Notify open LED detected on output ch 7
		[6]	open_6	0	Notify open LED detected on output ch 6
		[5]	open_5	0	Notify open LED detected on output ch 5
		[4]	open_4	0	Notify open LED detected on output ch 4
		[3]	open_3	0	Notify open LED detected on output ch 3
		[2]	open_2	0	Notify open LED detected on output ch 2
		[1]	open_1	0	Notify open LED detected on output ch 1
		[0]	open_0	0	Notify open LED detected on output ch 0
0x00E3	OPENLED_2	[15:0]	openled_31 - openled_16	0000_0000_0000_0000	Notify open LED detected on output ch 31 - 16
0x00E4	OPENLED_3	[15:0]	openled_47 - openled_32	0000_0000_0000_0000	Notify open LED detected on output ch 47 - 32
0x00E5	OPENLED_4	[15:0]	openled_63 - openled_48	0000_0000_0000_0000	Notify open LED detected on output ch 63 - 48
0x00E6	OPENLED_5	[15:0]	openled_79 - openled_64	0000_0000_0000_0000	Notify open LED detected on output ch 79 - 64
0x00E7	OPENLED_6	[15:0]	openled_95 - openled_80	0000_0000_0000_0000	Notify open LED detected on output ch 95 - 80

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00E8	COMP_REG1	[15]	comp_reg_15	0	Status of gate trip voltage comparator ch 15: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
		[14]	comp_reg_14	0	Status of gate trip voltage comparator ch 14
		[13]	comp_reg_13	0	Status of gate trip voltage comparator ch 13
		[12]	comp_reg_12	0	Status of gate trip voltage comparator ch 12
		[11]	comp_reg_11	0	Status of gate trip voltage comparator ch 11
		[10]	comp_reg_10	0	Status of gate trip voltage comparator ch 10
		[9]	comp_reg_9	0	Status of gate trip voltage comparator ch 9
		[8]	comp_reg_8	0	Status of gate trip voltage comparator ch 8
		[7]	comp_reg_7	0	Status of gate trip voltage comparator ch 7
		[6]	comp_reg_6	0	Status of gate trip voltage comparator ch 6
		[5]	comp_reg_5	0	Status of gate trip voltage comparator ch 5
		[4]	comp_reg_4	0	Status of gate trip voltage comparator ch 4
		[3]	comp_reg_3	0	Status of gate trip voltage comparator ch 3
		[2]	comp_reg_2	0	Status of gate trip voltage comparator ch 2
		[1]	comp_reg_1	0	Status of gate trip voltage comparator ch 1
		[0]	comp_reg_0	0	Status of gate trip voltage comparator ch 0
0x00E9	COMP_REG2	[15:0]	comp_reg_31 - comp_reg_16	0000_0000_0000_0000	Status of gate trip voltage comparator ch 31 - 16: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x00EA	COMP_REG3	[15:0]	comp_reg_47 - comp_reg_32	0000_0000_0000_0000	Status of gate trip voltage comparator ch 47 - 32: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x00EB	COMP_REG4	[15:0]	comp_reg_63 - comp_reg_48	0000_0000_0000_0000	Status of gate trip voltage comparator ch 63 - 48: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x00EC	COMP_REG5	[15:0]	comp_reg_79 - comp_reg_64	0000_0000_0000_0000	Status of gate trip voltage comparator ch 79 - 64: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x00ED	COMP_REG6	[15:0]	comp_reg_95 - comp_reg_80	0000_0000_0000_0000	Status of gate trip voltage comparator ch 95 - 80: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00EE	BIST_SHORT_1	[15]	bist_short_15	0	Short LED detected with BIST on ch 15: Read: **0: no short LED detected (default)** 1: Short LED detected Write: 1: clear fault
		[14]	bist_short_14	0	Short LED detected with BIST on ch 14
		[13]	bist_short_13	0	Short LED detected with BIST on ch 13
		[12]	bist_short_12	0	Short LED detected with BIST on ch 12
		[11]	bist_short_11	0	Short LED detected with BIST on ch 11
		[10]	bist_short_10	0	Short LED detected with BIST on ch 10
		[9]	bist_short_9	0	Short LED detected with BIST on ch 9
		[8]	bist_short_8	0	Short LED detected with BIST on ch 8
		[7]	bist_short_7	0	Short LED detected with BIST on ch 7
		[6]	bist_short_6	0	Short LED detected with BIST on ch 6
		[5]	bist_short_5	0	Short LED detected with BIST on ch 5
		[4]	bist_short_4	0	Short LED detected with BIST on ch 4
		[3]	bist_short_3	0	Short LED detected with BIST on ch 3
		[2]	bist_short_2	0	Short LED detected with BIST on ch 2
		[1]	bist_short_1	0	Short LED detected with BIST on ch 1
		[0]	bist_short_0	0	Short LED detected with BIST on ch 0
0x00EF	BIST_SHORT_2	[15:0]	bist_short_31 - bist_short_16	0000_0000_0000_0000	Short LED detected with BIST on ch 31 - 16
0x00F0	BIST_SHORT_3	[15:0]	bist_short_47 - bist_short_32	0000_0000_0000_0000	Short LED detected with BIST on ch 47 - 32
0x00F1	BIST_SHORT_4	[15:0]	bist_short_63 - bist_short_48	0000_0000_0000_0000	Short LED detected with BIST on ch 63 - 48
0x00F2	BIST_SHORT_5	[15:0]	bist_short_79 - bist_short_64	0000_0000_0000_0000	Short LED detected with BIST on ch 79 - 64
0x00F3	BIST_SHORT_6	[15:0]	bist_short_95 - bist_short_80	0000_0000_0000_0000	Short LED detected with BIST on ch 95 - 80

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00F4	COMP_CTRL	[15:11]	-	-	-
		[10]	comp_deb_en	1	COMP debounce (digital debounce) enable / disable: 0: disable **1: enable (default)**
		[9:4]	comp_deb_time [5:0]	00_0100	COMP debounce (digital debounce) time selection: 0.5μs/step 00_0000: 0μs 00_0001: 0.5μs 00_0010: 1μs 00_0011: 1.5μs **00_0100: 2μs (default)** … 11_1111: 31.5μs
		[3:2]	oled_r [1:0]	11	Reference voltage for feedback / open function Select LED PIN voltage threshold for feedback function LED pin configuration: 00: 0.275V 01: 0.25V 10: 0.225V **11: 0.2V (default)**
		[1:0]	cmp_d [1:0]	11	Select delay time for LED PIN detection: 00: 8μs 01: 4μs 10: 2μs **11: 1μs (default)**

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x00F5	HDR_CTRL	[15]	hdr_hw_en	0	HDR control select by hardware pin or register (0x00F5[3:0])
		[14:8]	hdr_tout [6:0]	001_1010	HDR hardware pin time out (8μs/per step) 0x1A: 208μs
		[7:4]	hdr_db [3:0]	0010	HDR hardware pin high level time setting: 0001: HDR high time > 8μs **0010: HDR high time > 16μs (default)** 0011: HDR high time > 24μs 0100: HDR high time > 32μs … 1111: HDR high time > 248μs
		[3:0]	hdr_level [3:0]	0000	HDR level control: **0000: 1 x IDAC** 0001: 0.9 x IDAC 0010: 0.8 x IDAC 0011: 0.7 x IDAC 0100: 0.6 x IDAC 0101: 0.5 x IDAC 0110: 0.4 x IDAC 0111: 0.3 x IDAC 1000: 0.2 x IDAC 1001: 0.1 x IDAC 1010: 1 x IDAC 1011: 0 x IDAC 1100: 0 x IDAC 1101: 0 x IDAC 1110: 0 x IDAC 1111: 0 x IDAC
0x00F6	MPRT_CTRL_1	[9:0]	mprt_blank [9:0]	00_0000_0001	MPRT control: blank time, percentage of VSYNC time MPRT blank time: mprt_blank/1023*VSYNC time (16.6ms - 60Hz)
0x00F7	MPRT_CTRL_2	[9:0]	mprt_active [9:0]	11_1111_1111	MPRT control: active time, time start from VSYNC edge MPRT active time: mprt_active/1023*VSYNC time (16.6ms - 60Hz)
0x00FC	OPENSHORT_ RETRIAL	[10:0]	retrial_time [10:0]	111_1100_1111	Open LED or Short LED Retrial Time (1ms/LSB) 000_0000_0001: 1ms 000_0000_0010: 2ms 000_0000_0011: 3ms … 111_1100_1111: 1.999s
0x00FF	ASICID	[15:4]	asic_id [11:0]	0101_0011_ 0101	Device ID of APE5035
		[3:0]	revision [3:0]	0000	Version of APE5035

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0100	DEL_CH0	[9:0]	del_ch_0[9:0]	00_0000_0000	Channel 0 Delay: based-on ILED Freq delay time/LSB=LED Frequency Reciprocals/1023 23.04KHz >> 1LSB= ~42.43ns 11.52KHz >> 1LSB= ~84.85ns 5.76KHz >> 1LSB= ~169.71ns 2.88KHz >> 1LSB= ~339.42ns 1.44KHz >> 1LSB= ~678.83ns 720Hz >> 1LSB= ~1357.66ns 360Hz >> 1LSB= ~2715.32ns 180Hz >> 1LSB= ~5430.65ns For example ILED Freq=23.04KHz 0x000: 0ns 0x001: 42.43ns 0x002: 84.85ns 0x003: 127.28ns 0x3FE: 43.36us 0x3FF: 43.4us
0x0101	DEL_CH1	[9:0]	del_ch_1[9:0]	00_0000_0000	Channel 1 delay
0x0102	DEL_CH2	[9:0]	del_ch_2[9:0]	00_0000_0000	Channel 2 delay
0x0103	DEL_CH3	[9:0]	del_ch_3[9:0]	00_0000_0000	Channel 3 delay
0x0104	DEL_CH4	[9:0]	del_ch_4[9:0]	00_0000_0000	Channel 4 delay
0x0105	DEL_CH5	[9:0]	del_ch_5[9:0]	00_0000_0000	Channel 5 delay
0x0106	DEL_CH6	[9:0]	del_ch_6[9:0]	00_0000_0000	Channel 6 delay
0x0107	DEL_CH7	[9:0]	del_ch_7[9:0]	00_0000_0000	Channel 7 delay
0x0108	DEL_CH8	[9:0]	del_ch_8[9:0]	00_0000_0000	Channel 8 delay
0x0109	DEL_CH9	[9:0]	del_ch_9[9:0]	00_0000_0000	Channel 9 delay
0x010A	DEL_CH10	[9:0]	del_ch_10[9:0]	00_0000_0000	Channel 10 delay
0x010B	DEL_CH11	[9:0]	del_ch_11[9:0]	00_0000_0000	Channel 11 delay
0x010C	DEL_CH12	[9:0]	del_ch_12[9:0]	00_0000_0000	Channel 12 delay
0x010D	DEL_CH13	[9:0]	del_ch_13[9:0]	00_0000_0000	Channel 13 delay
0x010E	DEL_CH14	[9:0]	del_ch_14[9:0]	00_0000_0000	Channel 14 delay
0x010F	DEL_CH15	[9:0]	del_ch_15[9:0]	00_0000_0000	Channel 15 delay
0x0110	DEL_CH16	[9:0]	del_ch_16[9:0]	00_0000_0000	Channel 16 delay
0x0111	DEL_CH17	[9:0]	del_ch_17[9:0]	00_0000_0000	Channel 17 delay
0x0112	DEL_CH18	[9:0]	del_ch_18[9:0]	00_0000_0000	Channel 18 delay
0x0113	DEL_CH19	[9:0]	del_ch_19[9:0]	00_0000_0000	Channel 19 delay
0x0114	DEL_CH20	[9:0]	del_ch_20[9:0]	00_0000_0000	Channel 20 delay
0x0115	DEL_CH21	[9:0]	del_ch_21[9:0]	00_0000_0000	Channel 21 delay
0x0116	DEL_CH22	[9:0]	del_ch_22[9:0]	00_0000_0000	Channel 22 delay
0x0117	DEL_CH23	[9:0]	del_ch_23[9:0]	00_0000_0000	Channel 23 delay
0x0118	DEL_CH24	[9:0]	del_ch_24[9:0]	00_0000_0000	Channel 24 delay
0x0119	DEL_CH25	[9:0]	del_ch_25[9:0]	00_0000_0000	Channel 25 delay

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x011A	DEL_CH26	[9:0]	del_ch_26[9:0]	00_0000_0000	Channel 26 delay
0x011B	DEL_CH27	[9:0]	del_ch_27[9:0]	00_0000_0000	Channel 27 delay
0x011C	DEL_CH28	[9:0]	del_ch_28[9:0]	00_0000_0000	Channel 28 delay
0x011D	DEL_CH29	[9:0]	del_ch_29[9:0]	00_0000_0000	Channel 29 delay
0x011E	DEL_CH30	[9:0]	del_ch_30[9:0]	00_0000_0000	Channel 30 delay
0x011F	DEL_CH31	[9:0]	del_ch_31[9:0]	00_0000_0000	Channel 31 delay
0x0120	DEL_CH32	[9:0]	del_ch_32[9:0]	00_0000_0000	Channel 32 delay
0x0121	DEL_CH33	[9:0]	del_ch_33[9:0]	00_0000_0000	Channel 33 delay
0x0122	DEL_CH34	[9:0]	del_ch_34[9:0]	00_0000_0000	Channel 34 delay
0x0123	DEL_CH35	[9:0]	del_ch_35[9:0]	00_0000_0000	Channel 35 delay
0x0124	DEL_CH36	[9:0]	del_ch_36[9:0]	00_0000_0000	Channel 36 delay
0x0125	DEL_CH37	[9:0]	del_ch_37[9:0]	00_0000_0000	Channel 37 delay
0x0126	DEL_CH38	[9:0]	del_ch_38[9:0]	00_0000_0000	Channel 38 delay
0x0127	DEL_CH39	[9:0]	del_ch_39[9:0]	00_0000_0000	Channel 39 delay
0x0128	DEL_CH40	[9:0]	del_ch_40[9:0]	00_0000_0000	Channel 40 delay
0x0129	DEL_CH41	[9:0]	del_ch_41[9:0]	00_0000_0000	Channel 41 delay
0x012A	DEL_CH42	[9:0]	del_ch_42[9:0]	00_0000_0000	Channel 42 delay
0x012B	DEL_CH43	[9:0]	del_ch_43[9:0]	00_0000_0000	Channel 43 delay
0x012C	DEL_CH44	[9:0]	del_ch_44[9:0]	00_0000_0000	Channel 44 delay
0x012D	DEL_CH45	[9:0]	del_ch_45[9:0]	00_0000_0000	Channel 45 delay
0x012E	DEL_CH46	[9:0]	del_ch_46[9:0]	00_0000_0000	Channel 46 delay
0x012F	DEL_CH47	[9:0]	del_ch_47[9:0]	00_0000_0000	Channel 47 delay
0x0130	DEL_CH48	[9:0]	del_ch_48[9:0]	00_0000_0000	Channel 48 delay
0x0131	DEL_CH49	[9:0]	del_ch_49[9:0]	00_0000_0000	Channel 49 delay
0x0132	DEL_CH50	[9:0]	del_ch_50[9:0]	00_0000_0000	Channel 50 delay
0x0133	DEL_CH51	[9:0]	del_ch_51[9:0]	00_0000_0000	Channel 51 delay
0x0134	DEL_CH52	[9:0]	del_ch_52[9:0]	00_0000_0000	Channel 52 delay
0x0135	DEL_CH53	[9:0]	del_ch_53[9:0]	00_0000_0000	Channel 53 delay
0x0136	DEL_CH54	[9:0]	del_ch_54[9:0]	00_0000_0000	Channel 54 delay
0x0137	DEL_CH55	[9:0]	del_ch_55[9:0]	00_0000_0000	Channel 55 delay
0x0138	DEL_CH56	[9:0]	del_ch_56[9:0]	00_0000_0000	Channel 56 delay
0x0139	DEL_CH57	[9:0]	del_ch_57[9:0]	00_0000_0000	Channel 57 delay
0x013A	DEL_CH58	[9:0]	del_ch_58[9:0]	00_0000_0000	Channel 58 delay
0x013B	DEL_CH59	[9:0]	del_ch_59[9:0]	00_0000_0000	Channel 59 delay
0x013C	DEL_CH60	[9:0]	del_ch_60[9:0]	00_0000_0000	Channel 60 delay
0x013D	DEL_CH61	[9:0]	del_ch_61[9:0]	00_0000_0000	Channel 61 delay
0x013E	DEL_CH62	[9:0]	del_ch_62[9:0]	00_0000_0000	Channel 62 delay
0x013F	DEL_CH63	[9:0]	del_ch_63[9:0]	00_0000_0000	Channel 63 delay

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0140	DEL_CH64	[9:0]	del_ch_64[9:0]	00_0000_0000	Channel 64 delay
0x0141	DEL_CH65	[9:0]	del_ch_65[9:0]	00_0000_0000	Channel 65 delay
0x0142	DEL_CH66	[9:0]	del_ch_66[9:0]	00_0000_0000	Channel 66 delay
0x0143	DEL_CH67	[9:0]	del_ch_67[9:0]	00_0000_0000	Channel 67 delay
0x0144	DEL_CH68	[9:0]	del_ch_68[9:0]	00_0000_0000	Channel 68 delay
0x0145	DEL_CH69	[9:0]	del_ch_69[9:0]	00_0000_0000	Channel 69 delay
0x0146	DEL_CH70	[9:0]	del_ch_70[9:0]	00_0000_0000	Channel 70 delay
0x0147	DEL_CH71	[9:0]	del_ch_71[9:0]	00_0000_0000	Channel 71 delay
0x0148	DEL_CH72	[9:0]	del_ch_72[9:0]	00_0000_0000	Channel 72 delay
0x0149	DEL_CH73	[9:0]	del_ch_73[9:0]	00_0000_0000	Channel 73 delay
0x014A	DEL_CH74	[9:0]	del_ch_74[9:0]	00_0000_0000	Channel 74 delay
0x014B	DEL_CH75	[9:0]	del_ch_75[9:0]	00_0000_0000	Channel 75 delay
0x014C	DEL_CH76	[9:0]	del_ch_76[9:0]	00_0000_0000	Channel 76 delay
0x014D	DEL_CH77	[9:0]	del_ch_77[9:0]	00_0000_0000	Channel 77 delay
0x014E	DEL_CH78	[9:0]	del_ch_78[9:0]	00_0000_0000	Channel 78 delay
0x014F	DEL_CH79	[9:0]	del_ch_79[9:0]	00_0000_0000	Channel 79 delay
0x0150	DEL_CH80	[9:0]	del_ch_80[9:0]	00_0000_0000	Channel 80 delay
0x0151	DEL_CH81	[9:0]	del_ch_81[9:0]	00_0000_0000	Channel 81 delay
0x0152	DEL_CH82	[9:0]	del_ch_82[9:0]	00_0000_0000	Channel 82 delay
0x0153	DEL_CH83	[9:0]	del_ch_83[9:0]	00_0000_0000	Channel 83 delay
0x0154	DEL_CH84	[9:0]	del_ch_84[9:0]	00_0000_0000	Channel 84 delay
0x0155	DEL_CH85	[9:0]	del_ch_85[9:0]	00_0000_0000	Channel 85 delay
0x0156	DEL_CH86	[9:0]	del_ch_86[9:0]	00_0000_0000	Channel 86 delay
0x0157	DEL_CH87	[9:0]	del_ch_87[9:0]	00_0000_0000	Channel 87 delay
0x0158	DEL_CH88	[9:0]	del_ch_88[9:0]	00_0000_0000	Channel 88 delay
0x0159	DEL_CH89	[9:0]	del_ch_89[9:0]	00_0000_0000	Channel 89 delay
0x015A	DEL_CH90	[9:0]	del_ch_90[9:0]	00_0000_0000	Channel 90 delay
0x015B	DEL_CH91	[9:0]	del_ch_91[9:0]	00_0000_0000	Channel 91 delay
0x015C	DEL_CH92	[9:0]	del_ch_92[9:0]	00_0000_0000	Channel 92 delay
0x015D	DEL_CH93	[9:0]	del_ch_93[9:0]	00_0000_0000	Channel 93 delay
0x015E	DEL_CH94	[9:0]	del_ch_94[9:0]	00_0000_0000	Channel 94 delay
0x015F	DEL_CH95	[9:0]	del_ch_95[9:0]	00_0000_0000	Channel 95 delay

SPI Interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in a “Daisy Chain” structure or a parallel structure.

SPI Daisy Chain Structure

All SPI slaves share the same clock (SCL) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.
The APE5035 SDO pin was output 3.3V, If the pin will be connecting to host, it must note whether the host I/O can withstand 3.3V.
Setting the SDO I/O type as Open-Drain, then SDO output HIGH was decide by external VIN through a pull-up resister. (As the following block diagram, VDDIO as the external VIN, and R_{SDO_PU} as the pull-up resister).

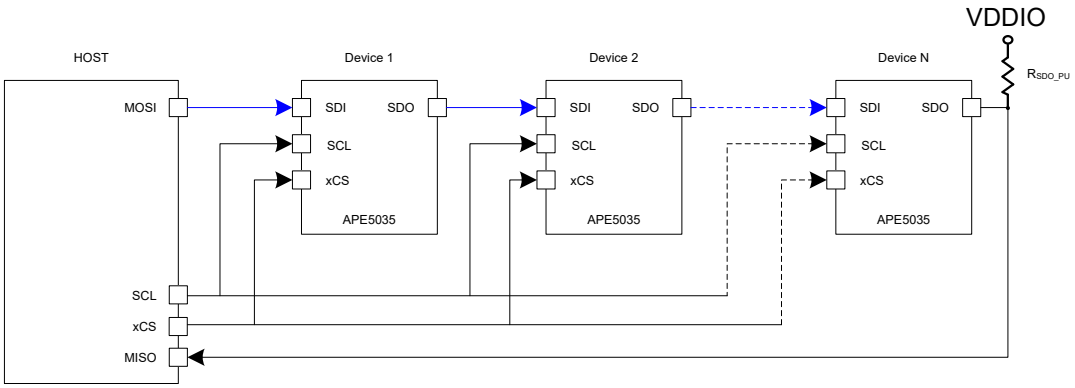


Figure 7: SPI Daisy Chain structure

SPI Parallel Structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCL) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has the “DevAddr=0x0001”. When SPI parallel structure was used then all device SDO pin must choose the open drain type.

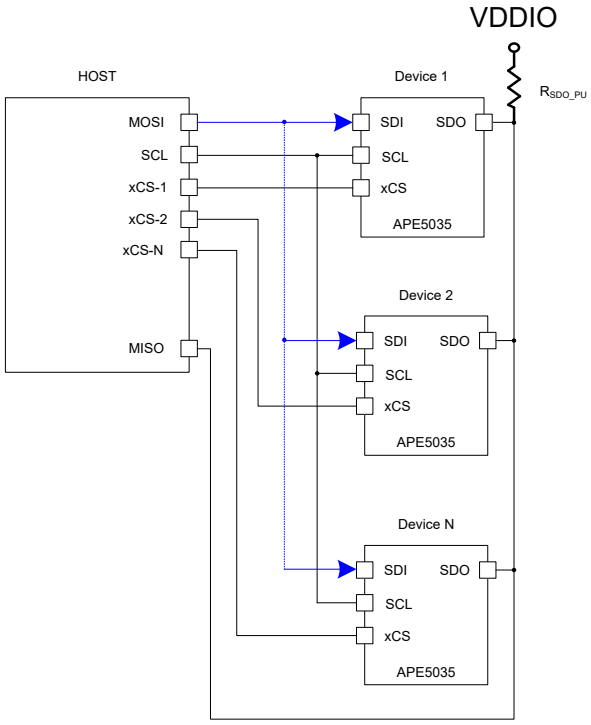


Figure 8: SPI Parallel Structure

SPI Device Address Enumeration

The device address of each driver is automatically set by the position of the device in the chain. The first device has DevAddr=0x0001, the second device has DevAddr=0x0002 and so on. Device Addresses (0x00 and 0x7F) are used for special broadcast writing commands described below.

SPI Protocol

The SPI transmission protocol of APE5035 is mainly composed of several bytes: Command, Register Address and Data. Which is organized in words (16 bit) packages. Each message can be built with the following words:

Command:

[15]	[14:8]	[7:0]
Sr	DevAddr	Nr_of_data

Bit	Meaning	Value and Description
[15]	Start bit	Must be 1
[14:8]	Device Address	Addresses a specific driver and defines protocol information 0x00: Broadcast transfer command, write same data to all devices 0x01 to 0x7E: Single device transfer command, Indicate which device to write/read 0x7F: Broadcast transfer command, write different data to all devices
[7:0]	Single byte	Write command: 0x01~0xFF Read command: 0x01~0xFF

Register_address:

[15]	[14:12]	[11:0]
R/W	Reserved	RegAddr

Bit	Meaning	Value and Description
[15]	Read/Write	0: write to register address 1: read from register address
[14:12]	Reserved	Reserved
[11:0]	Select register address	Address from 0x000 to 0xFFF

Data:

[15:0]
Data

The data to be transferred

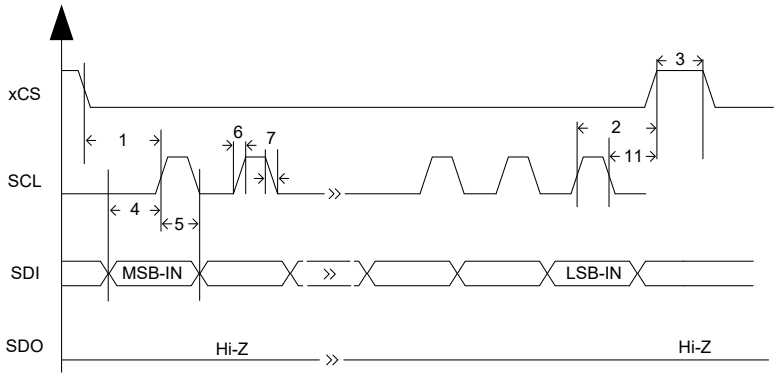
Bit	Meaning	Value and Description
[15:0]	Data	0x0000 to 0xFFFF

Time Characteristics

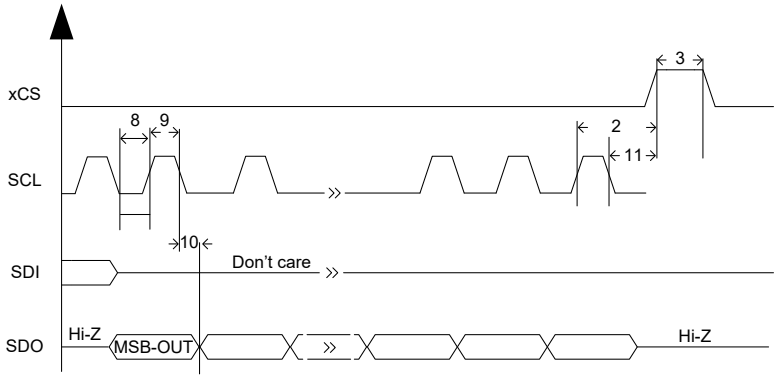
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLK}	SCL frequency	0	-	26	MHz
t1	xCS setup time	10	-	-	ns
t2	xCS hold time	10	-	-	ns
t3	xCS disable time	200	-	-	ns
t4	SDI setup time	10	-	-	ns
t5	SDI hold time	10	-	-	ns
t6	SCL rise time	-	-	10	ns
t7	SCL falling time	-	-	10	ns
t8	SCL low time	15	-	-	ns
t9	SCL high time	15	-	-	ns
t10	Output valid from SCL low	-	-	10	ns
t11	SCL falling to xCS rising edge	5	-	-	ns

Timing Characteristics: Shows the timing characteristics of the SPI Interface

SPI Input Timing

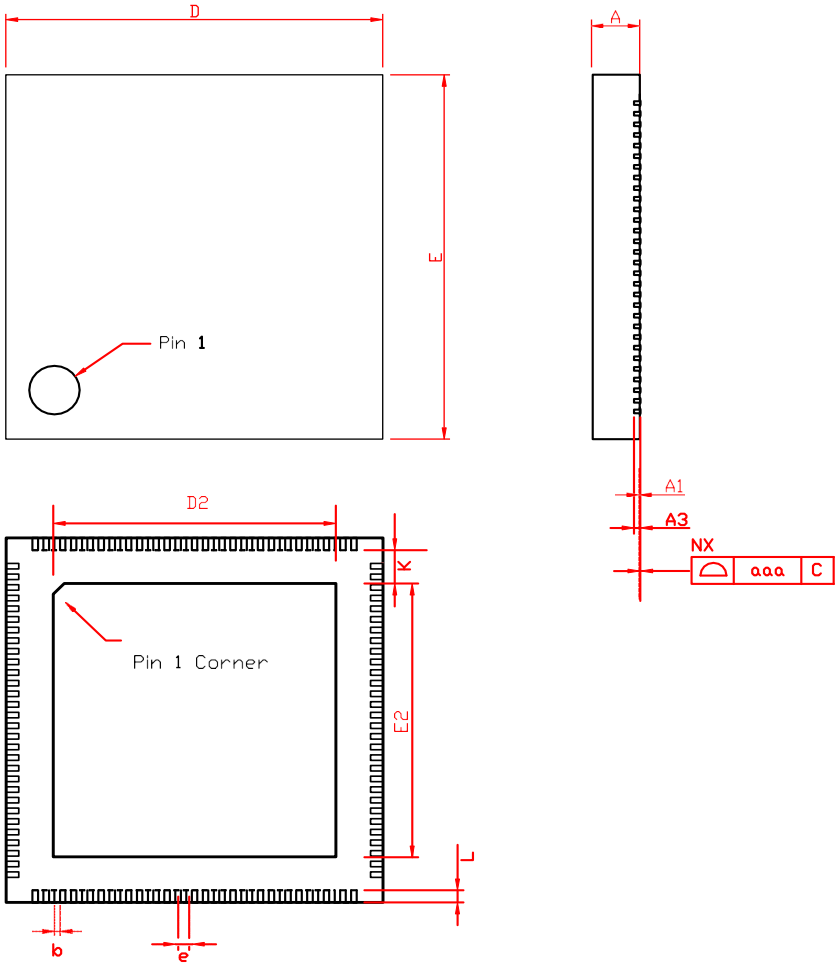


SPI Output Timing



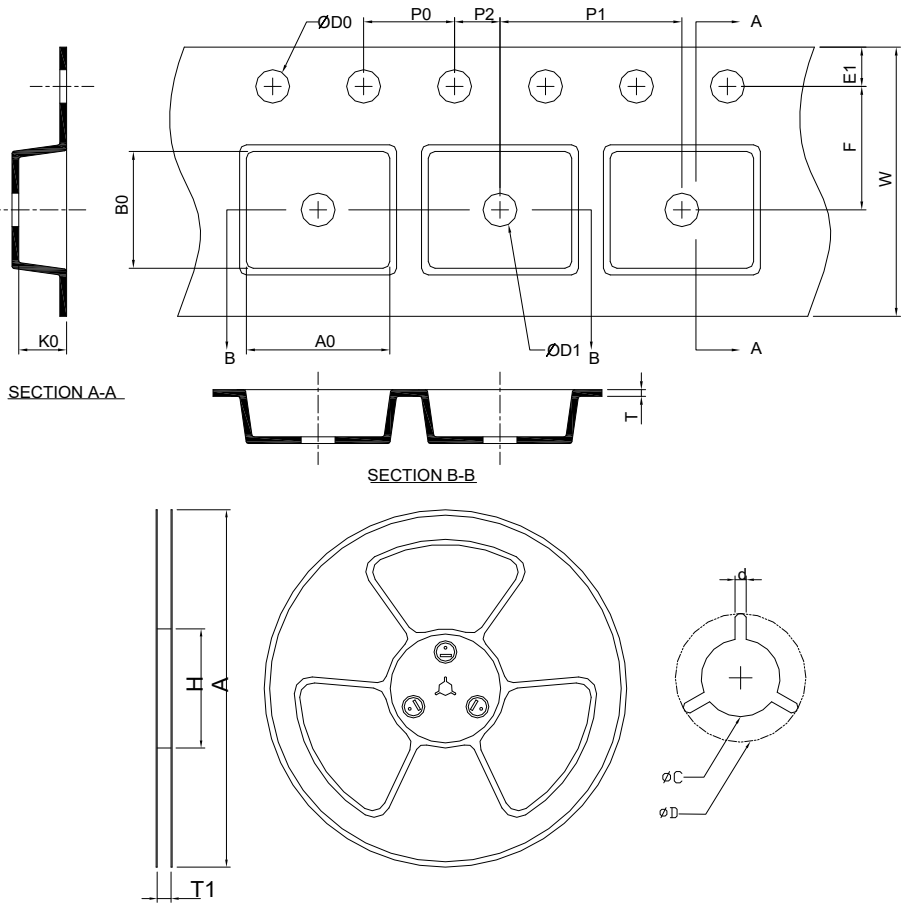
Package Information

QFN 12x12-120



SYMBOL	QFN12x12-120			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.13	0.23	0.005	0.009
D	11.90	12.10	0.469	0.476
D2	8.90	9.10	0.350	0.358
E	11.90	12.10	0.469	0.476
E2	8.90	9.10	0.350	0.358
e	0.35 BSC		0.014 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN 12x12	330.0±2.00	50 MIN.	24.8+2.00 -0.50	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	24.0±0.30	1.75±0.10	11.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	16.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.3+0.05 -0.05	12.30±0.10	12.30±0.10	0.95±0.10

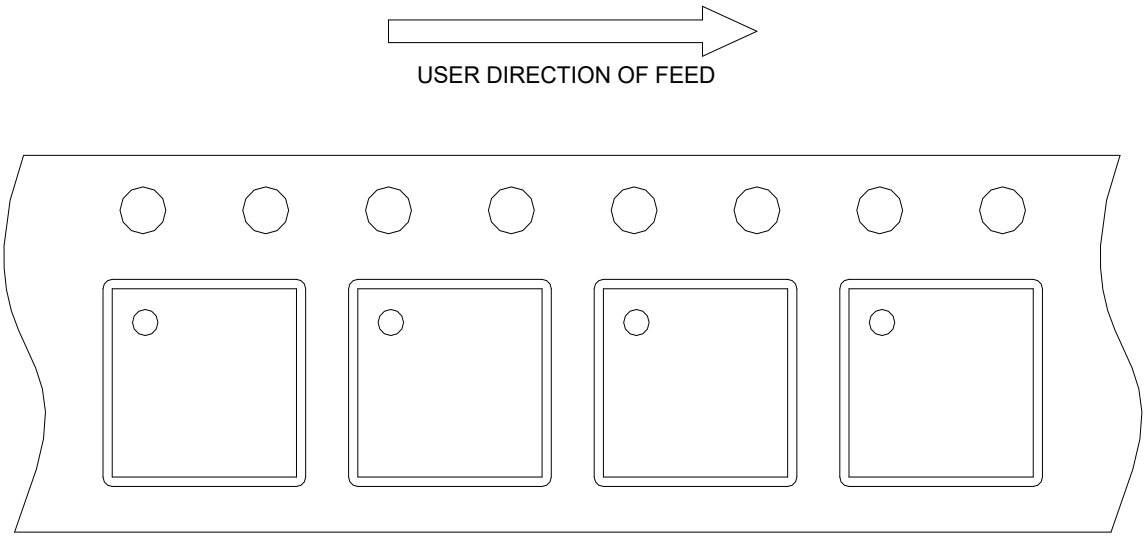
(mm)

Devices Per Unit

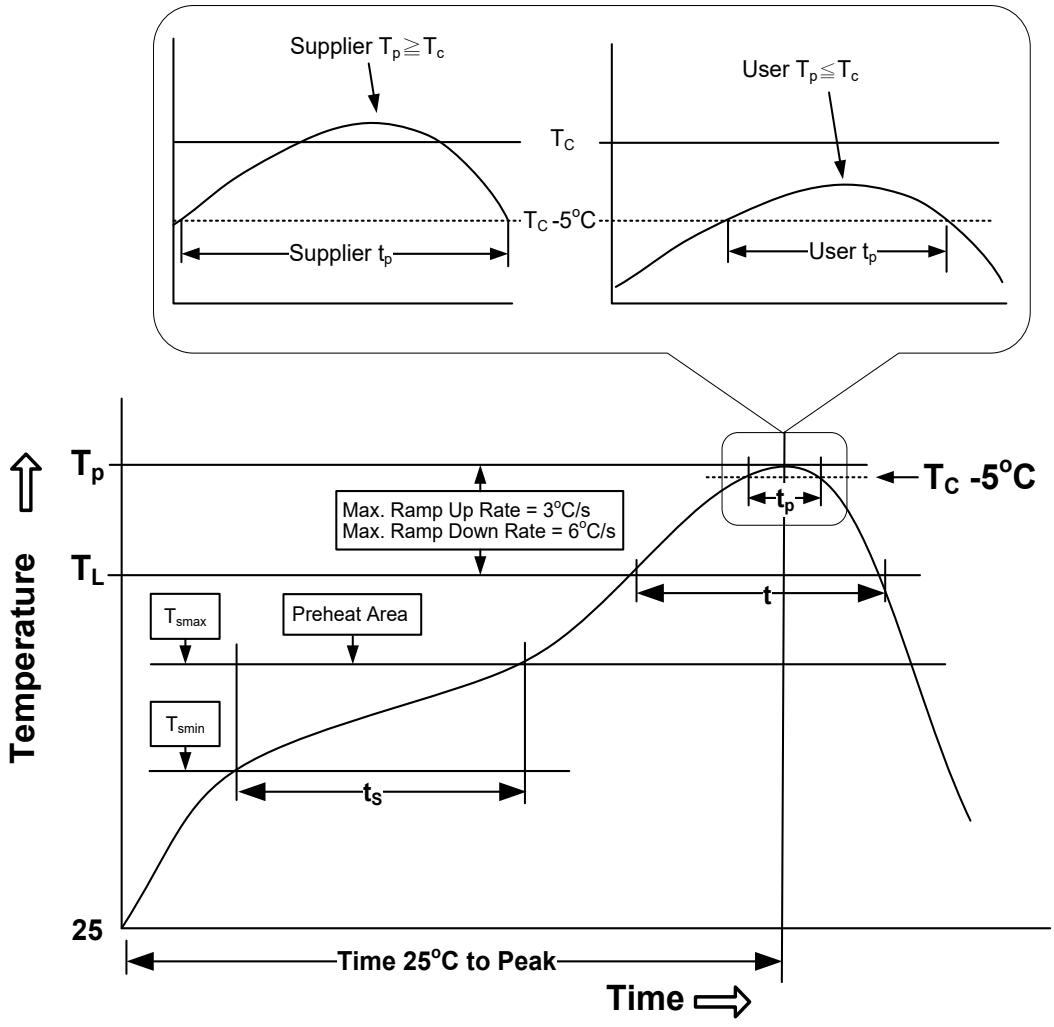
Package type	Packing	Quantity
QFN 12x12	Tape & Reel	2000

Taping Direction Information

QFN 12x12-120



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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