APE5039

40 Channel White LED Controller for LED Backlight

Features

- **Wide range input is 4.5V to 26V**
- **High Accurate LED Current 2% Typ. (ILED=60mA)**
- **LED current modulation method: PWM and DC mode**
- **40 Channel flexible PWM generators and independent for 13 Bits PWM Brightness**
- **Synchronization with TV Frame – VSYNC / Digital PLL Integrated**
- **Digital Configurable DC / DC Feedback**
- **Protection For Safety Features**
  - **- LED Short Detection**
  - **- LED Open Detection**
  - **- Temperature Shutdown detection**
  - **- UVLO**
- **PWM and DC Dimming Via SPI Interface (16 bit protocol)**
- **HDR mode for LED current modulation**
- **Available In QFN 9x9-76 Package**
- **One global / local high accurate 10 big DAC which sets the LED current**

Applications

- **Televisions**
- **Monitors**

General Description

The APE5039 are integrates Mosfet and 40 channel LED controller for LED backlight. It's high accurate LED current 2% (60mA LED current) and wide input voltage range.

The APE5039 has 40 Channel flexible PWM generators and independent 13 bits PWM brightness were control LED current for every channel. In addition; It's has one global/local high accurate 10 bit DAC which sets the LED current. It's synchronization with TV Frame including VSYNC and Digital PLL method.

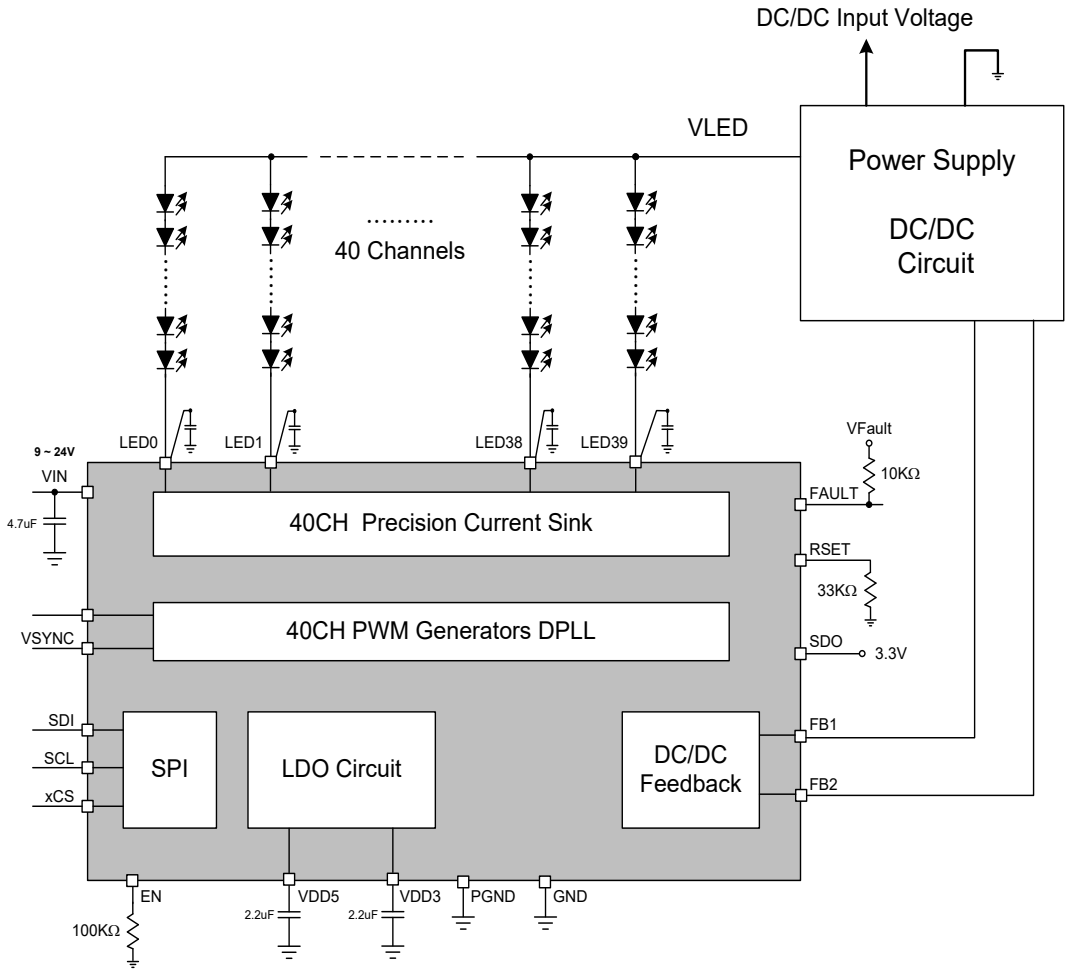
The APE5039 own LED current modulation method including PWM mode and DC mode. When applications have flicker frequency issue and then can using the DC mode method eliminate flicker frequency problem.

The APE5039 has two pins can be digital configurable DC/DC feedback, that's for control DC/DC architecture. As the same time; the device using programmable via SPI interface.

The APE5039 owns HDR mode for modulation LED current. It's build-in protection for safety; include LED short, LED Open, temperature shutdown protection and UVLO.

The APE5039 is available in QFN 9x9-76 packages.

Simplified Application Circuit

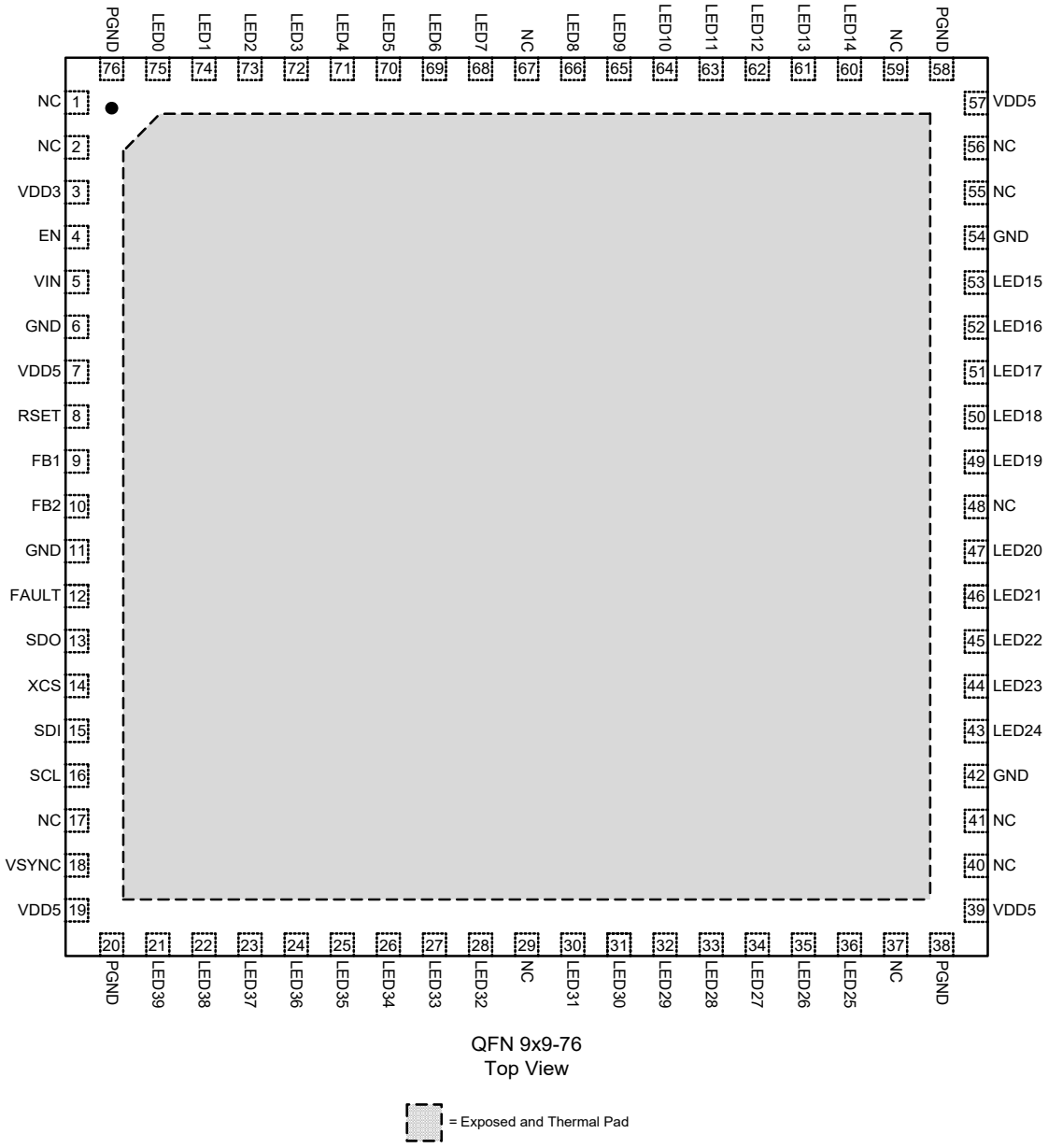


Ordering and Marking Information

APE5039 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN 9x9-76 Operating Ambient Temperature Range I : -40 to 85 ℃ Handling Code TR : Tape & Reel Assembly Material G : Green Part
APE5039 QA :  	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configurations



QFN 9x9-76
Top View

= Exposed and Thermal Pad

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 28	V
V_{ANALOG}	LED0 ~ LED39 to PGND	-0.3 ~ 50	V
	EN to PGND	-0.3 ~ 28	V
	VSYNC, FB1, FB2 and RSET to GND	-0.3 ~ 7	V
$V_{DIGITAL}$	VDD5, SDI, SCL, FAULT and XCS to GND	-0.3 ~ 7	V
	VDD3 and SDO to GND	-0.3 ~ 5	V
V_{GND}	GND to PGND	-0.3 ~ 0.3	V
T_J	Junction Temperature	180	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	25	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Input Supply Voltage	4.5 ~ 26	V
V_{LEDn}	LED String Voltage	~ 45	V
I_{LED}	LED Current	10 ~ 145	mA
C_{IN}	Converter Input Capacitor (MLCC)	4.7 ~	µF
C_{VDD_5}	VDD5 Output Capacitor (MLCC)	2.2 ~	µF
C_{VDD_3}	VDD3 Output Capacitor (MLCC)	2.2 ~	µF
R_{SET}	External Setting LED Current Resistor	33 ± 1%	KΩ
T_A	Ambient Temperature	-20 ~ 85	°C
T_J	Junction Temperature	-20 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, EN=3.3V, VSYNC=60Hz and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APE5039			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage Range		9	-	24	V
		VIN shorted to VDD5	4.5	5	5.5	V
V_{LDO_5}	5V LDO Voltage Regulation Output	IDAC Code setting to max, VIN=12V, EN=High	4.5	5	5.5	V
V_{LDO_3}	3.3V LDO Voltage Regulation Output	I_{LOAD}=20mA, VIN=12V, EN=High	3	3.3	3.6	V
V_{IN-POR}	VIN Power On Reset Level	EN=High, VIN Rising	3.4	3.9	4.4	V
$V_{IN\_POR\_HYS}$	POR Hysteresis	EN=High, VIN Falling	-	0.3	-	V
	Power On Delay Time	Waiting to Command Time (VIN >=4.5V and EN=high are already)	-	50	-	mS
I_Q	Quiescent Current	VIN=12V, IDAC is max, duty=50%, EN=high (Normal operation)	-	-	80	mA
	Shutdown Current	EN= Low (Shutdown)	-	-	100	μA
$I_{LED\_145\_10}$	LED Current Accuracy	ILED=9.375mA, REG_Code[9:0]=66, 25°C (Note: It's not include RSET)	9.1875	9.375	9.5625	mA
$I_{LED\_145\_60}$	LED Current Accuracy	ILED=59.94318mA, REG_Code[9:0]=422, 25°C (Note: It's not include RSET)	58.7443	59.94318	61.142	mA
$I_{LED\_145\_145}$	LED Current Accuracy	ILED=145.3125mA, REG_Code[9:0]=1023, 25°C (Note: It's not include RSET)	142.4062	145.3125	148.2187	mA
$I_{LED\_145\_10}$	Led Current Accuracy To All Temperature	ILED=9.375mA, REG_Code[9:0]=66, -25 ~ 85°C (Note: It's not included RSET)	-3	-	3	%
$I_{LED\_145\_145}$		ILED=145.3125mA, REG_Code[9:0]=1023, -25 ~ 85°C (Note: It's not included RSET)	-3	-	3	%
I_{LED_CH}	Channel To Channel Current Matching	ILED=9.375mA, REG_Code[9:0]=66, 25°C (Note: It's not included RSET)	-2	-	2	%
		ILED=145.3125mA, REG_Code[9:0]=1023, 25°C (Note: It's not included RSET)	-2	-	2	%
I_{FB_MAX}	Feedback Current Maximum	VFB_X > 0.25V, T_A=25°C	251	255	270	μA
FB_{IDAC_LSB}	Fb_dac_lsb		-	0.125	-	μA
T_{OTP}	Over-Temperature	Temperature rising	150	165	180	°C
T_{OTP_HYS}	Temperature Hysteresis		-	20	-	°C
T_{SHORT_MIN}	Minimum Pwm On Time To Detect Shorted Leds		-	3	-	μS

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V, EN=3.3V, VSYNC=60Hz and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APE5039			Unit
			Min.	Typ.	Max.	
F_{OSC}	Internal Clock	For OSC	22.413	23.592	24.772	MHz
F_{VSYNC}	VSYNC Frequency (No VRR Mode)	For DPLL	48.5	50	51.5	Hz
			58.2	60	61.8	Hz
			116.4	120	123.6	Hz
			139.68	144	148.32	Hz
			160.05	165	169.95	Hz
			232.8	240	247.2	Hz
			465.6	480	494.4	Hz
			931.2	960	988.8	Hz
	VSYNC Frequency (VRR Mode): OSC	For internal OSC: 1Hz (resolution)	40	-	240	Hz
F_{PWM}	LED output Frequency (No VRR mode)	180Hz to 23.04KHz (For Register select and based-on VSYNC signal)	0.18	-	23.04	KHz
			20.736	23.04	25.344	KHz
V_{IH}	High Level Input Voltage	Input PIN (VSYNC, XCS, SCL, SDI, EN)	1.7	-	VDD5+0.3	V
V_{IL}	Low Level Input Voltage	Input PIN (VSYNC, XCS, SCL, SDI, EN)	-0.3	-	0.7	V
V_{OH}	High Level Output Voltage	Output PIN (SDO), I=2mA	VDD3-0.3	-	-	V
V_{OL}	Low Level Output Voltage	Output PIN (SDO), I=2mA	-	-	0.3	V
V_{OL_PD}	Low Level Output Voltage Open Drain Outputs	Output PIN (FAULT), I=2mA	-	-	0.3	V
R_{PU}	Input Resistance Pull-Up	VIN =12V, EN=3.3V, XCS=GND	-	300	-	KΩ
R_{PD}	Input Resistance Pull-Down	VIN =12V, VSYNC, SCL, SDI=5V	-	300	-	KΩ
I_{LEK}	Leakage Current	VIN =12V, EN=3.3V For FAULT, FB1, FB2=5V, SDO=3.3V	-	-	1	μA
I_{LEDX_LEK}	Leakage Current For Ledx	VIN=12V, EN=3.3V, V_{LEDx}=45V	-	-	1	μA
I_{SPI_CLK}	SPI Clock Frequency		-	-	26	MHz
I_{EN}	EN Input Current	VIN=26V, EN=26V	-	-	30	μA
I_{BIAS}	LED Auto Bias Current	VIN=12V, EN=3.3V, current on, brightness off, RSET=33K	-	-	1	μA

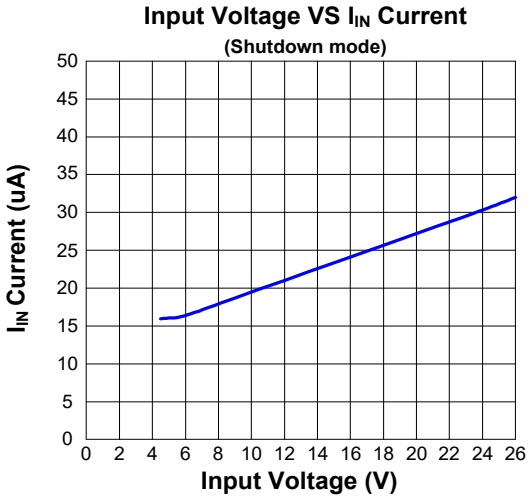
Pin Description

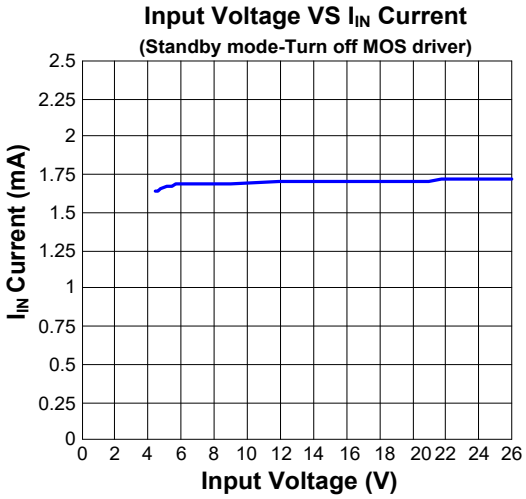
PIN		FUNCTION
NO.	NAME	
1, 2, 17, 29, 37, 40, 41, 48, 55, 56, 59, 67	NC	No Connection.
3	VDD3	Internal 3.3V LDO Regulation. Connect 2.2uF capacitor to GND.
7, 19, 39, 57	VDD5	Internal 5V LDO Regulation. Connect 2.2uF capacitor to GND.
4	EN	Enable control input. Forcing this pin above 1.7V enables the device or forcing this pin below 0.7V to shut it down. In shutdown, all function is disabled to decrease the supply current below 100uA. This pin is not floating (suggestion connector to 100K to ground).
5	VIN	Input Supply Voltage.
6, 11, 42, 54	GND	Analog Ground.
8	RSET	External Setting Iset Current Resistor, RSET to GND connection 33K. (±0.5%)
9	FB1	DC/DC Power supply feedback output 1.
10	FB2	DC/DC Power supply feedback output 2.
12	FAULT	Open drain fault output.
13	SDO	SPI interface data output. Tristate output.
14	xCS	SPI interface chip selects.
15	SDI	SPI interface data input.
16	SCL	SPI interface clock.
18	VSYNC	Clock input for PWM generators.
20, 38, 58, 76	PGND	Power Ground For LED Current Return Path.
21	LED39	LED Cathode Connection For LED String39.
22	LED38	LED Cathode Connection For LED String38.
23	LED37	LED Cathode Connection For LED String37.
24	LED36	LED Cathode Connection For LED String36.
25	LED35	LED Cathode Connection For LED String35.
26	LED34	LED Cathode Connection For LED String34.
27	LED33	LED Cathode Connection For LED String33.
28	LED32	LED Cathode Connection For LED String32.
30	LED31	LED Cathode Connection For LED String31.
31	LED30	LED Cathode Connection For LED String30.
32	LED29	LED Cathode Connection For LED String29.
33	LED28	LED Cathode Connection For LED String28.
34	LED27	LED Cathode Connection For LED String27.
35	LED26	LED Cathode Connection For LED String26.
36	LED25	LED Cathode Connection For LED String25.
43	LED24	LED Cathode Connection For LED String24.
44	LED23	LED Cathode Connection For LED String23.
45	LED22	LED Cathode Connection For LED String22.
46	LED21	LED Cathode Connection For LED String21.
47	LED20	LED Cathode Connection For LED String20.
49	LED19	LED Cathode Connection For LED String19.
50	LED18	LED Cathode Connection For LED String18.

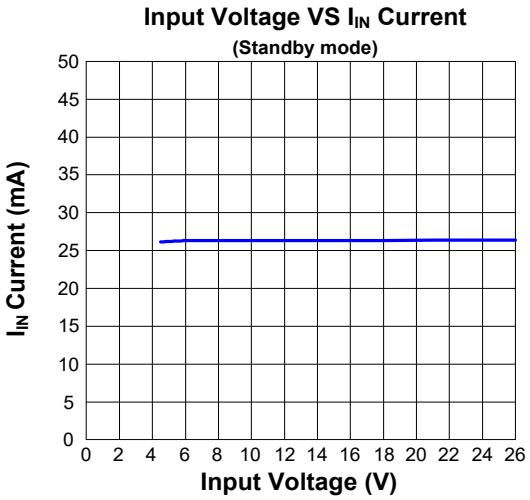
Pin Description (Cont.)

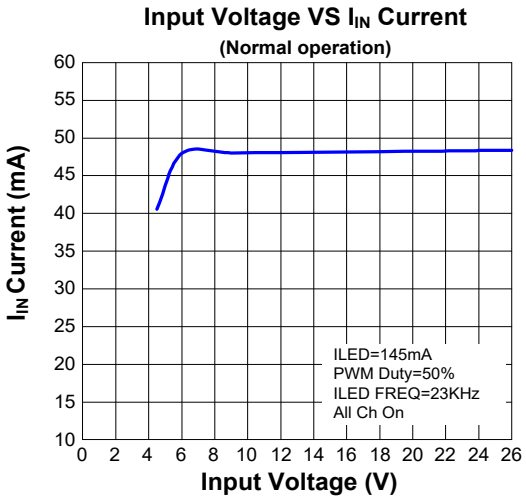
PIN		FUNCTION
NO.	NAME	
51	LED17	LED Cathode Connection For LED String17.
52	LED16	LED Cathode Connection For LED String16.
53	LED15	LED Cathode Connection For LED String15.
60	LED14	LED Cathode Connection For LED String14.
61	LED13	LED Cathode Connection For LED String13.
62	LED12	LED Cathode Connection For LED String12.
63	LED11	LED Cathode Connection For LED String11.
64	LED10	LED Cathode Connection For LED String10.
98	LED9	LED Cathode Connection For LED String9.
66	LED8	LED Cathode Connection For LED String8.
68	LED7	LED Cathode Connection For LED String7.
69	LED6	LED Cathode Connection For LED String6.
70	LED5	LED Cathode Connection For LED String5.
71	LED4	LED Cathode Connection For LED String4.
72	LED3	LED Cathode Connection For LED String3.
73	LED2	LED Cathode Connection For LED String2.
74	LED1	LED Cathode Connection For LED String1.
75	LED0	LED Cathode Connection For LED String0.
-	-	Exposed.

Typical Operating Characteristics







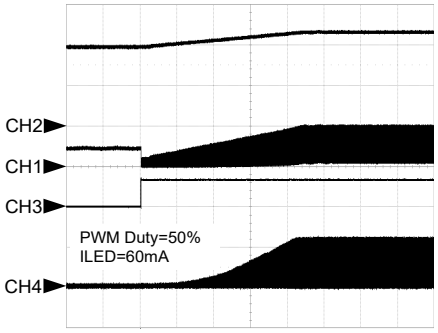


Operating Waveforms

Normal Operation

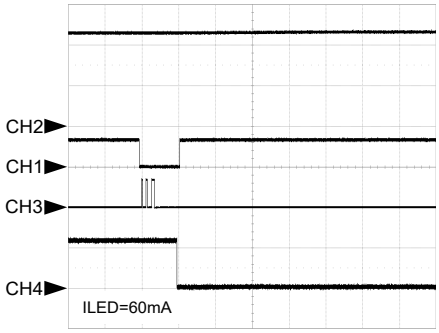
CH1: -
CH2: LEDx V_{Drain} - 200mV/div
CH3: -
CH4: I_{LEDx} - 20mA/div
Time: 20us/div

Start up - Current on enable



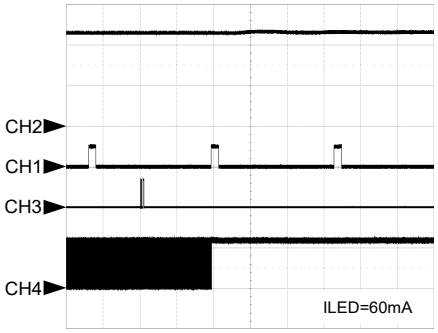
CH1: V_{drain} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: V_{SDI} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 20ms/div

Update Mode (xCS)
PWM duty 100% to 0%



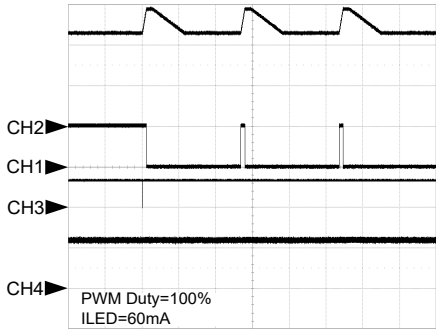
CH1: V_{xCS} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: V_{SDI} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 500us/div

Update Mode (Vsync)
PWM duty 50% to 100%



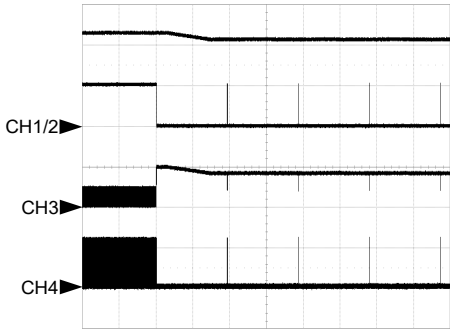
CH1: V_{VSYNC} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: V_{SDI} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 5ms/div

Open LED - Retrial



CH1: V_{xFAULT} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: V_{xCS} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 1s/div

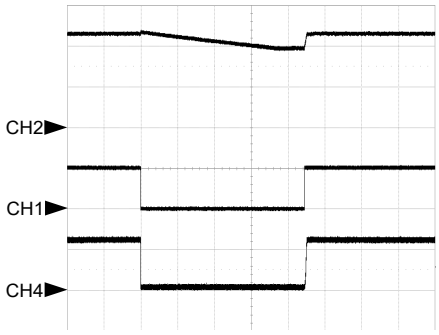
Short LED - Retrial



CH1: V_{xFAULT} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: V_{drainx} - 10V/div
CH4: I_{LEDx} - 50mA/div
Time: 200ms/div

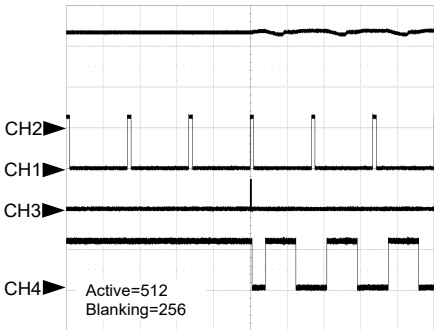
Operating Waveforms (Cont.)

OTW



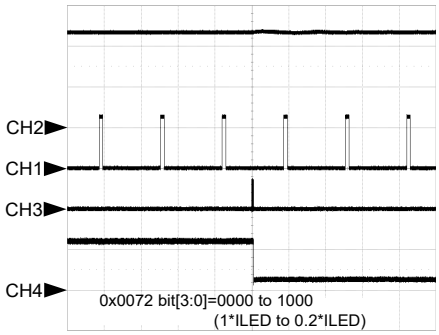
CH1: V_{xFAULT} - 5V/div
CH2: V_{OUT} - 10V/div
CH3: -
CH4: I_{LEDx} - 50mA/div
Time: 1s/div

MPRT
Disable to enable



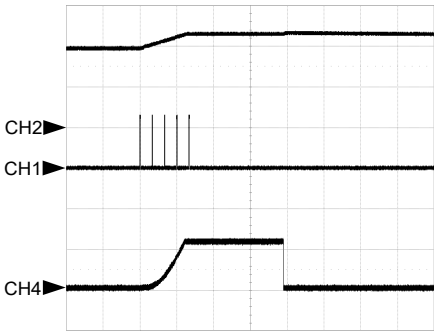
CH1: V_{VSYNC} - 2V/div
CH2: V_{OUT} - 10V/div
CH3: V_{SDI} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 10ms/div

HDR (Software Control)



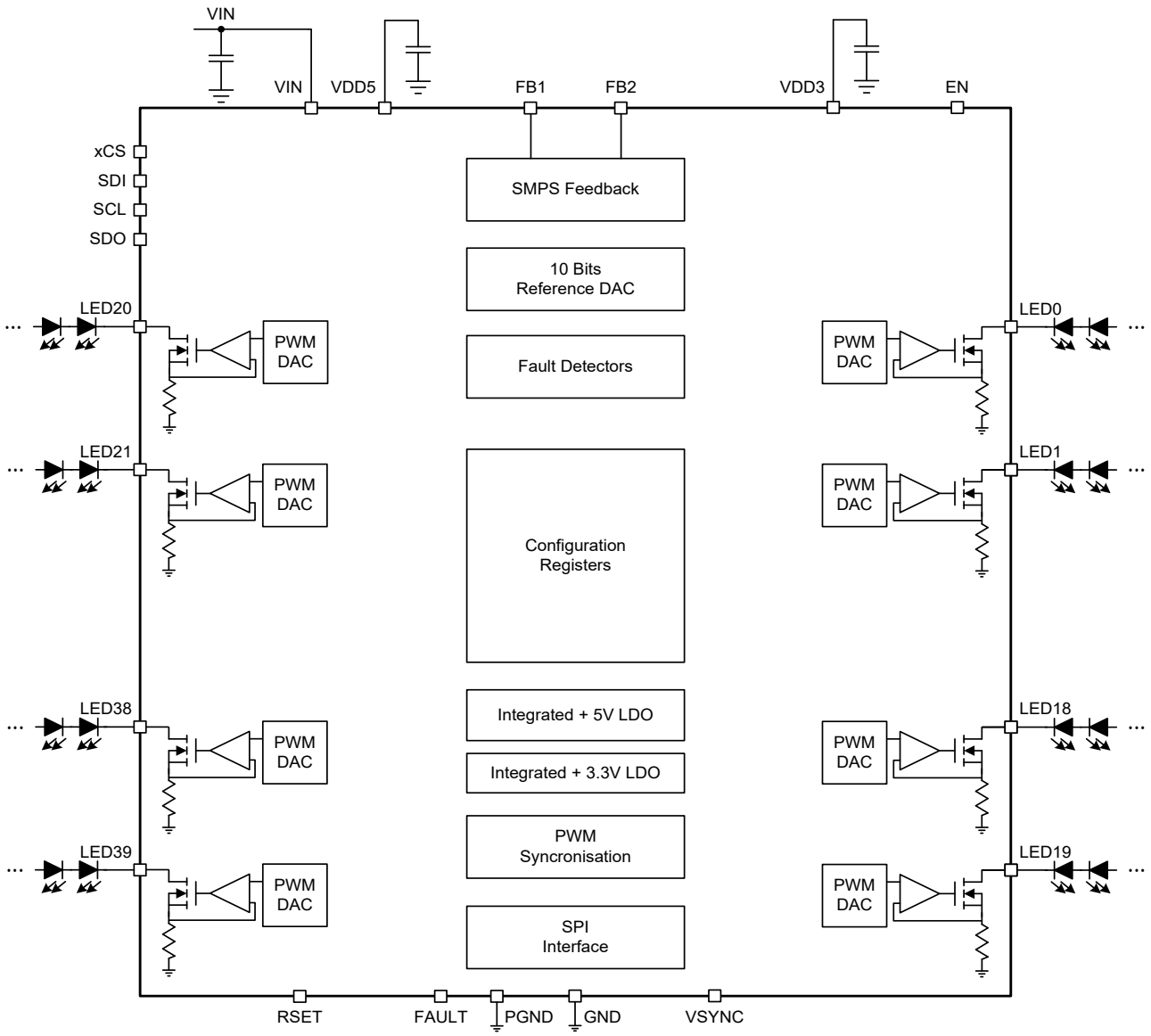
CH1: V_{VSYNC} - 2V/div
CH2: V_{OUT} - 10V/div
CH3: V_{SDI} - 5V/div
CH4: I_{LEDx} - 50mA/div
Time: 10ms/div

VSYNC Detection

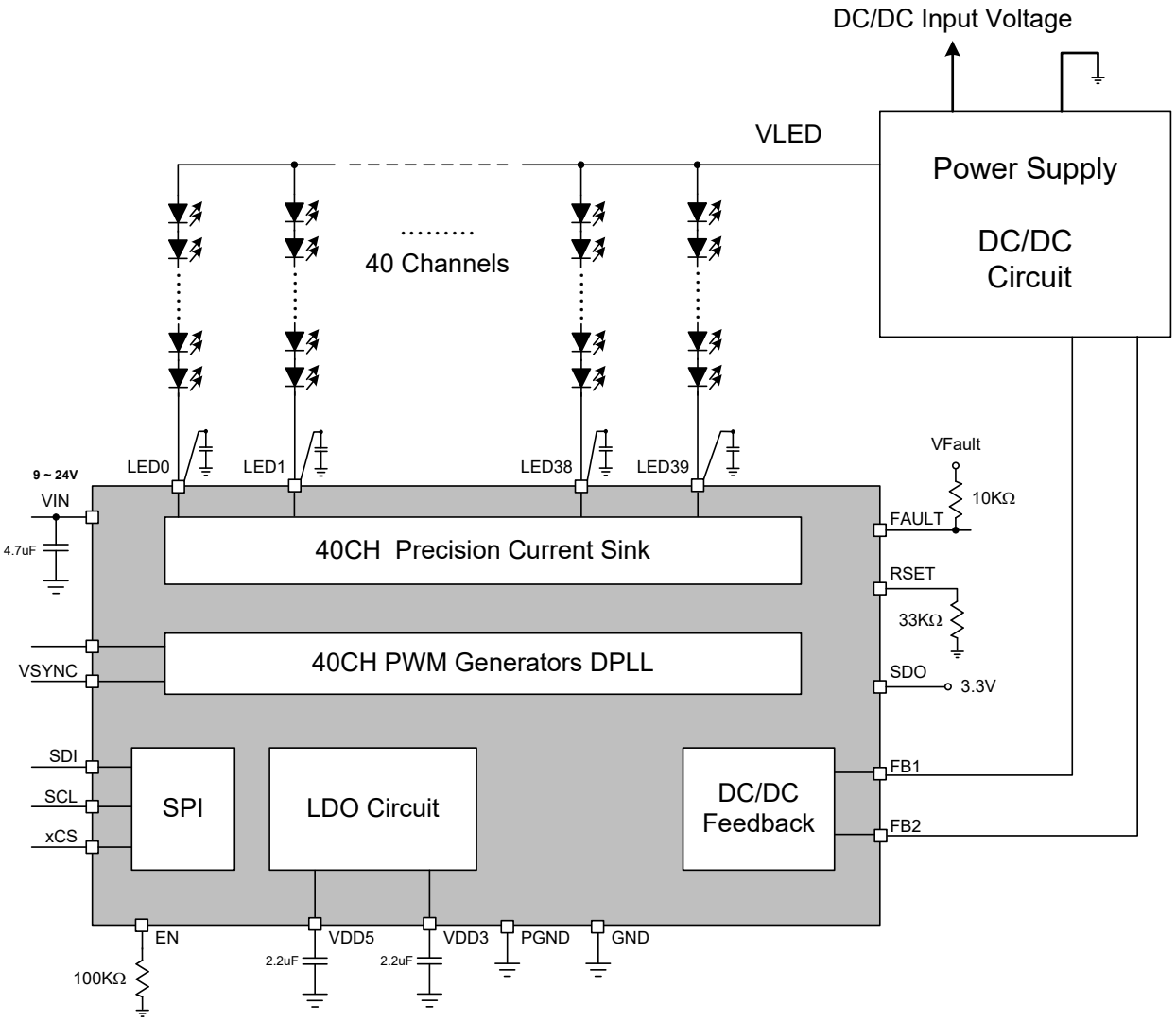


CH1: V_{VSYNC} - 2V/div
CH2: V_{OUT} - 10V/div
CH3: -
CH4: I_{LEDx} - 50mA/div
Time: 50ms/div

Block Diagram



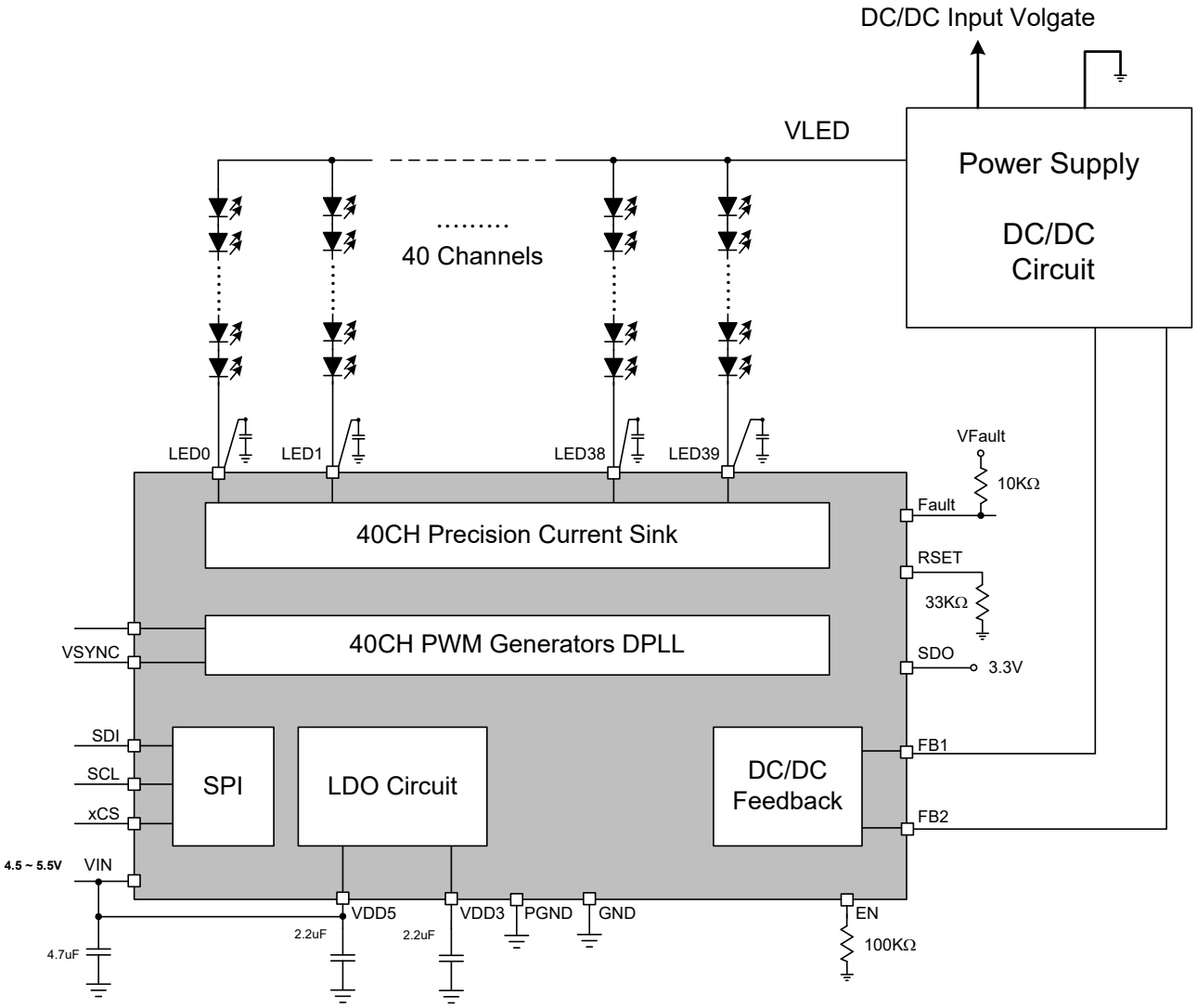
Typical Application Circuit 1:



Note 4: When LED0 to 39 of APE5039 pin-out location to External LED string cathode location has exceed 1uH wire inductance, suggestion add the MLCC capacitors for holdout interference.

Typical Application Circuit 2:

For VIN shorted to VDD5 application



Note 5: When LED0 to 39 of APE5039 pin-out location to External LED string cathode location has exceed 1uH wire inductance, suggestion add the MLCC capacitors for holdout interference.

Function Description

Power Sequence and UVLO

The APE5039 are integrates Mosfet and 40 channel LED controller for LCD backlight. Its high accurate LED current 2% (60mA LED current) and wide input voltage range.

The APE5039 Using power sequence as below figure 1 and 2:

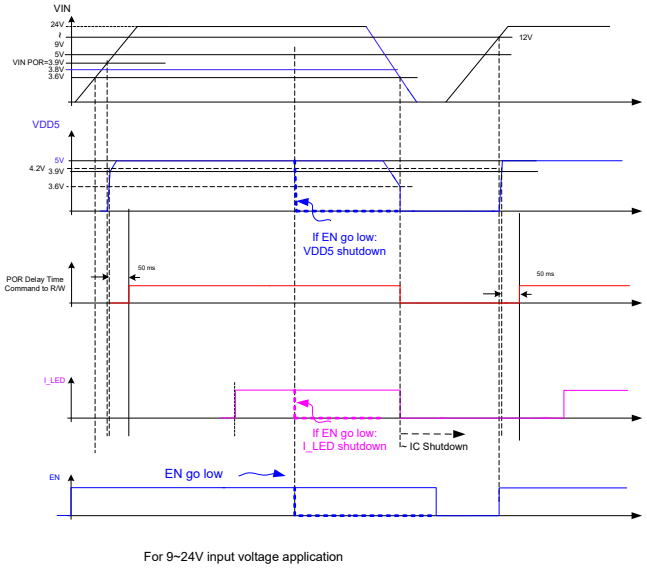


Figure 1: Power Sequence

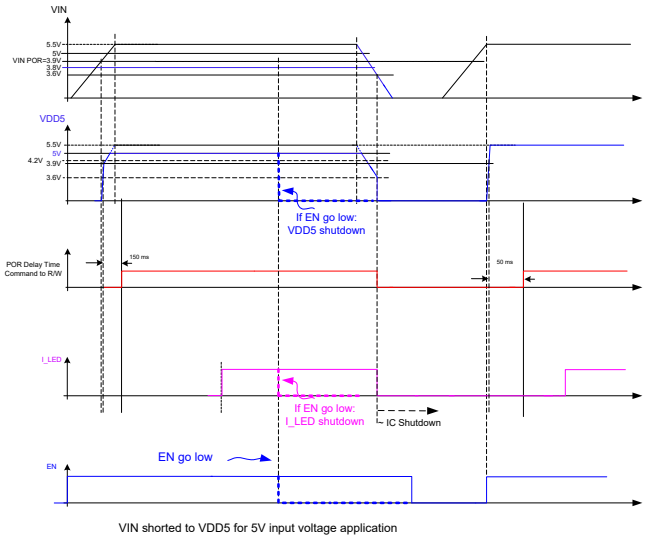


Figure 2: Power Sequence

When VIN supply power voltage exceeds input POR level (the EN pin must to be high level), the APE5039 will be standby mode status. At this time, the SPI commend can be reading / writing after must waiting 50ms.
If the VIN supply power voltage was continuous falling down to UVLO=3.6V (falling) then the APE5039 is shutdown mode (or EN pin was pull to low level).

LED Short Detection

The APE5039 has LED short detection function. When LED string happen short conditions then APE5039 can detection the abnormal condition. The register address 0x005D bits[12:10] are setting LED string short condition, it's from 3V adjustment to 12V for different LED string application.

Table 1: Short LED Function Register

Address	Bit	Name	Description
0x005Dh	[12:10]	Short_level[2:0]	Note 6

Note 6:
Short detection voltage based on drain.
Bits[12:10]=000 … 3V.
Bits[12:10]=001 … 4V.
…
Bits[12:10]=110 … 9V.
Bits[12:10]=111 … 12V.

APE5039 short LED function has retrial and auto-off behavior. If APE5039 want to enable auto-off function then register address 0x005D bit[13] must is 1 and register address 0x005D bit[15]=1, at this time; the LED0 to LED39 voltage was exceed setting short_level [2:0] then LED channels will be turn off. On the contrary; the LED channels was normal operation.

If short LED function behavior is retrial function then register address 0x005D bit[13], 0x005D bit[14] and 0x005D bit[15] are setting 1, when LED0 to LED39 voltage was exceed short_level [2:0] then LED channels will be on-off phenomenon, on the contrary; the LED channels were normal operation.

Table 2: Retrial Time Setting Register

Address	Bit	Name	Description
0x0075h	[10:0]	Retrial_Time	Note 7

Note 7:
The address 0x0075 bit[10:0] are setting LED open and short LED retrial time, the resolution is per 1ms/LSB.
0x0075 bits[10:0]=00000000000 … no retrial time.
0x0075 bits[10:0]=00000000001 … 1ms.
0x0075 bits[10:0]=00000000010 … 2ms.
…
0x0075 bits[10:0]=011111001110 … 1998ms.
0x0075 bits[10:0]=011111001111 … 1999ms.

Function Description (Cont.)

When short LED function was happened and short LED is retrial behavior, the retrial time can be setting and fault times also can be setting by register, see the table 2 and 3.

Table 3: Short LED Function Register

Address	Bit	Name	Description
0x005Dh	[9:8]	Short_debouncer	00: 1 fault 01: 6 faults 10: 11 faults 11: 15 faults

Suggestion the APE5039 using the LED short detection must the address register current_on can to 1 after the address 0x005D bits[15:13] is setting finished first. If the registers were setting; the registers value should not be adjusted.

LED Open Detection

The APE5039 has LED open detection function, when LED string or any LED happen open condition then the APE5039 can detection that abnormal operation.

Table 4: LED Open Function Register

Address	Bit	Name	Description
0x005Dh	[6]	LED_Open_EN	Note 8

Note 8:
Bit[6]=0 … LED Open detection disabled.
Bit[6]=1 … LED Open detection enable.

APE5039 LED open detection function is wanted to enable must use register address 0x005D bit[6]=1 then LED open detection will be enabled. On the contrary; the LED short function will be disabling.

Table 5: LED Open Function Register

Address	Bit	Name	Description
0x005Dh	[7]	Retrial_Open	Note 9
0x005Dh	[5]	Auto_Off_Open	Note 10

Note 9:
Bit[7]=0 … retrial open function disable.
Bit[7]=1 … retrial open function enable.

Note 10:
Bit[5]=0 … auto-off open function disable.
Bit[5]=1 … auto-off open function enable.

APE5039 LED open detection function has retrial open and auto-off open behavior. If APE5039 want to enable auto-off open function then register address 0x005D bit[6] must is 1 and register address 0x005D bit[5]=1, at this time; the LEDx voltage was lower than then internal threshold then LEDx channels will be turn off and latch. Even if the LED open failure was eliminating then LEDx channels are not work properly. The auto-off open function sees the figure 3-1 as below.

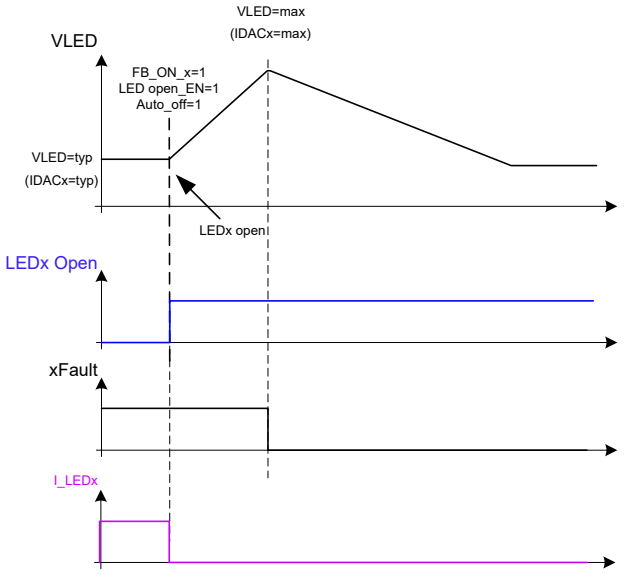


Figure 3-1: LED open - auto off

If the LED open function is wanted to retrial behavior, the register address 0x005D bit[6] and 0x005D bit[7] setting to 1. When any LEDx channels are open then IDACx will be increase to max value until to LED open is still existence. The detail LED open retrial behavior sees the figure 3-2 as below:

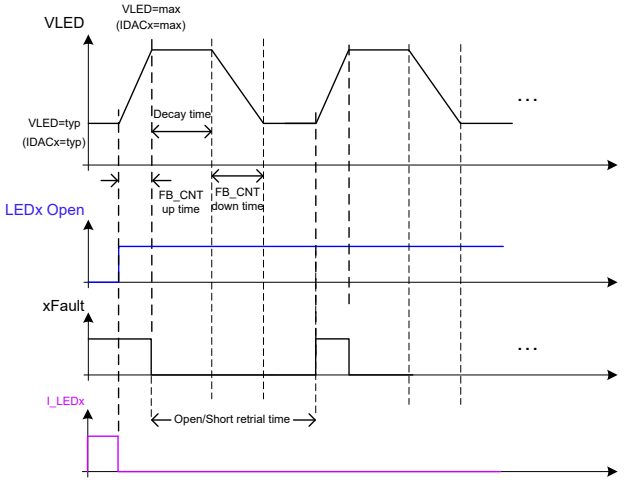


Figure 3-2: LED open - retrial

Function Description (Cont.)

OTW and OTP

The APE5039 has OTW and OTP protection function, when APE5039 happen any abnormal operation causes to over temperature until to reach OTP then the xfault pin will be turn low.

Table 6: Auto-off OTP Register

Address	Bit	Name	Description
0x005Dh	[3]	Auto_off_OTP	Note 11

Note 11:
Bit[3]=0 … temperature shutdown disabled.
Bit[3]=1 … temperature shutdown enable.

The table 6 is setting auto-off OTP, when this bit is setting to 1 then LED current will be turn off when happen OTP condition. On the contrary; the OTP function will be disabling. By the way; when the auto-off OTW and OTW selection was setting then auto-off OTP was not setting to 1 still can be turn off LED current.
Secondly; the address 0x0064 bit[4] is detection the OTP fault register. If this bit was written to 1 then OTP happen, On the contrary; the OTP condition is not happened. The same detection function address 0x0064 bit[6] is detection OTW function; the function is the same OTP. The address 0x0064 bit[6] must cooperate address 0x005D bit[1:0] was setting to 00 to 10 then this bit can be response.

Table 7: OTW Selection Function Register

Address	Bit	Name	Description
0x005Dh	[1:0]	OTW Selection	Note 12

Note 12:
Bits[1:0]=00 … 110°C.
Bits[1:0]=01 … 120°C.
Bits[1:0]=10 … 140°C.
Bits[1:0]=11 … Disable.

The table 7 is setting OTW selection register; it does can be setting different OTW point and OTW function disable.

Table 8: Auto-off OTW Register

Address	Bit	Name	Description
0x005Dh	[4]	Auto_off_OTW	Note 13

Note 13:
Bit[4]=0 … Warning temperature (OTW) shutdown disabled.
Bit[4]=1 … Warning temperature (OTW) shutdown enabled.

The table 8 is setting auto_off OTW function, when this bit is setting to 1 then the temperature is reaction to OTW point, the LED current will be turn off, on the contrary; then LED current is not turn off.

To sum it up the OTW and OTP function; the as below table 9 has OTW and OTP true table can see overall behavior.

Table 9: OTW and OTP True Table

Temperature	OTW SEL	OTW	OTP	OTW Fault register	OTP Fault register	LED Current	xFault PIN
Temp >110°C	0	0	0	x	x	x	High
Temp >160°C	0	0	0	x	fault	x	Low
Temp >110°C	0	0	1	x	x	x	High
Temp >160°C	0	0	1	x	fault	shutdown	Low
Temp >110°C	0	1	0	x	x	x	High
Temp >160°C	0	1	0	x	fault	x	Low
Temp >110°C	0	1	1	x	x	x	High
Temp >160°C	0	1	1	x	fault	shutdown	Low
Temp >110°C	1	0	0	fault	x	x	Low
Temp >160°C	1	0	0	fault	fault	x	Low
Temp >110°C	1	0	1	fault	x	x	Low
Temp >160°C	1	0	1	fault	fault	shutdown	Low
Temp >110°C	1	1	0	fault	x	shutdown	Low
Temp >160°C	1	1	0	fault	fault	shutdown	Low
Temp >110°C	1	1	1	fault	x	shutdown	Low
Temp >160°C	1	1	1	fault	fault	shutdown	Low

Dither PWM mode and Normal PWM mode

The Dither PWM mode is shown in the figure below.
When the code will increase, the output current conduction time will also increase at the same time. The method of increase is the red waveform in the figure. It is cycled every 8 times. For example; the PWM output current frequency was around 23KHz, when the output current conduction time was increase 1 code value then conduction time was increase around 86 ns. If the code increases, the red waveform will have more values until it reaches the maximum value.
The conduction time can adjustment 0x0000 register (local mode) of CH0 or 0x0050 register (global mode). See the register table.
the register 0x0000 bits[12:0] is setting dither PWM duty. It's adjustment range is from 0% to 100% and every ~0.0122%/LSB.

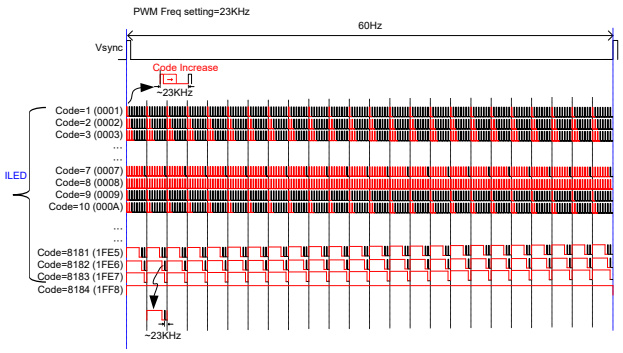


Figure 4: LED current of Dither PWM mode

Function Description (Cont.)

The Normal PWM mode was shown in the figure 5 below. The code is increasing, the output current conduction time will also increase at the same time. The increasing method is every PWM pulse conduction time was increased.
the register 0x0000 bits[9:0] is setting normal PWM duty. It's adjustment range is from 0% to 100% and every ~0.097656%/LSB.

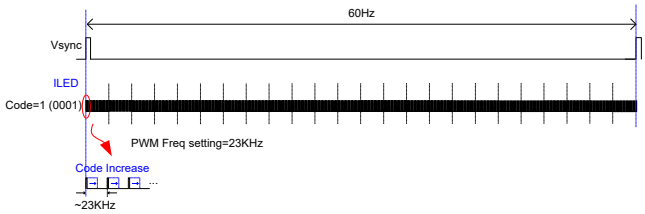


Figure 5: LED current of Normal PWM mode

Because the output frequency around 23KHz of LED current to limit minimum on application wherefore the PWM duty suggest setting to more than 7% (on time more than 3us) For the application using have better in minimum on.

LEDx channels on/off

The APE5039 has 40 LED channels that can be individually control on/off, see then table 10.

Table 10: LEDx channels on/off Register

Address	Bit	Name	Description
0x0052h	[15:0]	Curr_15 – Curr_0	Note 14
0x0053h	[15:0]	Curr_31 – Curr_16	Note 15
0x0054h	[7:0]	Curr_39 – Curr_32	Note 16

Note 14:
Bits[15:0]=0000000000000000 … LED15 to LED0 turn off.
Bits[15:0]=0000000000000001 … LED0 turn on.
Bits[15:0]=0000000000000010 … LED1 turn on.
…
Bits[15:0]=0100000000000000 … LED14 turn on.
Bits[15:0]=1000000000000000 … LED15 turn on.
Every bit is control individually LED channel on/off.

Note 15:
Bits[15:0]=0000000000000000 … LED31 to LED16 turn off.
Bits[15:0]=0000000000000001 … LED16 turn on.
Bits[15:0]=0000000000000010 … LED17 turn on.
…
Bits[15:0]=0100000000000000 … LED30 turn on.
Bits[15:0]=1000000000000000 … LED31 turn on.
Every bit is control individually LED channel on/off.

Note 16:
Bits[7:0]=00000000 … LED39 to LED32 turn off.
Bits[7:0]=00000001 … LED32 turn on.
Bits[7:0]=00000010 … LED33 turn on.
…
Bits[7:0]=01000000 … LED38 turn on.
Bits[7:0]=10000000 … LED39 turn on.
Every bit is control individually LED channel on/off.

IDAC Adjustment

The APE5039 include 10 bits IDAC code, it's provided user can be adjustment LED current. Every bit corresponds IDAC code adjustment LED current as below table 11:

Table 11: IDAC Correspondence Table

Bit (dec)	LED current (mA)	Note
1	~ 0.142045	-
2	~ 0.284091	-
422	~ 59.943182	default
704	~ 100	-
1022	~ 145.17045	-
1023	~ 145.3125	-

In addition; the address 0x0028 to 0x004F are CH0 to CH39 adjustment IDAC registers for LED current control. 0x0050 is setting LED current for global control all channels. See the table12.

Table 12: IDAC Register

Address	Bit	Name	Description
0x0028h	[9:0]	IDAC_CH0	-
0x0029h	[9:0]	IDAC_CH1	-
….. ….. …..			
0x004Eh	[9:0]	IDAC_CH38	-
0x004Fh	[9:0]	IDAC_CH39	-
0x0051h	[9:0]	GDAC	For all channels

This is a simple calculation formula for IDAC (mA).

PWM mode current:
I_{LED} (mA) = ~0.142045mA*IDAC_Code (1~1023)

As above formula calculate by RSET 33KOhm.

Function Description (Cont.)

PWM Delay and PWM Brightness

The address 0x0080 to 0x00A7 is setting PWM delay time. It's has 10 bits resolution can adjustment LED0 to LED39. The register sees the register map. The PWM delay time can adjustment range is from 0 to 1023 code base-on LED current frequency reciprocals.
The address 0x0000 to 0x0027 is setting PWM brightness. It's has 13 bits resolution can adjustment LED0 to LED39. the resolution is approximate 0.0122%/LSB for dither mode. On the contrary; it's the normal mode then 10 bits resolution can adjustment.

Decay Time

In order to auto adjustment optima output voltage by external circuit, it need to detect time and function. The table 13 is setting detection enable/disable. The detect time can be adjustment range from 16ms change to 128ms.
Suggestion the registers were setting; the registers value should not be adjusted.

Table 13: FB decay enable/disable Register

Address	Bit	Name	Description
0x005Ch	[1]	Fb2_decay_off	Note 17
0x005Ch	[0]	Fb1_decay_off	Note 18

Note 17:
Bit[1]=0 … FB counter2 decay time is enable and defined by register decay_time.
Bit[1]=1 … FB counter2 decay time is disable.

Note 18:
Bit[0]=0 … FB counter1 decay time is enable and defined by register decay_time.
Bit[0]=1 … FB counter1 decay time is disable.

Table 14: FB decay enable/disable Register

Address	Bit	Name	Description
0x005Ch	[3:2]	Fbcount_decay_time[1:0]	Note 19

Note 19:
Bits[3:2]=00 … 16ms.
Bits[3:2]=01 … 32ms.
Bits[3:2]=10 … 64ms.
Bits[3:2]=11 … 128ms.

HDR Control

The APE5039 has HDR mode function, it mainly control LED current by software mechanism.

When HDR control is setting to software control then LED current value by register 0x0072 bits[3:0].

Table 15: HDR Current Level Register

Address	Bit	Name	Description
0x0072h	[3:0]	HDR_Level	Note 20

Note 20:
Bits[3:0]=0000 … 1xIDAC.
Bits[3:0]=0001 … 0.9xIDAC.
…
Bits[3:0]=1001 … 0.1xIDAC.
Bits[3:0]=1010 … 1xIDAC.
Bits[3:0]=1011 … 1xIDAC.
…
Bits[3:0]=1111 … 1xIDAC.

ILED Output Mode

The APE5039 has selection ILED output mode by register 0x005B bit[6], it's control ILED current output type.

Table 16: ILED Output Control Register

Address	Bit	Name	Description
0x005Bh	[6]	DC_mode	Note 21

Note 21:
Bit[6]=0 … channels output current – PWM mode.
Bit[6]=1 … channels output current – DC mode.

Global Mode Control

The APE5039 has global/local mode, the register 0x005C bits[11:4], 0x0051 bits[9:0] and 0x005C bits[12:0] are control global mode behavior.

Function Description (Cont.)

Table 17: Global Mode Control

Address	Bit	Name	Description
0x005Ch	[11]	gfb_on	Note 22
0x005Ch	[10]	gfb_on_ctrl_en	Note 23
0x005Ch	[9]	gfb_sel	Note 24
0x005Ch	[8]	gfb_sel_ctrl_en	Note 25
0x005Ch	[7]	gcuron	Note 26
0x005Ch	[6]	gcuron_ctrl_en	Note 27
0x005Ch	[5]	gdac_ctrl_en	Note 28
0x005Ch	[4]	gbri_ctrl_en	Note 29

Note 22:
All channel (0 - 39) FB_ON (Enables feedback) control:
Bit[11]=0 … feedback function of all channel disabled.
Bit[11]=1 … feedback function of all channel enabled.

Note 23:
All channel (0 - 39) FB_ON (Enables feedback) control by "gfb_on (REG: 0x005C[11])" or every channel FB_ON (Enables feedback) control by specific brightness "FB_ONx (REG 0x0058 - 0x005A)"
Bit[10]=0 …FB_ON control by FB_ONx.
Bit[10]=1 … FB_ON control by gfb_on.

Note 24:
All channel select FB for current outputs:
Bit[9]=0 … select FB pin FB1.
Bit[9]=1 … select FB pin FB2.

Note 25:
All channel (0 - 39) FB_SEL (select FB) control by "gfb_sel (REG: 0x005C[9])" or every channel brightness control by specific brightness "FB_SELx (REG 0x0055 - 0x0057)"
Bit[8]=0 … FB_SEL control by FB_SELx.
Bit[8]=1 … FB_SEL control by gfb_sel.

Note 26:
All Channel current output driver control:
Bit[7]=0 … output driver disabled.
Bit[7]=1 … output driver enabled.

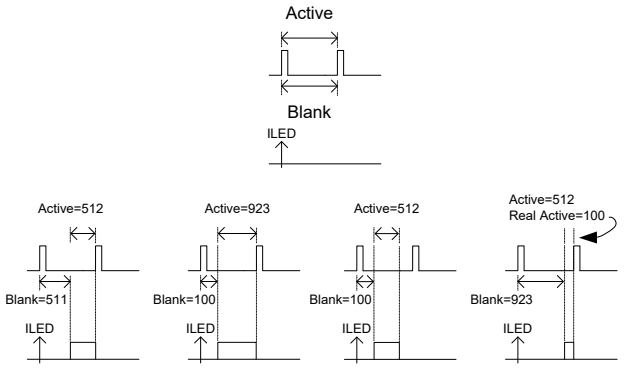
Note 27:
All channel (0 - 39) CUR_ON control by "gcuron (REG: 0x005C[7])" or every channel brightness control by specific brightness "CUR_ONx (REG 0x0052 - 0x0054)"
Bit[6]=0 … CUR_ON control by CUR_ONx.
Bit[6]=1 … CUR_ON control by gcuron.

Note 28:
All channel (0 - 39) IDAC_CH (maximum current) control by "GDAC (REG: 0x0051)" or every channel IDAC_CH (maximum current) control by specific dac "IDAC_CHx (REG 0x0028 - 0x004F)"
Bit[5]=0 … MAX current control by IDAC_CHx.
Bit[5]=1 … MAX current control by GDAC.

Note 29:
All channel (0 - 39) BR_CH (Brightness) control by "GBRI (REG: 0x0050)" or every channel BR_CH (Brightness) control by specific brightness "BR_CHx (REG 0x0000 - 0x0027)"
Bit[4]=0 … MAX current control by BR_CHx.
Bit[4]=1 … MAX current control by GBRI.

MPRT

APE5039 has MPRT function to insert black picture. It's provide the blank time and active time to adjustment.
the blank time is main decided to insert black picture time. the blank start time was from VSYNC rising edge until that's time was stop and then the active time will continue to blank stop time to LED current conduction time to stop. by the way; the active time is main decide LED current conduction time.
the register 0x005B bit[11] is setting this function enable or disable. that bit is setting to 1 then MPRT function will be enable, on the contrary; it's will be disable.
the register 0x0073 bits[9:0] and 0x0074 bits[9:0] are setting blank time and active time. The both adjustment range is from 0 to 1023 and every 1/LSB. For the application using. The sum of blank time and active time were not over than 1023. If blank and active total time was more than 1023, then real active time will be change to (1023 minus active), otherwise; active time was keeping to original time. The waveform is shown the figure 6 as below.



$$ILED = ILED_{SETTING} * \frac{Active\ (real\ active)}{1023}$$

Figure 6: MPRT

Function Description (Cont.)

VSYNC Detection

The APE5039 has VSYNC detection function, the register 0x005B bit[2] is setting to 1 then detect VSYNC signal. If VSYNC is not exist then ILED current will be turn off, on the contrary; then ILED current is exist.

Table 18: ILED Output Control Register

Address	Bit	Name	Description
0x005Bh	[2]	VSYNC_detect	Note 30

Note 30:
Bit[2]=0 … VSYNC detection disabled.
Bit[2]=1 … VSYNC detection enabled.

All outputs are turned off if VSYNC signal is missing for 100ms.

Auto Bias Current

APE5039 has an automatic bias current function. This function mainly provides weak current to prevent the IC terminal from reaching high voltage from the external power circuit and damaging the IC.

Table 19: ILED Output Control Register

Address	Bit	Name	Description
0x0077h	[1:0]	Ibias_set	Note 31

Note 31:
Bits[1:0]=00 … off.
Bits[1:0]=01 … 0.237uA.
Bits[1:0]=10 … 0.473uA.
Bits[1:0]=11 … 0.947uA.

ILED Output Current Frequency Selection

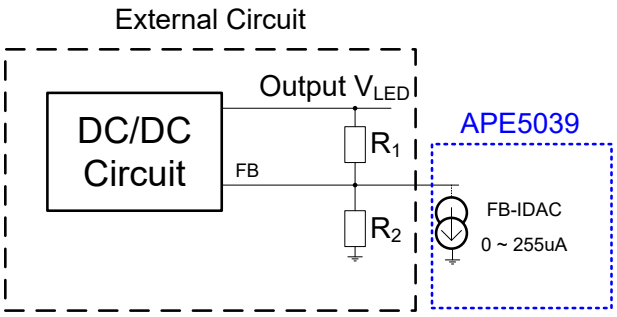
The APE5039 has ILED output current frequency selection function, it's according 0x005B bits[14:12] and VSYNC signal decide to LED current frequency. See the below table 20.

Table 20: LED Current Frequency

Register	VSYNC				(Unit: Hz)
0x005B [14:12]	60	120	240	480	960
000	23040	23040	23040	23040	23040
001	11520	11520	11520	11520	11520
010	5760	5760	5760	5760	5760
011	2880	2880	2880	2880	2880
100	1440	1440	1440	1440	locked (2880)
101	720	720	720	locked (1440)	locked (2880)
110	360	360	locked (720)	locked (1440)	locked (2880)
111	180	locked (360)	locked (720)	locked (1440)	locked (2880)

Dynamic Feedback Control

The APE5039 has FB1 and FB2 terminal can be connect to feedback pin of external DC/DC circuit and control output voltage (V_{LED}) for optimal power efficiency.
The dynamic control mechanism is according to output voltage is not enough condition and then increasing the FB-IDAC value, at the same time; output voltage also increase until to LED current achieve target.
In order to simplify design step, a few process step provide calculate and design as below:



Step 1: Calculate R1
The output voltage is depending on min to max range of LED. Design the R1 value according to with max IDAC value 255uA as below formula:

$$R_1 = \frac{V_{LED(MAX)} - V_{LED(MIN)}}{255uA}$$

Suggestion the R1 value multiply by IDAC current max value is not more than over voltage protection point of external DC/DC circuit. Otherwise; when the IDAC value is increasing to max value then happen protection of external DC/DC circuit. Secondly; the LED output voltage max to min range must according to actual LED specification.

Function Description (Cont.)

Step 2: Calculate R2
The R2 value calculates as below formula:

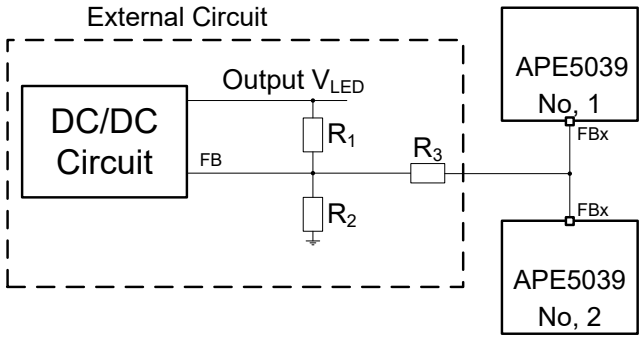
$$R_2 = \frac{R_1}{(\frac{V_{LED(MIN)}}{V_{FB}} - 1)}$$

The APE5039 using automatic mode and manual mode can be adjustment FB-IDAC current. If adjustment mode is choosing the manual mode, then using address 0x005E bit [5] and bit[4] setting to 1 and increasing the address 0x005F bits[10:0] and 0x0060 bits[10:0] value so that increasing output voltage.
According to formula as below:

$$V_{LED} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB} + R_1 \times FB\_IDAC_{(COUNTER)} \times 0.125uA$$

If one DC/DC converter is connected 2 or more than APE5039 structure suggest series resistor between FBx terminal and DC/DC circuit feedback terminal let FBx current can up to 255uA. The R3 value calculates as below:

$$R_3 = \frac{V_{FB}}{255uA}$$



If possible; try to let FBx pin terminal keep to 0.25V and it's not less than 0.25V.

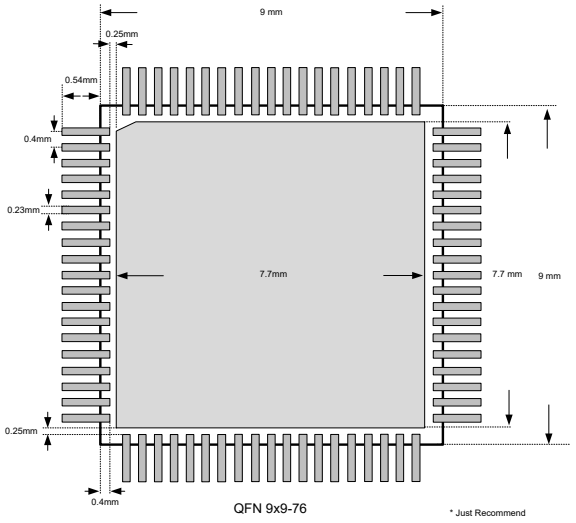
Application Information

Layout Consideration

The APE5039 was using less external components. Suggestion the RSET, input capacitor and VDD5/VDD3 capacitor are as possible closed to IC terminal.
If using APE5039 the layout consideration can be seen as below figure. When LED current was larges can cause to thermal issue, suggestion using to via then solve the thermal issue.
The holes and via numbers can be effect to thermal, if using holes and via are more, the thermal issue will be decreasing. Thermal problem can using as below points can decrease the thermal issue:

1. Increasing the PCB dimension and add the copper plating of ground side areas.
2. If possible, the PCB layers suggest using 4 layers or more than layer is better.
3. Using the holes size and via connect to all layers and then decrease the thermal issue. To sum it up, according to as be above points, the thermal issue will be effective decreasing and solution.

Minimum Footprint



Register Map

Register Address (hex)	Name	BIT	Label	Default	Description
0x0000	BR_CH0	[12:0]	BR_CH_0[12:0]	0_0000_0000_0000	Channel 0 output current=br_ch_0 x idac Channel 0 brightness control (0.0122% per step) Dither Mode (data width 13bit) 0x0000: 0% (default) 0x0001: 0.10986328% (9/1024*8) 0x0002: 0.12207031% (10/1024*8) 0x0003: 0.13427734% (11/1024*8) 0x0004: 0.14648437% (12/1024*8) 0x0005: 0.15869140% (13/1024*8) 0x0006: 0.17089843% (14/1024*8) 0x0007: 0.18310546% (15/1024*8) … 0x0011: 0.305175781% (25/1024*8) ... 0x00A4: 2.099609375% (172/1024*8) ... 0x0657: 19.90966796% (1631/1024*8) ... 0x0FF8: 50.00000000% (4096/1024*8) ... 0x1FF6: 99.97558593% (8190/1024*8) 0x1FF7: 99.98779296% (8191/1024*8) 0x1FF8: 100.00000000% (8192/1024*8) 0x1FF9: 100.00000000% (8192/1024*8) ... 0x1FFF: 100.00000000% (8192/1024*8) ---------- Normal Mode (data width 10bit) (0.09765625% per step) 0x0000: 0% (default) 0x0001: 0.19531250% (2/1024) 0x0002: 0.29296875% (3/1024) 0x0003: 0.39062500% (4/1024) 0x0004: 0.48828125% (5/1024) 0x0005: 0.58593750% (6/1024) 0x0006: 0.68389375% (7/1024) 0x0007: 0.78125000% (8/1024) … 0x01FF: 50.00000000% (511/1024) ... 0x03FE: 99.90234375% (1023/1024) 0x03FF: 100.00000000% (1024/1024)

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0001	BR_CH1	[12:0]	BR_CH_1[12:0]	0_0000_0000_0000	CH1 PWM Brightness
0x0002	BR_CH2	[12:0]	BR_CH_2[12:0]	0_0000_0000_0000	CH2 PWM Brightness
0x0003	BR_CH3	[12:0]	BR_CH_3[12:0]	0_0000_0000_0000	CH3 PWM Brightness
0x0004	BR_CH4	[12:0]	BR_CH_4[12:0]	0_0000_0000_0000	CH4 PWM Brightness
0x0005	BR_CH5	[12:0]	BR_CH_5[12:0]	0_0000_0000_0000	CH5 PWM Brightness
0x0006	BR_CH6	[12:0]	BR_CH_6[12:0]	0_0000_0000_0000	CH6 PWM Brightness
0x0007	BR_CH7	[12:0]	BR_CH_7[12:0]	0_0000_0000_0000	CH7 PWM Brightness
0x0008	BR_CH8	[12:0]	BR_CH_8[12:0]	0_0000_0000_0000	CH8 PWM Brightness
0x0009	BR_CH9	[12:0]	BR_CH_9[12:0]	0_0000_0000_0000	CH9 PWM Brightness
0x000A	BR_CH10	[12:0]	BR_CH_10[12:0]	0_0000_0000_0000	CH10 PWM Brightness
0x000B	BR_CH11	[12:0]	BR_CH_11[12:0]	0_0000_0000_0000	CH11 PWM Brightness
0x000C	BR_CH12	[12:0]	BR_CH_12[12:0]	0_0000_0000_0000	CH12 PWM Brightness
0x000D	BR_CH13	[12:0]	BR_CH_13[12:0]	0_0000_0000_0000	CH13 PWM Brightness
0x000E	BR_CH14	[12:0]	BR_CH_14[12:0]	0_0000_0000_0000	CH14 PWM Brightness
0x000F	BR_CH15	[12:0]	BR_CH_15[12:0]	0_0000_0000_0000	CH15 PWM Brightness
0x0010	BR_CH16	[12:0]	BR_CH_16[12:0]	0_0000_0000_0000	CH16 PWM Brightness
0x0011	BR_CH17	[12:0]	BR_CH_17[12:0]	0_0000_0000_0000	CH17 PWM Brightness
0x0012	BR_CH18	[12:0]	BR_CH_18[12:0]	0_0000_0000_0000	CH18 PWM Brightness
0x0013	BR_CH19	[12:0]	BR_CH_19[12:0]	0_0000_0000_0000	CH19 PWM Brightness
0x0014	BR_CH20	[12:0]	BR_CH_20[12:0]	0_0000_0000_0000	CH20 PWM Brightness
0x0015	BR_CH21	[12:0]	BR_CH_21[12:0]	0_0000_0000_0000	CH21 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0016	BR_CH22	[12:0]	BR_CH_22[12:0]	0_0000_0000_0000	CH22 PWM Brightness
0x0017	BR_CH23	[12:0]	BR_CH_23[12:0]	0_0000_0000_0000	CH23 PWM Brightness
0x0018	BR_CH24	[12:0]	BR_CH_24[12:0]	0_0000_0000_0000	CH24 PWM Brightness
0x0019	BR_CH25	[12:0]	BR_CH_25[12:0]	0_0000_0000_0000	CH25 PWM Brightness
0x001A	BR_CH26	[12:0]	BR_CH_26[12:0]	0_0000_0000_0000	CH26 PWM Brightness
0x001B	BR_CH27	[12:0]	BR_CH_27[12:0]	0_0000_0000_0000	CH27 PWM Brightness
0x001C	BR_CH28	[12:0]	BR_CH_28[12:0]	0_0000_0000_0000	CH28 PWM Brightness
0x001D	BR_CH29	[12:0]	BR_CH_29[12:0]	0_0000_0000_0000	CH29 PWM Brightness
0x001E	BR_CH30	[12:0]	BR_CH_30[12:0]	0_0000_0000_0000	CH30 PWM Brightness
0x001F	BR_CH31	[12:0]	BR_CH_31[12:0]	0_0000_0000_0000	CH31 PWM Brightness
0x0020	BR_CH32	[12:0]	BR_CH_32[12:0]	0_0000_0000_0000	CH32 PWM Brightness
0x0021	BR_CH33	[12:0]	BR_CH_33[12:0]	0_0000_0000_0000	CH33 PWM Brightness
0x0022	BR_CH34	[12:0]	BR_CH_34[12:0]	0_0000_0000_0000	CH34 PWM Brightness
0x0023	BR_CH35	[12:0]	BR_CH_35[12:0]	0_0000_0000_0000	CH35 PWM Brightness
0x0024	BR_CH36	[12:0]	BR_CH_36[12:0]	0_0000_0000_0000	CH36 PWM Brightness
0x0025	BR_CH37	[12:0]	BR_CH_37[12:0]	0_0000_0000_0000	CH37 PWM Brightness
0x0026	BR_CH38	[12:0]	BR_CH_38[12:0]	0_0000_0000_0000	CH38 PWM Brightness
0x0027	BR_CH39	[12:0]	BR_CH_39[12:0]	0_0000_0000_0000	CH39 PWM Brightness

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0028	IDAC_CH0	[9:0]	IDAC_CH_0[9:0]	01_1010_0110	IDAC: single channel maximum current control (142.045uA per step), setting active 0x000: 0mA 0x001: 0.142045mA 0x002: 0.284091mA 0x003: 0.426136mA 0x004: 0.568182mA 0x005: 0.710227mA 0x006: 0.852273mA 0x007: 0.994318mA … 0x0D3: 29.971591mA ... 0x11A: 40.056818mA ... 0x160: 50.000000mA ... 0x1A6: **59.943182mA (default)** ... 0x2C0: 100.0mA ... 0x3FF: 145.3125mA
0x0029	IDAC_CH1	[9:0]	IDAC_CH_1[9:0]	01_1010_0110	CH1 IDAC current
0x002A	IDAC_CH2	[9:0]	IDAC_CH_2[9:0]	01_1010_0110	CH2 IDAC current
0x002B	IDAC_CH3	[9:0]	IDAC_CH_3[9:0]	01_1010_0110	CH3 IDAC current
0x002C	IDAC_CH4	[9:0]	IDAC_CH_4[9:0]	01_1010_0110	CH4 IDAC current
0x002D	IDAC_CH5	[9:0]	IDAC_CH_5[9:0]	01_1010_0110	CH5 IDAC current
0x002E	IDAC_CH6	[9:0]	IDAC_CH_6[9:0]	01_1010_0110	CH6 IDAC current
0x002F	IDAC_CH7	[9:0]	IDAC_CH_7[9:0]	01_1010_0110	CH7 IDAC current
0x0030	IDAC_CH8	[9:0]	IDAC_CH_8[9:0]	01_1010_0110	CH8 IDAC current
0x0031	IDAC_CH9	[9:0]	IDAC_CH_9[9:0]	01_1010_0110	CH9 IDAC current
0x0032	IDAC_CH10	[9:0]	IDAC_CH_10[9:0]	01_1010_0110	CH10 IDAC current
0x0033	IDAC_CH11	[9:0]	IDAC_CH_11[9:0]	01_1010_0110	CH11 IDAC current
0x0034	IDAC_CH12	[9:0]	IDAC_CH_12[9:0]	01_1010_0110	CH12 IDAC current
0x0035	IDAC_CH13	[9:0]	IDAC_CH_13[9:0]	01_1010_0110	CH13 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0036	IDAC_CH14	[9:0]	IDAC_CH_14[9:0]	01_1010_0110	CH14 IDAC current
0x0037	IDAC_CH15	[9:0]	IDAC_CH_15[9:0]	01_1010_0110	CH15 IDAC current
0x0038	IDAC_CH16	[9:0]	IDAC_CH_16[9:0]	01_1010_0110	CH16 IDAC current
0x0039	IDAC_CH17	[9:0]	IDAC_CH_17[9:0]	01_1010_0110	CH17 IDAC current
0x003A	IDAC_CH18	[9:0]	IDAC_CH_18[9:0]	01_1010_0110	CH18 IDAC current
0x003B	IDAC_CH19	[9:0]	IDAC_CH_19[9:0]	01_1010_0110	CH19 IDAC current
0x003C	IDAC_CH20	[9:0]	IDAC_CH_20[9:0]	01_1010_0110	CH20 IDAC current
0x003D	IDAC_CH21	[9:0]	IDAC_CH_21[9:0]	01_1010_0110	CH21 IDAC current
0x003E	IDAC_CH22	[9:0]	IDAC_CH_22[9:0]	01_1010_0110	CH22 IDAC current
0x003F	IDAC_CH23	[9:0]	IDAC_CH_23[9:0]	01_1010_0110	CH23 IDAC current
0x0040	IDAC_CH24	[9:0]	IDAC_CH_24[9:0]	01_1010_0110	CH24 IDAC current
0x0041	IDAC_CH25	[9:0]	IDAC_CH_25[9:0]	01_1010_0110	CH25 IDAC current
0x0042	IDAC_CH26	[9:0]	IDAC_CH_26[9:0]	01_1010_0110	CH26 IDAC current
0x0043	IDAC_CH27	[9:0]	IDAC_CH_27[9:0]	01_1010_0110	CH27 IDAC current
0x0044	IDAC_CH28	[9:0]	IDAC_CH_28[9:0]	01_1010_0110	CH28 IDAC current
0x0045	IDAC_CH29	[9:0]	IDAC_CH_29[9:0]	01_1010_0110	CH29 IDAC current
0x0046	IDAC_CH30	[9:0]	IDAC_CH_30[9:0]	01_1010_0110	CH30 IDAC current
0x0047	IDAC_CH31	[9:0]	IDAC_CH_31[9:0]	01_1010_0110	CH31 IDAC current
0x0048	IDAC_CH32	[9:0]	IDAC_CH_32[9:0]	01_1010_0110	CH32 IDAC current
0x0049	IDAC_CH33	[9:0]	IDAC_CH_33[9:0]	01_1010_0110	CH33 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x004A	IDAC_CH34	[9:0]	IDAC_CH_34[9:0]	01_1010_0110	CH34 IDAC current
0x004B	IDAC_CH35	[9:0]	IDAC_CH_35[9:0]	01_1010_0110	CH35 IDAC current
0x004C	IDAC_CH36	[9:0]	IDAC_CH_36[9:0]	01_1010_0110	CH36 IDAC current
0x004D	IDAC_CH37	[9:0]	IDAC_CH_37[9:0]	01_1010_0110	CH37 IDAC current
0x004E	IDAC_CH38	[9:0]	IDAC_CH_38[9:0]	01_1010_0110	CH38 IDAC current
0x004F	IDAC_CH39	[9:0]	IDAC_CH_39[9:0]	01_1010_0110	CH39 IDAC current

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0050	GBRI	[12:0]	GBRI[12:0]	0_0000_0000_0000	All Channel output current=br_ch_0 x idac Global Channel brightness control (0.0122% per step) Dither Mode (data width 13bit) 0x0000: 0% (default) 0x0001: 0.10986328% (9/1024*8) 0x0002: 0.12207031% (10/1024*8) 0x0003: 0.13427734% (11/1024*8) 0x0004: 0.14648437% (12/1024*8) 0x0005: 0.15869140% (13/1024*8) 0x0006: 0.17089843% (14/1024*8) 0x0007: 0.18310546% (15/1024*8) … 0x0011: 0.305175781% (25/1024*8) ... 0x00A4: 2.099609375% (172/1024*8) ... 0x0657: 19.90966796% (1631/1024*8) ... 0x0FF8: 50.00000000% (4096/1024*8) ... 0x1FF6: 99.97558593% (8190/1024*8) 0x1FF7: 99.98779296% (8191/1024*8) 0x1FF8: 100.00000000% (8192/1024*8) 0x1FF9: 100.00000000% (8192/1024*8) ... 0x1FFF: 100.00000000% (8192/1024*8) ---------- Normal Mode (data width 10bit) (0.09765625% per step) 0x0000: 0% (default) 0x0001: 0.19531250% (2/1024) 0x0002: 0.29296875% (3/1024) 0x0003: 0.39062500% (4/1024) 0x0004: 0.48828125% (5/1024) 0x0005: 0.58593750% (6/1024) 0x0006: 0.68389375% (7/1024) 0x0007: 0.78125000% (8/1024) … 0x01FF: 50.00000000% (511/1024) ... 0x03FE: 99.90234375% (1023/1024) 0x03FF: 100.00000000% (1024/1024)

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0051	GDAC	[9:0]	GDAC[9:0]	01_1010_0110	Global IDAC: single channel maximum current control (142.045uA per step), setting active 0x000: 0mA 0x001: 0.142045mA 0x002: 0.284091mA 0x003: 0.426136mA 0x004: 0.568182mA 0x005: 0.710227mA 0x006: 0.852273mA 0x007: 0.994318mA … 0x0D3: 29.971591mA ... 0x11A: 40.056818mA ... 0x160: 50.000000mA ... **0x1A6: 59.943182mA (default)** ... 0x2C0: 100.0mA ... 0x3FF: 145.3125mA

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0052	CUR_ON_1	[15]	CUR_ON_CH15	0	Channel 15 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[14]	CUR_ON_CH14	0	Channel 14 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[13]	CUR_ON_CH13	0	Channel 13 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[12]	CUR_ON_CH12	0	Channel 12 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[11]	CUR_ON_CH11	0	Channel 11 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[10]	CUR_ON_CH10	0	Channel 10 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[9]	CUR_ON_CH9	0	Channel 9 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[8]	CUR_ON_CH8	0	Channel 8 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[7]	CUR_ON_CH7	0	Channel 7 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[6]	CUR_ON_CH6	0	Channel 6 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[5]	CUR_ON_CH5	0	Channel 5 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[4]	CUR_ON_CH4	0	Channel 4 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[3]	CUR_ON_CH3	0	Channel 3 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[2]	CUR_ON_CH2	0	Channel 2 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[1]	CUR_ON_CH1	0	Channel 1 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[0]	CUR_ON_CH0	0	Channel 0 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x0053	CUR_ON_2	[15:0]	CURR_ON_CH31 - CURR_ON_CH16	0000_0000_0000_0000	Channel 31 - 16 current output driver control: **0: output driver disabled (default)** 1: output driver enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0054	CUR_ON_3	[7:0]	CURR_ON_CH39 - CURR_ON_CH32	0000_0000	Channel 39 - 32 current output driver control: **0: output driver disabled (default)** 1: output driver enabled
0x0055	FB_SEL_1	[15]	FB_SEL_15	0	Select FB channel 15 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[14]	FB_SEL_14	0	Select FB channel 14 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB3
		[13]	FB_SEL_13	0	Select FB channel 13 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB4
		[12]	FB_SEL_12	0	Select FB channel 12 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB5
		[11]	FB_SEL_11	0	Select FB channel 11 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB6
		[10]	FB_SEL_10	0	Select FB channel 10 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB7
		[9]	FB_SEL_9	0	Select FB channel 9 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB8
		[8]	FB_SEL_8	0	Select FB channel 8 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB9
		[7]	FB_SEL_7	0	Select FB channel 7 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[6]	FB_SEL_6	0	Select FB channel 6 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[5]	FB_SEL_5	0	Select FB channel 5 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[4]	FB_SEL_4	0	Select FB channel 4 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[3]	FB_SEL_3	0	Select FB channel 3 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[2]	FB_SEL_2	0	Select FB channel 2 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[1]	FB_SEL_1	0	Select FB channel 1 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[0]	FB_SEL_0	0	Select FB channel 0 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0056	FB_SEL_2	[15:0]	FB_SEL_31 - FB_SEL_16	0000_0000_0000_0000	Select FB channel 31 - 16 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x0057	FB_SEL_3	[7:0]	FB_SEL_39 - FB_SEL_32	0000_0000	Select FB channel 39 - 32 for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
0x0058	FB_ON_1	[15]	FB_ON_15	0	Enables feedback function of output channel 15: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[14]	FB_ON_14	0	Enables feedback function of output channel 14: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[13]	FB_ON_13	0	Enables feedback function of output channel 13: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[12]	FB_ON_12	0	Enables feedback function of output channel 12: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[11]	FB_ON_11	0	Enables feedback function of output channel 11: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[10]	FB_ON_10	0	Enables feedback function of output channel 10: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[9]	FB_ON_9	0	Enables feedback function of output channel 9: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[8]	FB_ON_8	0	Enables feedback function of output channel 8: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[7]	FB_ON_7	0	Enables feedback function of output channel 7: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[6]	FB_ON_6	0	Enables feedback function of output channel 6: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[5]	FB_ON_5	0	Enables feedback function of output channel 5: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0058	FB_ON_1	[4]	FB_ON_4	0	Enables feedback function of output channel 4: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[3]	FB_ON_3	0	Enables feedback function of output channel 3: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[2]	FB_ON_2	0	Enables feedback function of output channel 2: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[1]	FB_ON_1	0	Enables feedback function of output channel 1: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
		[0]	FB_ON_0	0	Enables feedback function of output channel 0: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x0059	FB_ON_2	[15:0]	FB_ON_31 - FB_ON_16	0000_0000_0000_0000	Enables feedback function of output channels 31 - 16: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled
0x005A	FB_ON_3	[7:0]	FB_ON_39 - FB_ON_32	0000_0000	Enables feedback function of output channels 39 - 32: **0: feedback function of selected channel disabled (default)** 1: feedback function of selected channel enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x005B	CTRL	[15]	sw_reset	0	Software reset: **0: normal operation (default)** 1: software reset bit (resets all registers to default)
		[14:12]	pwm_freq_sel [2:0]	000	PWM output frequence selection: **000: 23KHz (default)** 001: 23KHz/2 010: 23KHz/4 011: 23KHz/8 100: 23KHz/16 101: 23KHz/32 110: 23KHz/64 111: 23KHz/128
		[11]	mprt_en	0	MPRT enable/disable: **0: Disable (default)** 1: Enable
		[10:8]	Cgate_compensation [2:0]	000	Current output precharge compensation: **000: Off (default)** 001: Compensate 1 step for PWM output 010: Compensate 2 step for PWM output 011: Compensate 3 step for PWM output 100: Compensate 4 step for PWM output 101: Compensate 5 step for PWM output 110: Compensate 6 step for PWM output 111: Compensate 7 step for PWM output
		[7]	dither_en	1	Dither mode enable/disable: 0: Disable (Brightness resolution 10bit) **1: Enable (Brightness resolution 13bit) (default)**
		[6]	dc_mode	0	PWM/DC Output current control: **0: channels output current - PWM (default)** 1: channels output current - DC (100% duty)
		[5]	clk_sel1	0	Clock source for internal PWM generators: **0: internal RC oscillator (default)** 1: DPLL output
		[4]	clk_sel0	0	Clock source for internal PWM generators: **0: internal RC oscillator (default)** 1: -
		[3]	pwm_inv	0	PWM control invert: **0: normal PWM operation (default)** 1: PWM signals are inverted Note: High time becomes Low Time
		[2]	vsync_detect	0	VSYNC detection: **0: VSYNC detection disabled (default)** 1: VSYNC detection enabled All outputs are turned off if VSYNC signal is missing for 100ms
		[1]	vsync_edge	0	Defines VSYNC trigger edge: **0: trigger on rising edge of VSYNC (default)** 1: trigger on falling edge of VSYNC
		[0]	update_mode	0	Defines when registers (brightness control) are updated: **0: Registers updated with rising edge of xCS (default)** 1: Registers updated with next VSYNC-edge

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x005C	GLOBAL_CTRL	[15]	Standby	0	Standby mode - save power: **0: normal operation (default)** 1: Analog circuit power off (MOS) Digital circuit gating clock
		[14]	dual_ch	0	Two channel combine: odd number channel control by even number channel (EX, ch1 PWM output=ch0 PWM output, ch3 PWM output=ch2 PWM output) **0: disable (default)** 1: enable
		[13:12]	pwm_mode [2:0]	00	PWM output type mode: **00: left-side mode (default)** 01: center mode 10: right-side mode
		[11]	gfb_on	0	All channel (0 - 39) FB_ON (Enables feedback) control: **0: feedback function of all channel disabled (default)** 1: feedback function of all channel enabled
		[10]	gfb_on_ctrl_en	0	All channel (0 - 39) FB_ON (Enables feedback) control by "gfb_on (REG: 0x005C[11])" or every channel FB_ON (Enables feedback) control by specific brightness "FB_ONx (REG 0x0058 - 0x005A)" **0: FB_ON control by FB_ONx (default)** 1: FB_ON control by gfb_on
		[9]	gfb_sel	0	All channel select FB for current outputs: **0: select FB pin FB1 (default)** 1: select FB pin FB2
		[8]	gfb_sel_ctrl_en	0	All channel (0 - 39) FB_SEL (select FB) control by "gfb_sel (REG: 0x005C[9])" or every channel brightness control by specific brightness "FB_SELx (REG 0x0055 - 0x0057)" **0: FB_SEL control by FB_SELx (default)** 1: FB_SEL control by gfb_sel
		[7]	gcuron	0	All Channel current output driver control: **0: output driver disabled (default)** 1: output driver enabled
		[6]	gcuron_ctrl_en	0	All channel (0 - 39) CUR_ON control by "gcuron (REG: 0x005C[7])" or every channel brightness control by specific brightness "CUR_ONx (REG 0x0052 - 0x0054)" **0: CUR_ON control by CUR_ONx (default)** 1: CUR_ON control by gcuron
		[5]	gdac_ctrl_en	0	All channel (0 - 39) IDAC_CH (maximum current) control by "GDAC (REG: 0x0051)" or every channel IDAC_CH (maximum current) control by specific dac "IDAC_CHx (REG 0x0028 - 0x004F)" **0: MAX current control by IDAC_CHx (default)** 1: MAX current control by GDAC

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x005C	GLOBAL_CTRL	[4]	gbri_ctrl_en	0	All channel (0 - 39) BR_CH (Brightness) control by "GBRI (REG: 0x0050)" or every channel BR_CH (Brightness) control by specific brightness "BR_CHx (REG 0x0000 - 0x0027)" **0: MAX current control by BR_CHx (default)** 1: MAX current control by GBRI
		[3:2]	decay_time [1:0]	11	Decay time for power feedback control: 00: 16ms 01: 32ms 10: 64ms **11: 128ms (default)**
		[1]	fb2_decay_off	0	**0: FB counter 2 decay time is defined by register decay_time** 1: FB counter 2 decay time is infinite as long all high times in FB group 2 are 0
		[0]	fb1_decay_off	0	**0: FB counter 1 decay time is defined by register decay_time** 1: FB counter 1 decay time is infinite as long all high times in FB group 1 are 0
0x005D	FAULT_1	[15]	short_retrial	0	**0: retrial function disabled** 1: retrial function enabled Note: channels turned on every second
		[14]	short_auto_off	0	**0: automatic turn off function disabled** 1: automatic turn off channels of shorted group
		[13]	LED_short_en	0	**0: short LED detection disabled** 1: short LED detection for all channels enabled
		[12:10]	short_level [2:0]	011	Short detection voltage: 000…3V 001…4V 010…5V **011…6V** 100…7V 101…8V 110…9V 111…12V
		[9:8]	short_debouncer [1:0]	11	00: 1 fault 01: 6 faults 10: 11 faults **11: 15 faults**
		[7]	open_retrial	0	**0: open LED retrial function disabled** 1: open LED retrial function enabled
		[6]	open_en	0	**0: open LED detection disabled** 1: open LED detection for all channels enabled
		[5]	open_auto_off	0	Automatic feedback turn off in case of open LED: **0: feedback function of open LED channel disabled** 1: feedback function of open LED channel automatically enabled
		[4]	otw_auto_off	0	**0: Warning temperature (OTW) shutdown disabled** 1: Warning temperature (OTW) shutdown enabled

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x005D	FAULT_1	[3]	ovtemp_auto_off	1	0: temperature shutdown disabled **1: temperature shutdown enabled**
		[2]	-	-	-
		[1:0]	otw_sel [1:0]	11	OTW pin configuration: 00: 110°C 01: 120°C 10: 140°C **11: disable**
0x005E	IO_CTRL	[15:14]	slew_rate	00	Defines the slew rate of the output stage: **00: slower** 01: 10: 11: faster
		[13:12]	fbcnt_dn_xn_sel [1:0]	00	FB down counting step time magnification setting: **00: x1** 01: x2 10: x4 11: x8
		[11:10]	fbcnt_up_xn_sel [1:0]	00	FB up counting step time magnification setting: **00: x1** 01: x2 10: x4 11: x8
		[9:8]	fault_io_config [1:0]	00	xFault pin configuration: **00: Open Drain / Pulldown** 01: Push - Pull 10: - 11: -
		[7:6]	sdo_io_config [1:0]	01	SDO output pin configuration: 00: Open Drain / Pulldown **01: Push - Pull** 10: Disabled (HIZ) 11: not used
		[5]	fbcounter_man_fb2	0	**0: FB2 counter in automatic mode** 1: FB2 counter is set manually
		[4]	fbcounter_man_fb1	0	**0: FB1 counter in automatic mode** 1: FB1 counter is set manually
		[3:2]	fbcounter_dn_time [1:0]	01	FB1 and FB2 down counting step time: 00: 512μs **01: 2048μs** 10: 4096μs 11: 8192μs
		[1:0]	fbcounter_up_time [1:0]	01	FB1 and FB2 up counting step time: 00: 1024μs **01: 256μs** 10: 64μs 11: 16μs
0x005F	IDAC_FB1_ COUNTER	[10:0]	idac_fb1_counter [10:0]	000_0000_ 0000	Feedback counter (IDAC) 1 value: **0x000: FB-current 0μA** 0x7FF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb2=1

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0060	IDAC_FB2_ COUNTER	[10:0]	idac_fb2_counter [10:0]	000_0000_ 0000	Feedback counter (IDAC) 2 value: **0x000: FB-current 0μA** 0x7FF: FB-current 255μA Value can be overwritten if Fb_cnt_man_fb1=1
0x0061	BIST_ CONTROL1	[15:6]	-	-	-
		[5]	short_bist_enable2	0	Short BIST enable for FB2: **0: BIST disabled (default)** 1: Start shortled BIST2 test
		[4]	short_bist_enable1	0	Short BIST enable for FB1: **0: BIST disabled (default)** 1: Start shortled BIST1 test
		[3]	bist_fast_time	0	Short BIST up/down time step: **0: 64μS (default)** 1: 128μS
		[2]	bist_select_time	0	**0: use bist_fast_time register value (default)** 1: use fbcounter_up_time / fbcounter_dn_time register values
		[1:0]	wait_sync_pulses [1:0]	10	Wait after BIST target has been reached: 0: no wait 01: wait 1 VSYNC pulse **10: wait 2 VSYNC pulses (default)** 11: wait 3 VSYNC pulses
0x0062	BIST_IDAC1	[10:0]	bist_idac1_val [10:0]	111_1111_1111	Defines the IDAC1 target value for BIST
0x0063	BIST_IDAC2	[10:0]	bist_idac2_val [10:0]	111_1111_1111	Defines the IDAC2 target value for BIST
0x0064	STATUS	[15:8]	-	-	-
		[7]	CLKDCO_LOCK	0	1: notify Clock DCO frequency lock
		[6]	STAT OTW	0	1: notify over temperature warning
		[5]	STAT novsync	0	1: notify VSYNC is missing >100ms
		[4]	STAT ov_temp	0	1: notify over temperature fault
		[3]	STAT open	0	1: notify open LED fault
		[2]	Short LED	0	1: notify short LED fault
		[1]	Short BIST	0	1: notify short BIST fault
		[0]	Power_good	0	0: no power supply (por or res=active) 1: device ok

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0065	SHORTLED_1	[15]	shortled_15	0	Notify shorted LED detected on output ch 15: Read: **0: No shorted LED detected** 1: Shorted LED detected Write: 1: clear fault
		[14]	shortled_14	0	Notify shorted LED detected on output ch 14
		[13]	shortled_13	0	Notify shorted LED detected on output ch 13
		[12]	shortled_12	0	Notify shorted LED detected on output ch 12
		[11]	shortled_11	0	Notify shorted LED detected on output ch 11
		[10]	shortled_10	0	Notify shorted LED detected on output ch 10
		[9]	shortled_9	0	Notify shorted LED detected on output ch 9
		[8]	shortled_8	0	Notify shorted LED detected on output ch 8
		[7]	shortled_7	0	Notify shorted LED detected on output ch 7
		[6]	shortled_6	0	Notify shorted LED detected on output ch 6
		[5]	shortled_5	0	Notify shorted LED detected on output ch 5
		[4]	shortled_4	0	Notify shorted LED detected on output ch 4
		[3]	shortled_3	0	Notify shorted LED detected on output ch 3
		[2]	shortled_2	0	Notify shorted LED detected on output ch 2
		[1]	shortled_1	0	Notify shorted LED detected on output ch 1
		[0]	shortled_0	0	Notify shorted LED detected on output ch 0
0x0066	SHORTLED_2	[15:0]	shortled_31 - shortled_16	0000_0000_0000_0000	Notify shorted LED detected on output ch 31 - 16
0x0067	SHORTLED_3	[7:0]	shortled_39 - shortled_32	0000_0000	Notify shorted LED detected on output ch 39 - 32
0x0068	OPENLED_1	[15]	open_15	0	Notify open LED detected on output ch 15: Read: **0: No open LED detected** 1: Open LED detected Write: 1: clear fault
		[14]	open_14	0	Notify open LED detected on output ch 14
		[13]	open_13	0	Notify open LED detected on output ch 13
		[12]	open_12	0	Notify open LED detected on output ch 12
		[11]	open_11	0	Notify open LED detected on output ch 11
		[10]	open_10	0	Notify open LED detected on output ch 10
		[9]	open_9	0	Notify open LED detected on output ch 9
		[8]	open_8	0	Notify open LED detected on output ch 8
		[7]	open_7	0	Notify open LED detected on output ch 7
		[6]	open_6	0	Notify open LED detected on output ch 6
		[5]	open_5	0	Notify open LED detected on output ch 5
		[4]	open_4	0	Notify open LED detected on output ch 4
		[3]	open_3	0	Notify open LED detected on output ch 3
		[2]	open_2	0	Notify open LED detected on output ch 2
		[1]	open_1	0	Notify open LED detected on output ch 1
		[0]	open_0	0	Notify open LED detected on output ch 0
0x0069	OPENLED_2	[15:0]	openled_31 - openled_16	0000_0000_0000_0000	Notify open LED detected on output ch 31 - 16

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x006A	OPENLED_3	[7:0]	openled_39 - openled_32	0000_0000	Notify open LED detected on output ch 39 - 32
0x006B	COMP_REG1	[15]	comp_reg_15	0	Status of gate trip voltage comparator ch 15: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
		[14]	comp_reg_14	0	Status of gate trip voltage comparator ch 14
		[13]	comp_reg_13	0	Status of gate trip voltage comparator ch 13
		[12]	comp_reg_12	0	Status of gate trip voltage comparator ch 12
		[11]	comp_reg_11	0	Status of gate trip voltage comparator ch 11
		[10]	comp_reg_10	0	Status of gate trip voltage comparator ch 10
		[9]	comp_reg_9	0	Status of gate trip voltage comparator ch 9
		[8]	comp_reg_8	0	Status of gate trip voltage comparator ch 8
		[7]	comp_reg_7	0	Status of gate trip voltage comparator ch 7
		[6]	comp_reg_6	0	Status of gate trip voltage comparator ch 6
		[5]	comp_reg_5	0	Status of gate trip voltage comparator ch 5
		[4]	comp_reg_4	0	Status of gate trip voltage comparator ch 4
		[3]	comp_reg_3	0	Status of gate trip voltage comparator ch 3
		[2]	comp_reg_2	0	Status of gate trip voltage comparator ch 2
		[1]	comp_reg_1	0	Status of gate trip voltage comparator ch 1
		[0]	comp_reg_0	0	Status of gate trip voltage comparator ch 0
0x006C	COMP_REG2	[15:0]	comp_reg_31 - comp_reg_16	0000_0000_ 0000_0000	Status of gate trip voltage comparator ch 31 - 16: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x006D	COMP_REG3	[7:0]	comp_reg_39 - comp_reg_32	0000_0000	Status of gate trip voltage comparator ch 39 - 32: **0: Vgate < Vtrip (default)** 1: Vgate > Vtrip
0x006E	BIST_SHORT_1	[15]	bist_short_15	0	Short LED detected with BIST on ch 15 Read: **0: no short LED detected (default)** 1: Short LED detected Write: 1: clear fault
		[14]	bist_short_14	0	Short LED detected with BIST on ch 14
		[13]	bist_short_13	0	Short LED detected with BIST on ch 13
		[12]	bist_short_12	0	Short LED detected with BIST on ch 12
		[11]	bist_short_11	0	Short LED detected with BIST on ch 11
		[10]	bist_short_10	0	Short LED detected with BIST on ch 10
		[9]	bist_short_9	0	Short LED detected with BIST on ch 9
		[8]	bist_short_8	0	Short LED detected with BIST on ch 8
		[7]	bist_short_7	0	Short LED detected with BIST on ch 7
		[6]	bist_short_6	0	Short LED detected with BIST on ch 6
		[5]	bist_short_5	0	Short LED detected with BIST on ch 5
		[4]	bist_short_4	0	Short LED detected with BIST on ch 4
		[3]	bist_short_3	0	Short LED detected with BIST on ch 3
		[2]	bist_short_2	0	Short LED detected with BIST on ch 2
		[1]	bist_short_1	0	Short LED detected with BIST on ch 1
		[0]	bist_short_0	0	Short LED detected with BIST on ch 0

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x006F	BIST_SHORT_2	[15:0]	bist_short_31 - bist_short_16	0000_0000_0000_0000	Short LED detected with BIST on ch 31 - 16
0x0070	BIST_SHORT_3	[7:0]	bist_short_39 - bist_short_32	0000_0000	Short LED detected with BIST on ch 39 - 32
0x0071	COMP_CTRL	[11]	comp_deb_en	1	COMP debounce (digital debounce) enable / disable: 0: disable **1: enable (default)**
		[10:5]	comp_deb_time [5:0]	00_0100	COMP debounce (digital debounce) time selection: 0.5μs/step 00_0000: disable 00_0001: 0.5μs 00_0010: 1μs 00_0011: 1.5μs **00_0100: 2μs (default)** … 11_1111: 31.5μs
		[4:2]	oled_r [2:0]	001	Reference voltage for feedback / open function Select LED PIN voltage threshold for feedback function LED pin configuration: 000: 0.25V **001: 0.3V (default)** 010: 0.35V 011: 0.4V 100: 0.45V 101: 0.5V 110: 0.55V 111: 0.6V
		[1:0]	cmp_d [1:0]	11	Select delay time for LED PIN detection: 00: 8μs 01: 4μs 10: 2μs **11: 1μs (default)**
0x0072	HDR_CTRL	[3:0]	hdr_level [3:0]	0000	HDR level control: **0000: 1 x IDAC** 0001: 0.9 x IDAC 0010: 0.8 x IDAC 0011: 0.7 x IDAC 0100: 0.6 x IDAC 0101: 0.5 x IDAC 0110: 0.4 x IDAC 0111: 0.3 x IDAC 1000: 0.2 x IDAC 1001: 0.1 x IDAC 1010: 1 x IDAC 1011: 1 x IDAC 1100: 1 x IDAC 1101: 1 x IDAC 1110: 1 x IDAC 1111: 1 x IDAC

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0073	MPRT_CTRL_1	[9:0]	mprt_blank [9:0]	00_0000_0001	MPRT control: blank time, percentage of VSYNC time MPRT blank time: mprt_blank/1023*VSYNC time (16.6ms - 60Hz)
0x0074	MPRT_CTRL_2	[9:0]	mprt_active [9:0]	11_1111_1111	MPRT control: active time, time start from VSYNC edge (0.5us/per step) MPRT active time: mprt_active/1023*VSYNC time (16.6ms - 60Hz)
0x0075	OPENSHORT_ RETRIAL	[10:0]	retrial_time [10:0]	111_1100_1111	Open LED or Short LED Retrial Time (1ms / LSB) 000_0000_0001: 1ms 000_0000_0010: 2ms 000_0000_0011: 3ms … **111_1100_1111: 1.999s**
0x0077	CURR_CTRL	[1:0]	ibias_set [1:0]	01	00: off **01: 0.237uA** 10: 0.473uA 11: 0.947uA
0x007F	ASICID	[15:4]	asic_id[11:0]	0101_0011_ 0101	Device ID of APE5039
		[3:0]	revision[3:0]	0000	Version of APE5039
0x0080	DEL_CH0	[9:0]	del_ch_0[9:0]	00_0000_0000	Channel 0 Delay: based-on ILED Freq delay time/LSB=LED Frequency Reciprocals/1023 23.04KHz >> 1LSB= ~42.43ns 11.52KHz >> 1LSB= ~84.85ns 5.76KHz >> 1LSB= ~169.71ns 2.88KHz >> 1LSB= ~339.42ns 1.44KHz >> 1LSB= ~678.83ns 720Hz >> 1LSB= ~1357.66ns 360Hz >> 1LSB= ~2715.32ns 180Hz >> 1LSB= ~5430.65ns For example ILED Freq=23.04KHz 0x000: 0ns 0x001: 42.43ns 0x002: 84.85ns 0x003: 127.28ns 0x3FE: 43.36us 0x3FF: 43.4us

Register Map (Cont.)

Register Address (hex)	Name	BIT	Label	Default	Description
0x0081	DEL_CH1	[9:0]	del_ch_1[9:0]	00_0000_0000	Channel 1 delay
0x0082	DEL_CH2	[9:0]	del_ch_2[9:0]	00_0000_0000	Channel 2 delay
0x0083	DEL_CH3	[9:0]	del_ch_3[9:0]	00_0000_0000	Channel 3 delay
0x0084	DEL_CH4	[9:0]	del_ch_4[9:0]	00_0000_0000	Channel 4 delay
0x0085	DEL_CH5	[9:0]	del_ch_5[9:0]	00_0000_0000	Channel 5 delay
0x0086	DEL_CH6	[9:0]	del_ch_6[9:0]	00_0000_0000	Channel 6 delay
0x0087	DEL_CH7	[9:0]	del_ch_7[9:0]	00_0000_0000	Channel 7 delay
0x0088	DEL_CH8	[9:0]	del_ch_8[9:0]	00_0000_0000	Channel 8 delay
0x0089	DEL_CH9	[9:0]	del_ch_9[9:0]	00_0000_0000	Channel 9 delay
0x008A	DEL_CH10	[9:0]	del_ch_10[9:0]	00_0000_0000	Channel 10 delay
0x008B	DEL_CH11	[9:0]	del_ch_11[9:0]	00_0000_0000	Channel 11 delay
0x008C	DEL_CH12	[9:0]	del_ch_12[9:0]	00_0000_0000	Channel 12 delay
0x008D	DEL_CH13	[9:0]	del_ch_13[9:0]	00_0000_0000	Channel 13 delay
0x008E	DEL_CH14	[9:0]	del_ch_14[9:0]	00_0000_0000	Channel 14 delay
0x008F	DEL_CH15	[9:0]	del_ch_15[9:0]	00_0000_0000	Channel 15 delay
0x0090	DEL_CH16	[9:0]	del_ch_16[9:0]	00_0000_0000	Channel 16 delay
0x0091	DEL_CH17	[9:0]	del_ch_17[9:0]	00_0000_0000	Channel 17 delay
0x0092	DEL_CH18	[9:0]	del_ch_18[9:0]	00_0000_0000	Channel 18 delay
0x0093	DEL_CH19	[9:0]	del_ch_19[9:0]	00_0000_0000	Channel 19 delay
0x0094	DEL_CH20	[9:0]	del_ch_20[9:0]	00_0000_0000	Channel 20 delay
0x0095	DEL_CH21	[9:0]	del_ch_21[9:0]	00_0000_0000	Channel 21 delay
0x0096	DEL_CH22	[9:0]	del_ch_22[9:0]	00_0000_0000	Channel 22 delay
0x0097	DEL_CH23	[9:0]	del_ch_23[9:0]	00_0000_0000	Channel 23 delay
0x0098	DEL_CH24	[9:0]	del_ch_24[9:0]	00_0000_0000	Channel 24 delay
0x0099	DEL_CH25	[9:0]	del_ch_25[9:0]	00_0000_0000	Channel 25 delay
0x009A	DEL_CH26	[9:0]	del_ch_26[9:0]	00_0000_0000	Channel 26 delay
0x009B	DEL_CH27	[9:0]	del_ch_27[9:0]	00_0000_0000	Channel 27 delay
0x009C	DEL_CH28	[9:0]	del_ch_28[9:0]	00_0000_0000	Channel 28 delay
0x009D	DEL_CH29	[9:0]	del_ch_29[9:0]	00_0000_0000	Channel 29 delay
0x009E	DEL_CH30	[9:0]	del_ch_30[9:0]	00_0000_0000	Channel 30 delay
0x009F	DEL_CH31	[9:0]	del_ch_31[9:0]	00_0000_0000	Channel 31 delay
0x00A0	DEL_CH32	[9:0]	del_ch_32[9:0]	00_0000_0000	Channel 32 delay
0x00A1	DEL_CH33	[9:0]	del_ch_33[9:0]	00_0000_0000	Channel 33 delay
0x00A2	DEL_CH34	[9:0]	del_ch_34[9:0]	00_0000_0000	Channel 34 delay
0x00A3	DEL_CH35	[9:0]	del_ch_35[9:0]	00_0000_0000	Channel 35 delay
0x00A4	DEL_CH36	[9:0]	del_ch_36[9:0]	00_0000_0000	Channel 36 delay
0x00A5	DEL_CH37	[9:0]	del_ch_37[9:0]	00_0000_0000	Channel 37 delay
0x00A6	DEL_CH38	[9:0]	del_ch_38[9:0]	00_0000_0000	Channel 38 delay
0x00A7	DEL_CH39	[9:0]	del_ch_39[9:0]	00_0000_0000	Channel 39 delay

SPI Interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in “Daisy Chain” structure or parallel structure.

SPI Daisy Chain Structure

All SPI slaves share the same clock (SCL) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.
The APE5039 SDO pin was output 3.3V. If the pin will be connecting to host, it must note whether the host I/O can withstand 3.3V.
Setting the SDO I/O type as Open-Drain, then SDO output HIGH was decide by external VIN through a pull-up resister. (As the following block diagram, VDDIO as the external VIN, and R_{SDO_PU} as the pull-up resister).

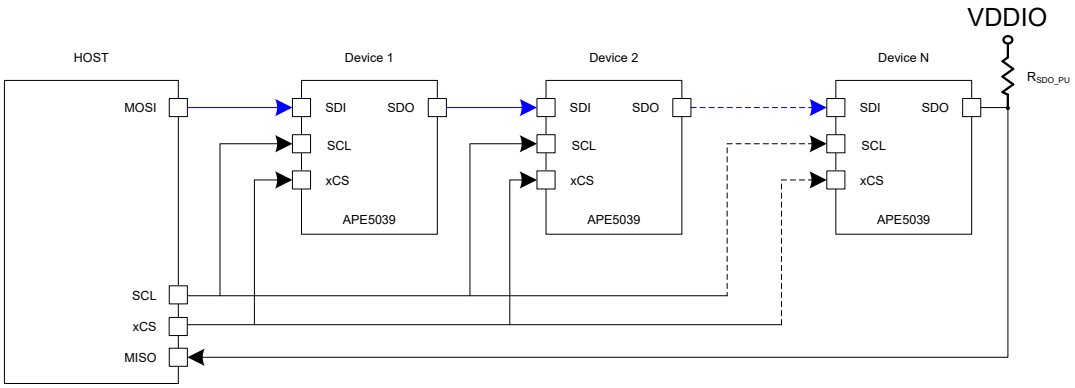


Figure 7: SPI Daisy Chain structure

SPI Parallel Structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCL) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has the “DevAddr=0x0001”. When SPI parallel structure was used then all device SDO pin must choose the open drain type.

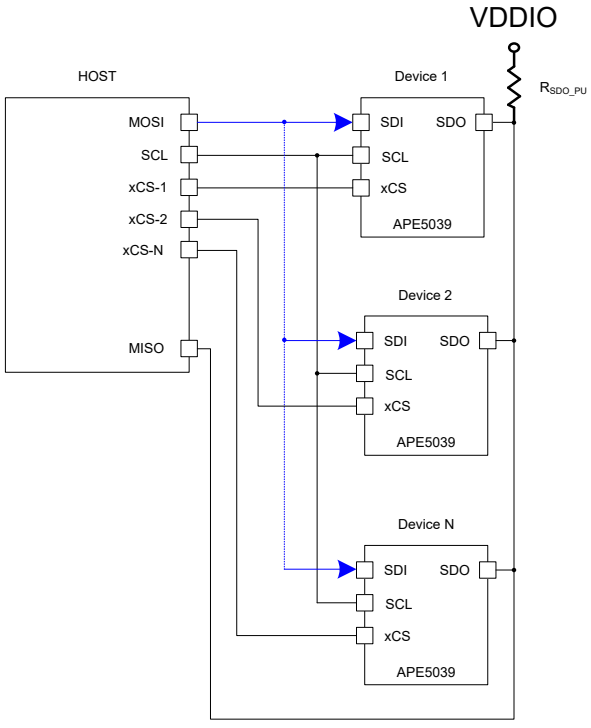


Figure 8: SPI Parallel Structure

SPI Device Address Enumeration

The device address of each driver is automatically set by the position of the device in the chain. The first device has DevAddr=0x0001, the second device has DevAddr=0x0002 and so on. Device Addresses (0x00 and 0x7F) are used for special broadcast writing commands described below.

SPI Protocol

The SPI transmission protocol of APE5039 is mainly composed of several bytes: Command, Register Address and Data. Which is organized in words (16bit) packages. Each message can be built with the following words:

Command:

[15]	[14:8]	[7:0]
Sr	DevAddr	Nr_of_data

Bit	Meaning	Value and Description
[15]	Start bit	Must be 1
[14:8]	Device Address	Addresses a specific driver and defines protocol information 0x00: Broadcast transfer command, write same data to all devices 0x01 to 0x7E: Single device transfer command, Indicate which device to write/read 0x7F: Broadcast transfer command, write different data to all devices
[7:0]	Single byte	Write command: 0x01~0xFF Read command: 0x01~0xFF

Register_address:

[15]	[14:12]	[11:0]
R/W	Reserved	RegAddr

Bit	Meaning	Value and Description
[15]	Read/Write	0: write to register address 1: read from register address
[14:12]	Reserved	Reserved
[11:0]	Select register address	Address from 0x000 to 0xFFF

Data:

[15:0]
Data

The data to be transferred

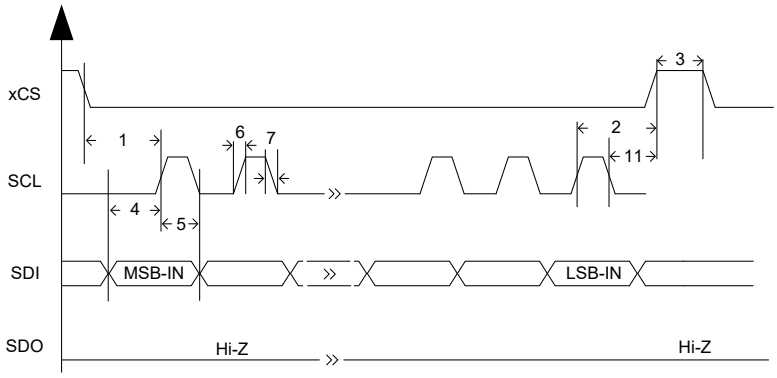
Bit	Meaning	Value and Description
[15:0]	Data	0x0000 to 0xFFFF

Time Characteristics

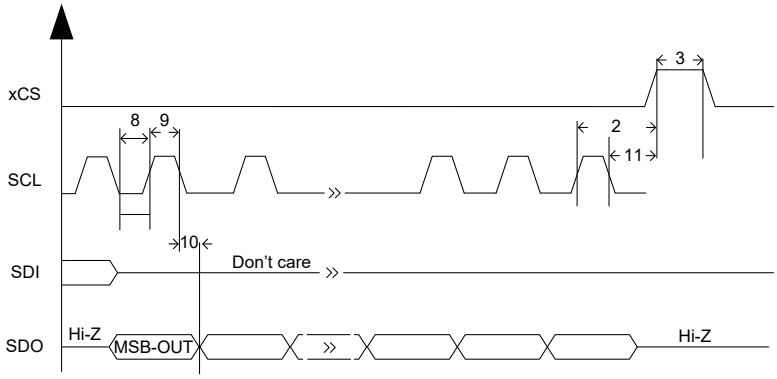
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{CLK}	SCL frequency	0	-	26	MHz
t1	xCS setup time	10	-	-	ns
t2	xCS hold time	10	-	-	ns
t3	xCS disable time	200	-	-	ns
t4	SDI setup time	10	-	-	ns
t5	SDI hold time	10	-	-	ns
t6	SCL rise time	-	-	10	ns
t7	SCL falling time	-	-	10	ns
t8	SCL low time	15	-	-	ns
t9	SCL high time	15	-	-	ns
t10	Output valid from SCL low	-	-	10	ns
t11	SCL falling to xCS rising edge	5	-	-	ns

Timing Characteristics: Shows the timing characteristics of the SPI Interface

SPI Input Timing

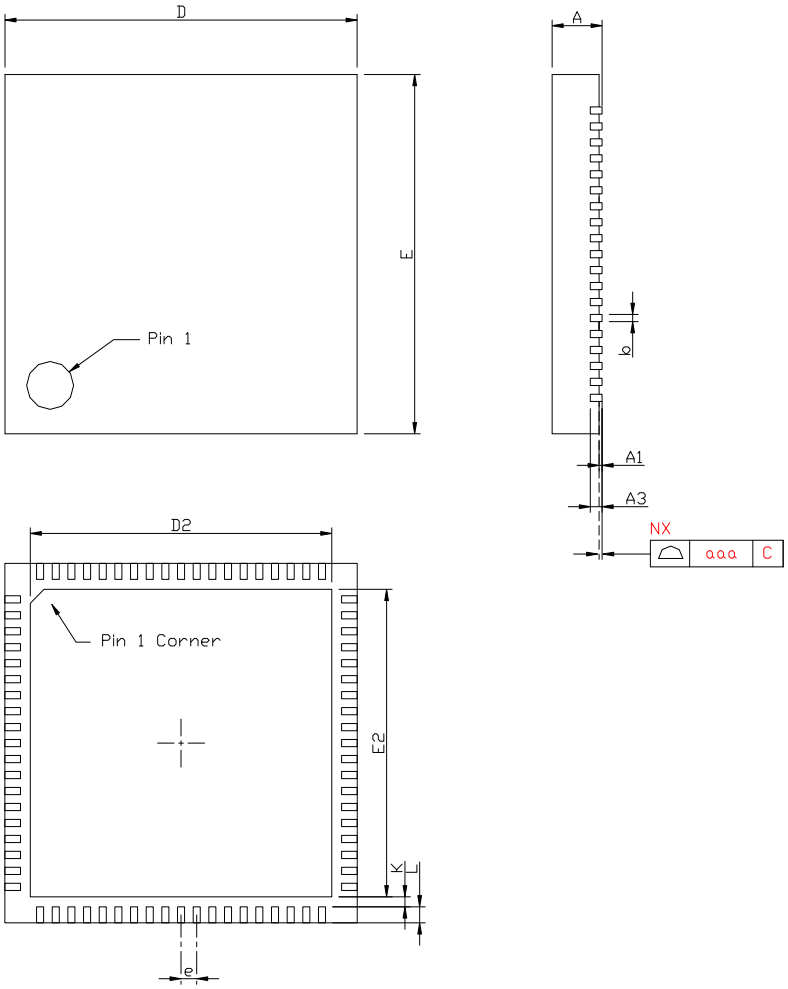


SPI Output Timing



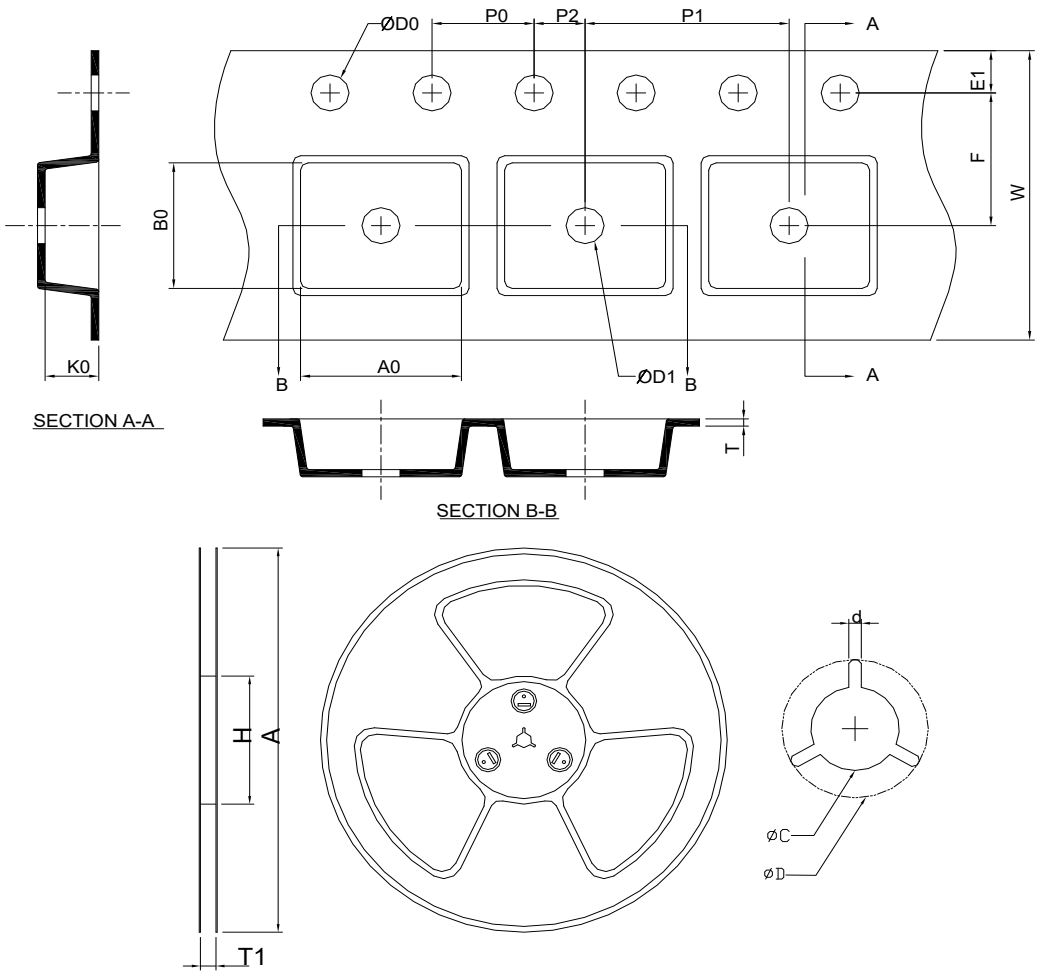
Package Information

QFN9x9-76



SYMBOL	QFN9x9-76			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.13	0.23	0.005	0.009
D	8.90	9.10	0.350	0.358
D2	7.60	7.80	0.299	0.307
E	8.90	9.10	0.350	0.358
E2	7.60	7.80	0.299	0.307
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN 9x9	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.3±0.20	9.30±0.20	9.30±0.20	1.30±0.20

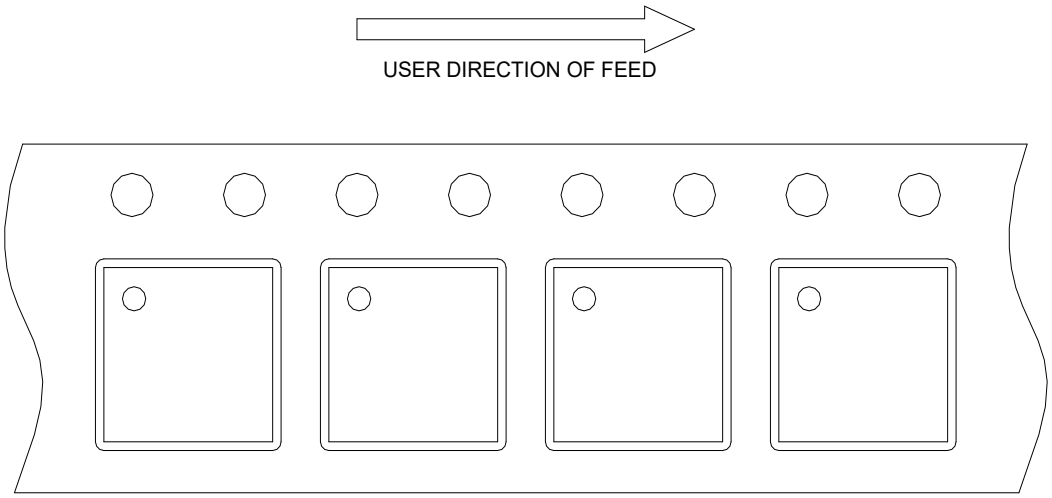
(mm)

Devices Per Unit

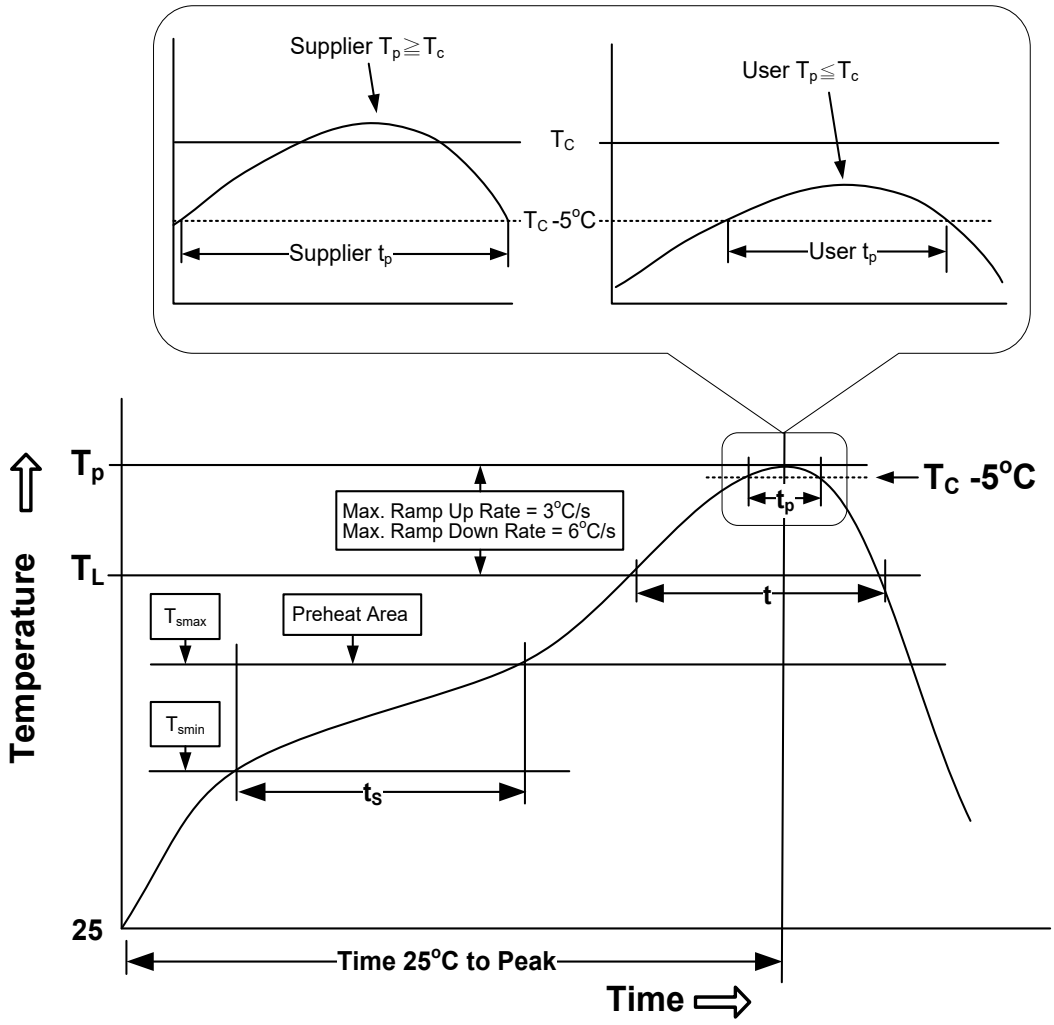
Package type	Packing	Quantity
QFN 9x9	Tape & Reel	2500

Taping Direction Information

QFN9x9-76



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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