Ultra-Low On-Resistance, Power Load Switch with Soft Start

Features

- **7.8mΩ(Typical) On-resistance**
- **Low Quiescent Current: 30μA(max)**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Input Voltage Range (VIN): 0.8V to 5.5V**
- **Supply Voltage Range (VDD): 3V to 5.5V**
- **Enable Control Function**
- **Output Discharge when Switch Disabled**
- **Over-Temperature Protection with Hysteresis**
- **Tiny small TDFN2x2-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APL3529A/B is an ultra-low On-resistance, power-distribution switch with external soft start control.

The APL3529A/B can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V or ENB above 0.8V will shuts off the output.

The device integrates over-temperature protection. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 160°C and will automatically turns on the power switch when the temperature drops by 40°C.

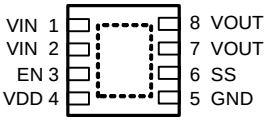
The device is available in lead free TDFN2x2-8 package.

Applications

- **Notebook**
- **AIO PC**

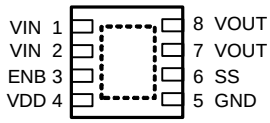
Pin Configurations

APL3529A



TDFN2x2-8
(Top View)

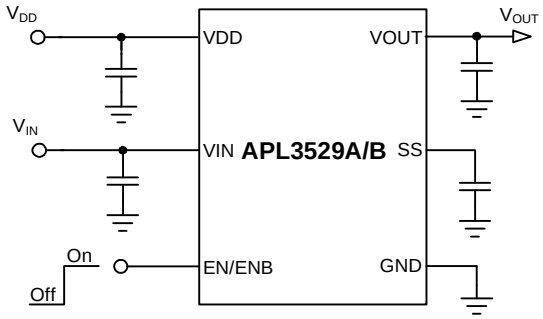
APL3529B



TDFN2x2-8
(Top View)

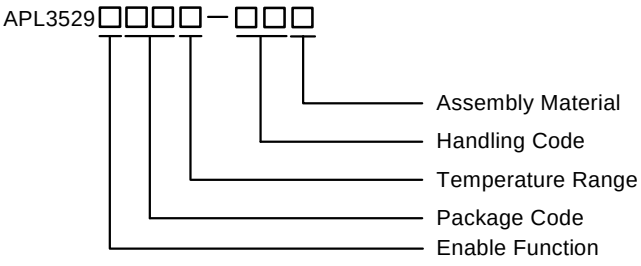
= Exposed Pad (connected to ground plane for better heat dissipation)

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information



Enable Function
A : Active High B: Active Low
Package Code
QB : TDFN2x2-8
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL3529A QB:	L29A • X	X - Date Code
APL3529B QB:	L29B • X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	VDD to GND Voltage	-0.3 ~ 6	V
V_{IN}	VIN to GND Voltage	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 6	V
V_{EN}	EN to GND Voltage	-0.3 ~ 6	V
V_{ENB}	ENB to GND Voltage	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in free air (Note 2) TDFN2x2-8	75	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{DD}	VDD Input Voltage ($V_{DD} \geq V_{IN}$)	3.0 ~ 5.5	V
V_{IN}	VIN Input Voltage	0.8 ~ 5.5	V
I_{OUT}	VOUT Output Current	0 ~ 6	A
	Maximum pulsed switch current, pulse<300μs, 1% duty cycle	8	
V_{IH}	EN/ENB Logic High Input Voltage	0.8 ~ 5.5	V
V_{IL}	EN/ENB Logic Low Input Voltage	0 ~ 0.4	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}= 1.05V, V_{DD}=5V, V_{EN}=5V (or V_{ENB}=0V) and T_A=-40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3529A/B			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
	VDD Supply Current	No load	-	20	30	μA
	VDD Supply Current at Shutdown	No load, V_{DD}=5V, V_{EN}=0V or V_{ENB}=5V	-	-	1	μA
	VIN Supply Current	No load	-	10	20	μA
	VIN Off-State Supply Current	No load, V_{DD}=5V, V_{IN}=5V, V_{EN}=0V or V_{ENB}=5V	-	0.1	10	μA
		No load, V_{DD}=5V, V_{IN}=3.3V, V_{EN}=0V or V_{ENB}=5V	-	0.1	5	μA
		No load, V_{DD}=5V, V_{IN}=1.8V, V_{EN}=0V or V_{ENB}=5V	-	0.1	2	μA
		No load, V_{DD}=5V, V_{IN}=0.8V, V_{EN}=0V or V_{ENB}=5V	-	0.1	1	μA
	VOUT Leakage Current	V_{OUT}=0V, V_{EN}=0V or V_{ENB}=5V	-	0.1	7	μA
	Reverse Leakage Current	V_{EN}=0V or V_{ENB}=5V, V_{OUT}=5.5V, V_{IN}=0V,	-	0.1	16	μA
UNDER-VOLTAGE LOCKOUT (UVLO)						
	Rising VDD UVLO Threshold	V_{DD} rising, T_J=25°C	1.9	2.4	2.9	V
	VDD UVLO Hysteresis		-	0.1	-	V
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	V_{DD}=5V, I_{OUT}=6A, T_A=25°C	-	7.8	9.5	mΩ
		V_{DD}=3.3V, I_{OUT}=6A, T_A=25°C	-	8.6	10.5	
	VOUT Discharge Resistance	V_{EN}=0V or V_{ENB}=5V, VOUT force 1V	-	100	150	Ω

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}= 1.05V, V_{DD}=5V, V_{EN}=5V (or V_{ENB}=0V) and T_A=-40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3529A/B			Unit
			Min	Typ	Max	
SOFT-START CONTROL PIN						
	SS Discharge Resistance	V_{SS}=6V, V_{EN}=0V or V_{ENB}=5V, measured at SS	-	10	-	kΩ
EN OR ENB INPUT PIN						
	Input Logic HIGH		0.8	-	-	V
	Input Logic Low		-	-	0.4	V
	Input Current	V_{EN}=5.5V or V_{ENB}=5.5V	-	-	1	µA
$t_{D(ON)}$	Turn On Delay Time	C_{SS}=0nF, C_L=0.1µF, R_L=10Ω, From being enabled to VOUT rising	-	5	-	µs
$t_{D(OFF)}$	Turn Off Delay Time	C_{SS}=0nF, C_L=0.1µF, R_L=10Ω	-	2	-	µs
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Protection	T_J rising	-	160	-	°C
	Over-Temperature Protection Hysteresis		-	40	-	°C

Timing Chart

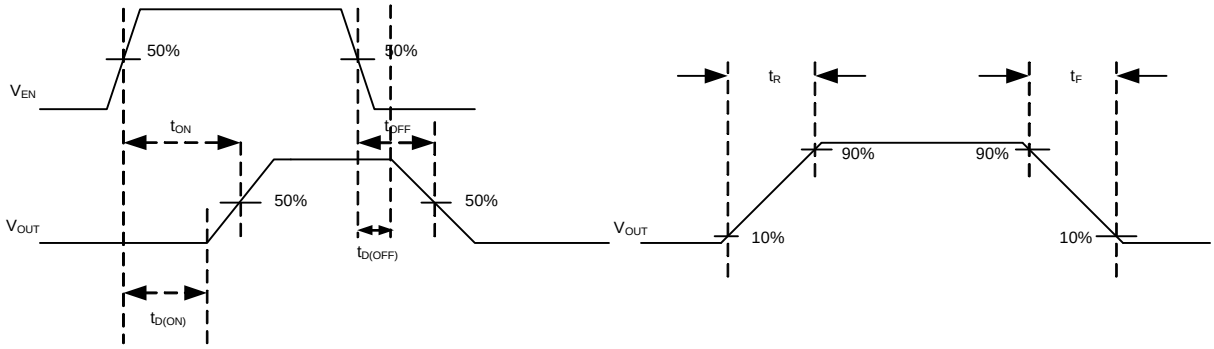


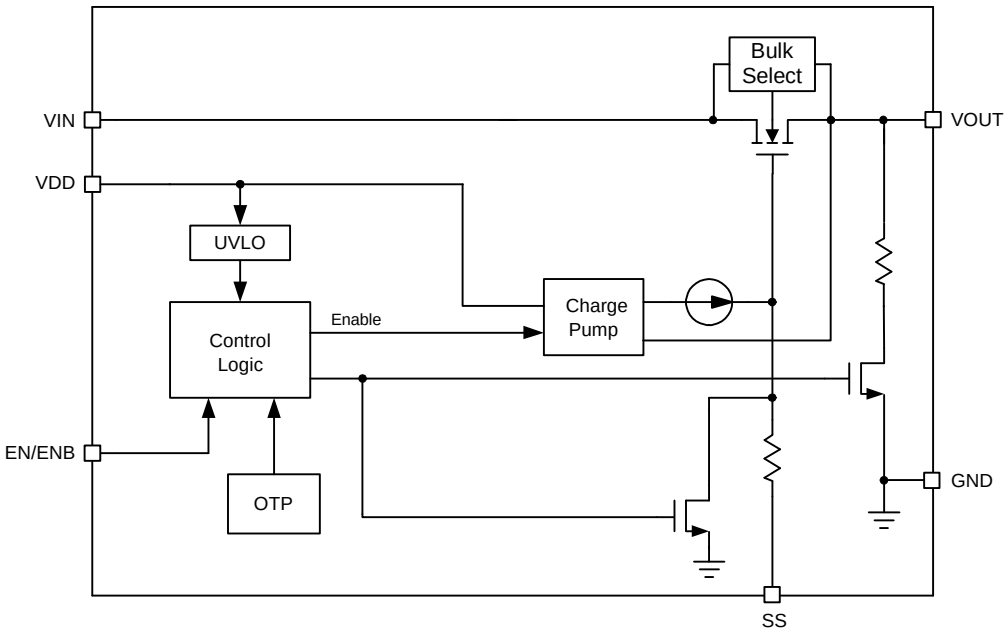
Figure 1. $t_{D(ON)}/t_{D(OFF)}$, t_{ON}/t_{OFF}, t_R/t_F Waveforms

Note4: t_{rise} and t_{fall} of the control signal is 100ns.

Pin Description

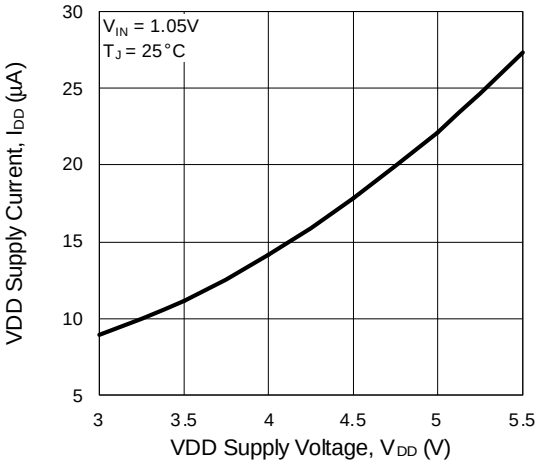
PIN		Function
NO.	NAME	
1, 2	VIN	Power supply Input of switch. Connect this pin to an external DC supply.
3	EN	Enable input of switch. Logic high turns on switch. The EN pin cannot be left floating.
	ENB	Enable input of switch. Logic low turns on switch. The ENB pin cannot be left floating.
4	VDD	VDD voltage input pin for internal control circuitry. Connecting this pin to a 5V or 3.3V supply voltage provides the bias for the control circuitry and charge pump.
5	GND	Power supply Input of switch. Connect this pin to an external DC supply.
6	SS	Soft start control of switch. A capacitor from this pin to ground sets the VOUT' s rise slew rate.
7, 8	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When EN is low or ENB is high, the output voltage is discharged by an internal resistor.
Exposed Pad	GND	Ground pin of the circuitry.

Block Diagram

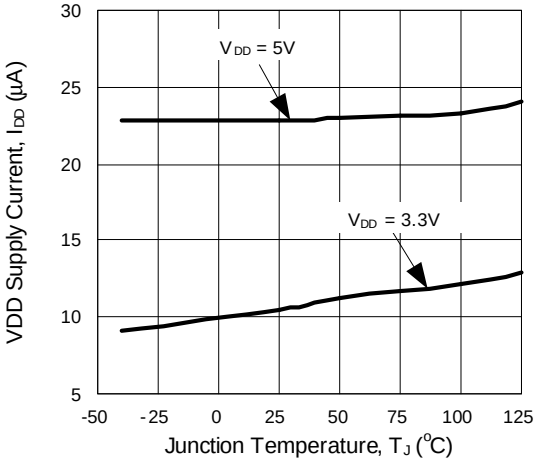


Typical Operating Characteristics

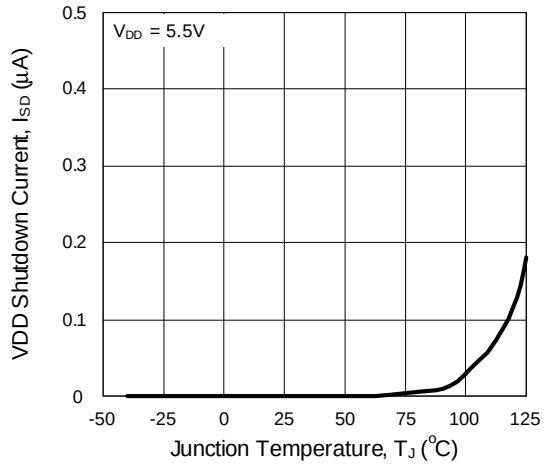
VDD Supply Current vs. VDD Supply Voltage



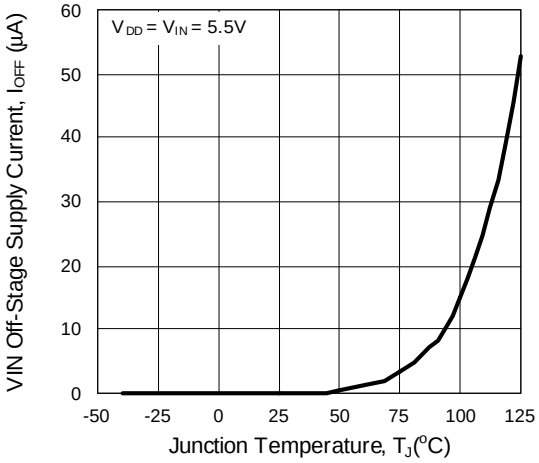
VDD Supply Current vs. Junction Temperature



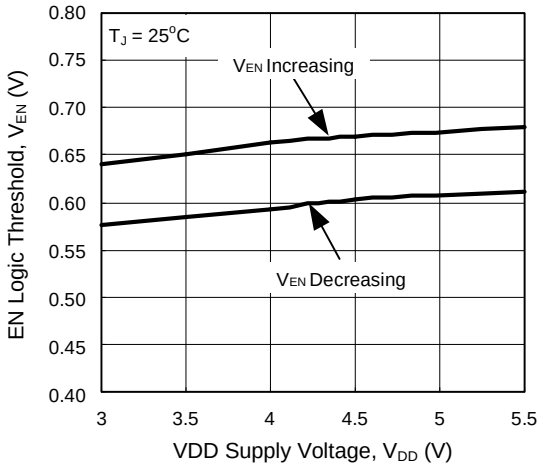
VDD Shutdown Current vs . Junction Temperature



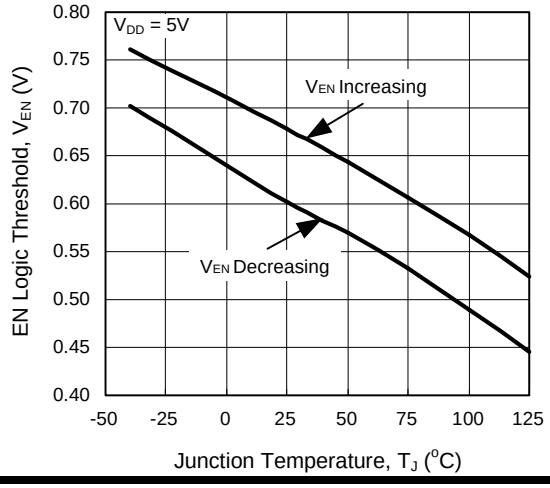
VIN Off-Stage Supply Current vs. Junction Temperature



EN Logic Threshold vs. VDD Supply Voltage

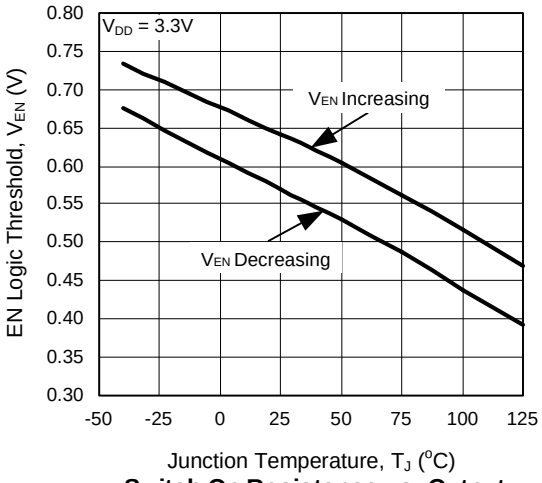


EN Logic Threshold vs. Junction Temperature

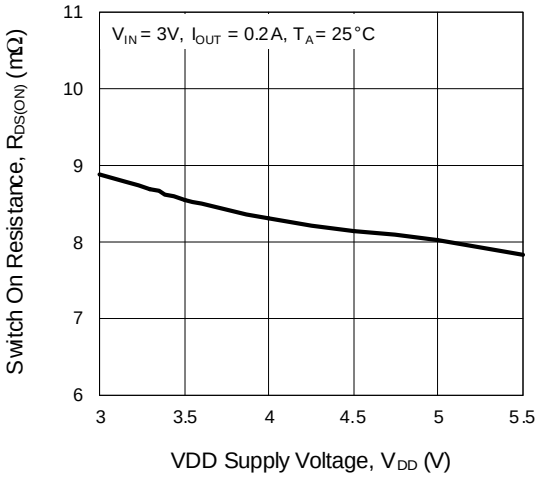


Typical Operating Characteristics

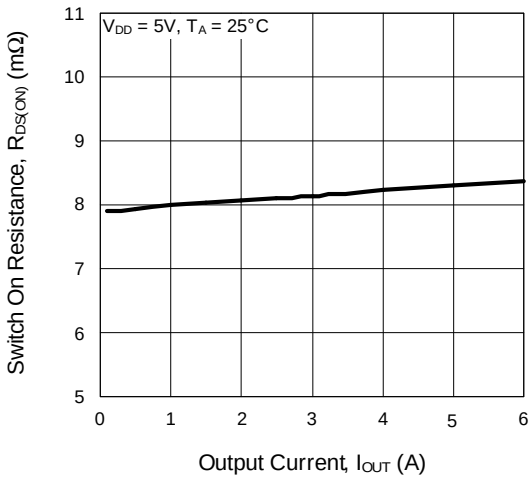
EN Logic Threshold vs. Junction Temperature



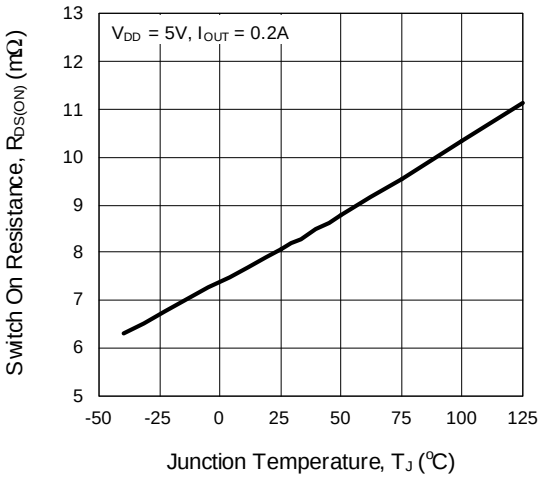
Switch On Resistance vs. VDD Supply Voltage



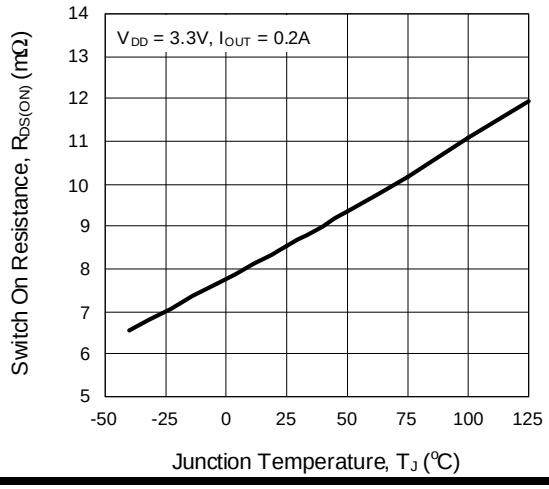
Switch On Resistance vs. Output Current



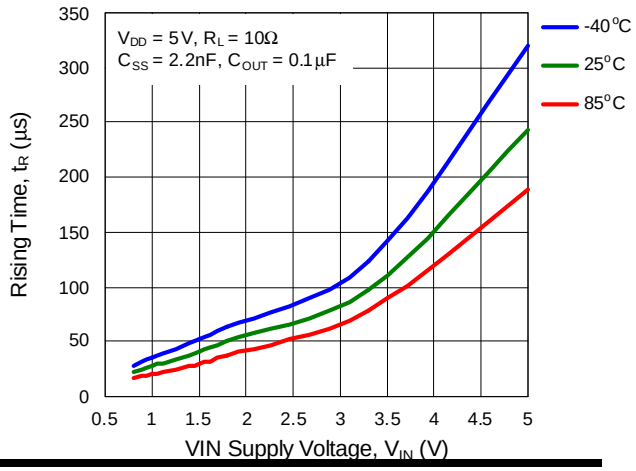
Switch On Resistance vs. Junction Temperature



Switch On Resistance vs. Junction Temperature

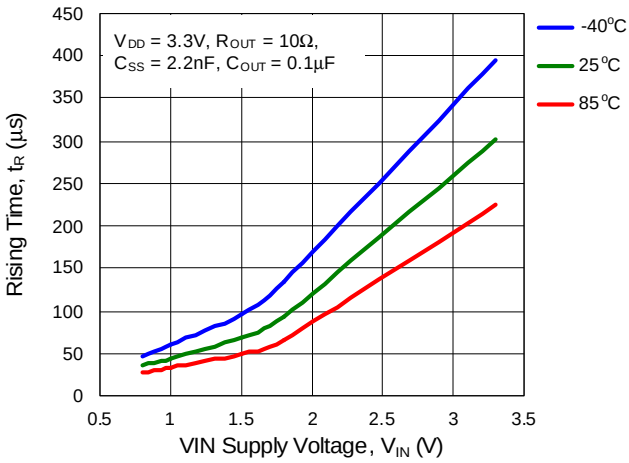


Rising Time vs. VIN Supply Voltage

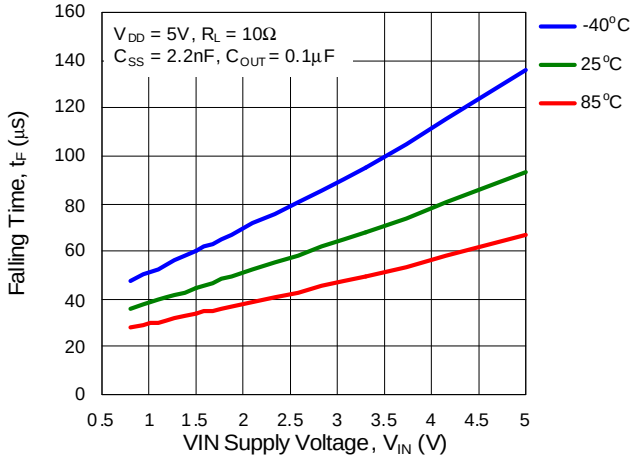


Typical Operating Characteristics

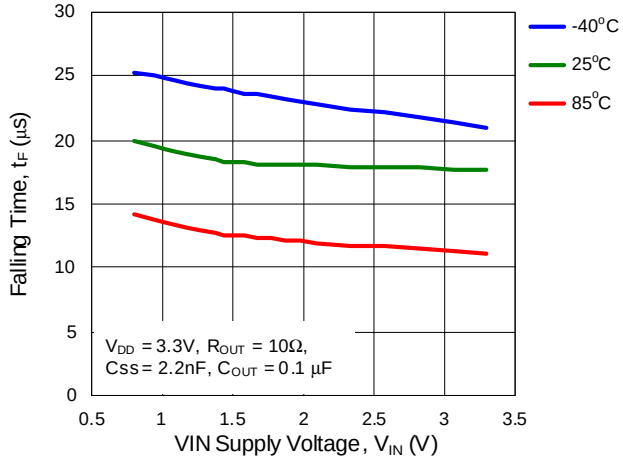
Rising Time vs. VIN Supply Voltage



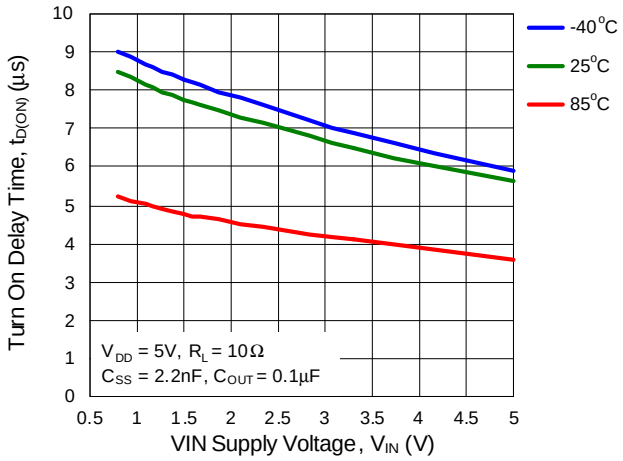
Falling Time vs. VIN Supply Voltage



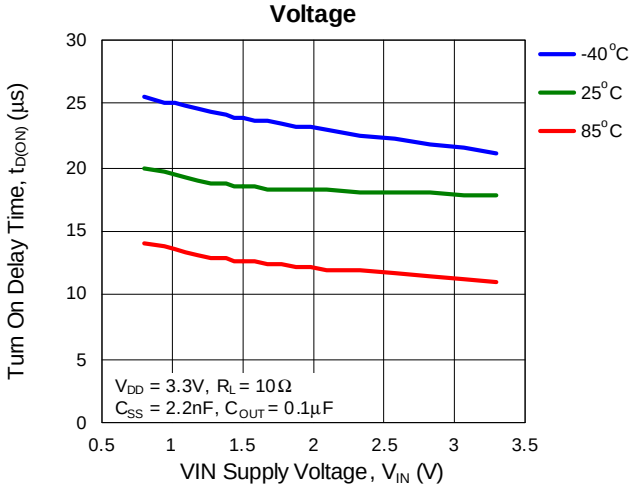
Falling Time vs. VIN Supply Voltage



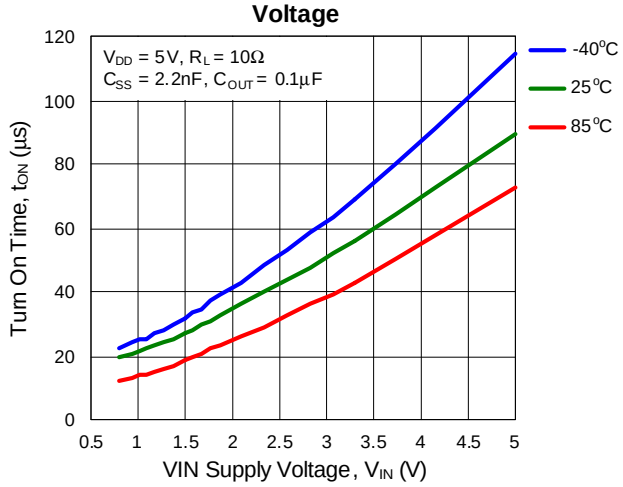
Turn On Delay Time vs. VIN Supply Voltage



Turn On Delay Time vs. VIN Supply Voltage

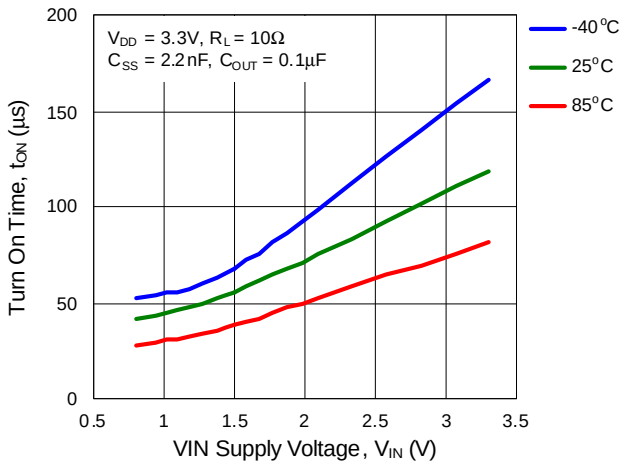


Turn On Time vs. VIN Supply Voltage

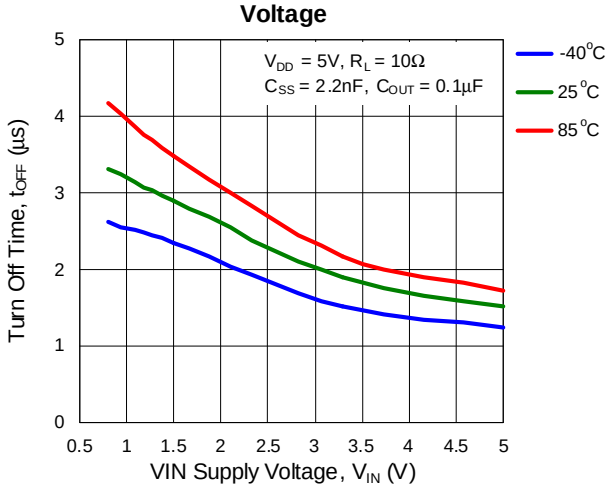


Typical Operating Characteristics

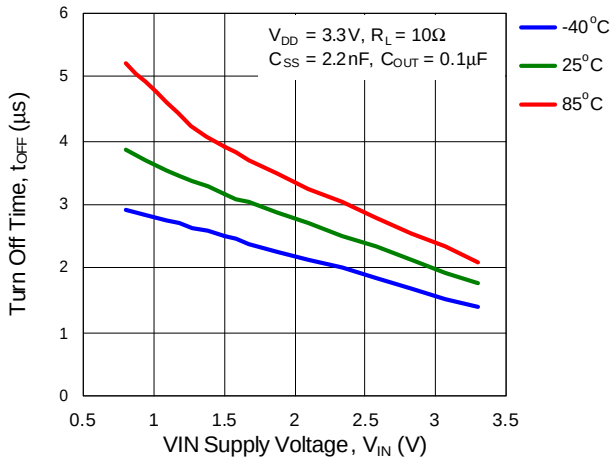
Turn On Time vs. VIN Supply Voltage



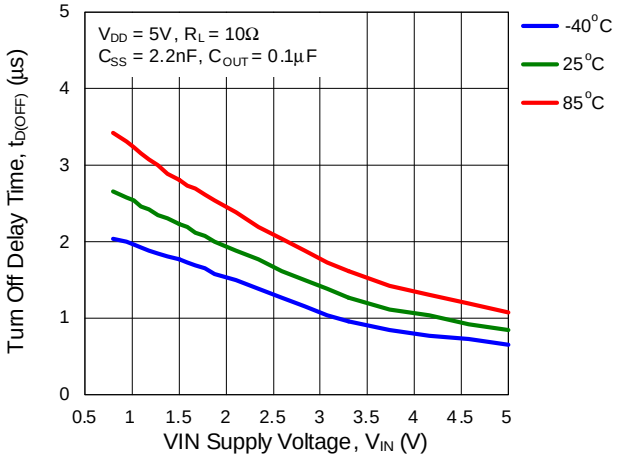
Turn Off Time vs. VIN Supply Voltage



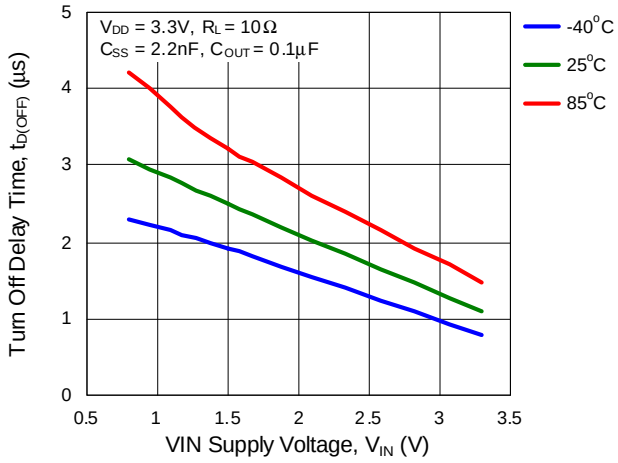
Turn Off Time vs. VIN Supply Voltage



Turn Off Delay Time vs. VIN Supply Voltage



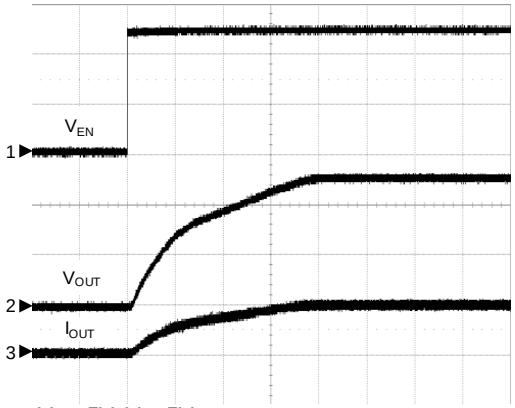
Turn Off Delay Time vs. VIN Supply Voltage



Operating Waveforms

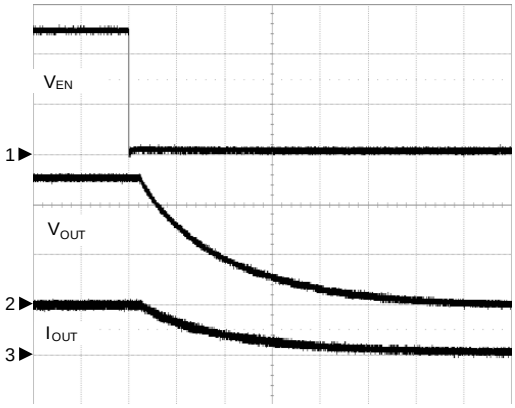
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

Enable



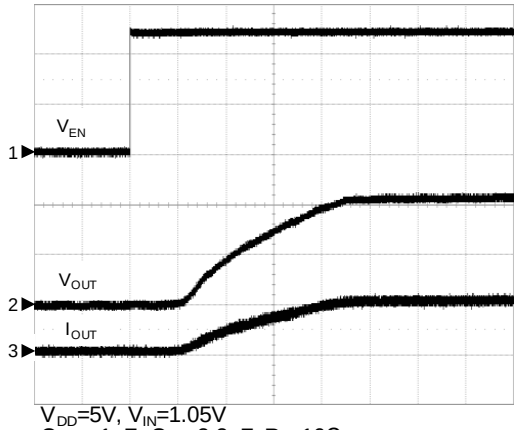
V_{DD}=5V, V_{IN}=5V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 500mA/Div, DC
TIME:100µs/Div

Shutdown



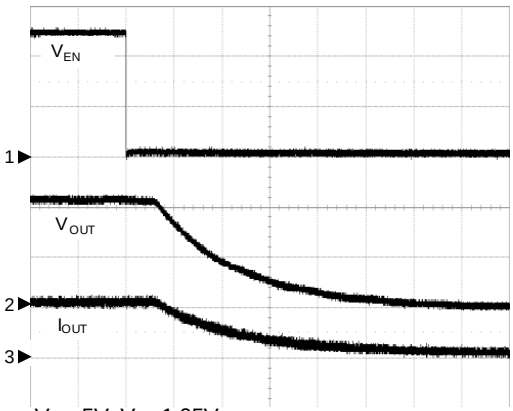
V_{DD}=5V, V_{IN}=5V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 500mA/Div, DC
TIME: 5µs/Div

Enable



V_{DD}=5V, V_{IN}=1.05V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 10µs/Div

Shutdown

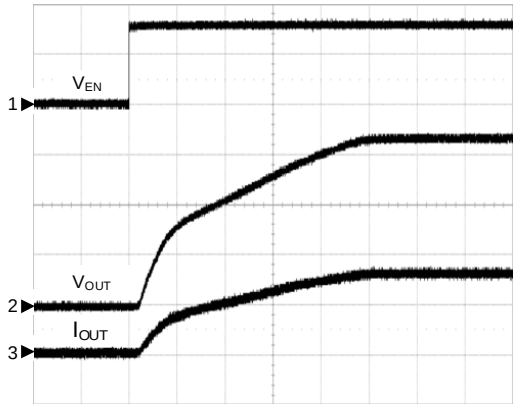


V_{DD}=5V, V_{IN}=1.05V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 5µs/Div

Operating Waveforms

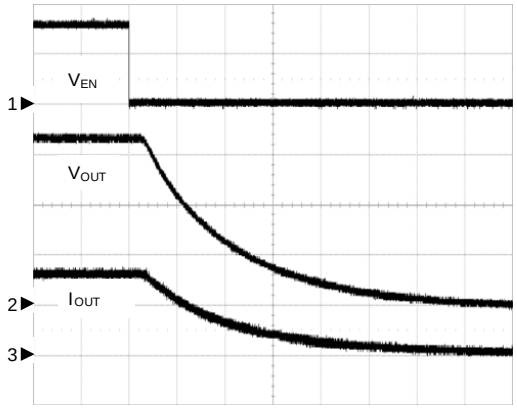
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

Enable



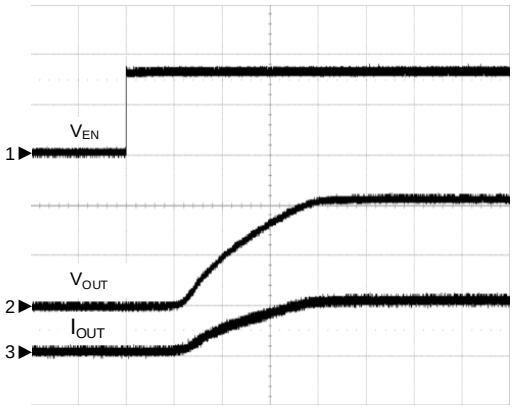
V_{DD}=3.3V, V_{IN}=3.3V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: I_{OUT}, 200mA/Div, DC
TIME: 100µs/Div

Shutdown



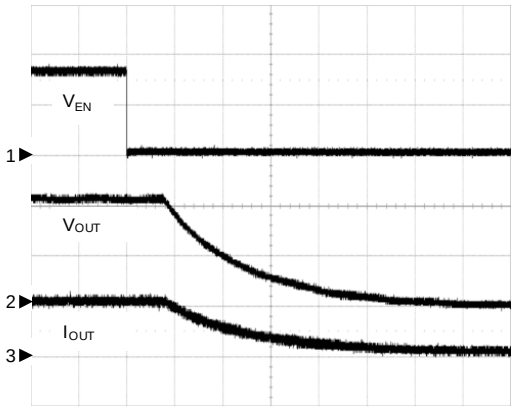
V_{DD}=3.3V, V_{IN}=3.3V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: I_{OUT}, 200mA/Div, DC
TIME: 5µs/Div

Enable



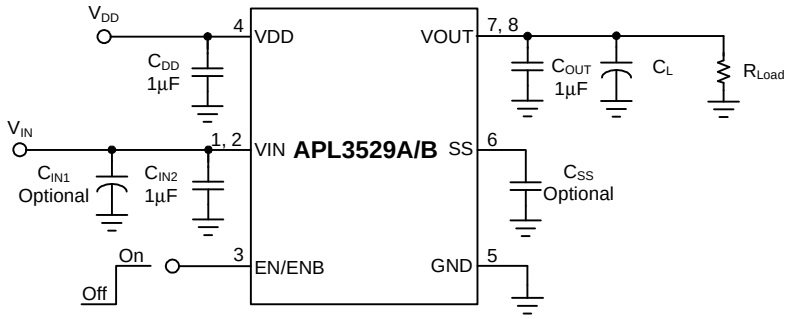
V_{DD}=3.3V, V_{IN}=1.05V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 20µs/Div

Shutdown



V_{DD}=3.3V, V_{IN}=1.05V
C_{OUT}=1µF, C_{SS}=2.2nF, R_L=10Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 5µs/Div

Typical Application Circuit



Css (nF)	Soft-Start Time (µs) 10% to 90%, V_{DD}=5V, C_{IN}=1µF, C_{OUT}=1µF, C_L=0.1µF, R_L=10Ω, Typical values are at T_A=25°C.						
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.8V
0	26.9	15.2	9.6	8.1	7.2	7.1	6.1
1	120	47	24	20	16	15	12
2.2	236	87	40	33	26	24	18
3.3	355	117	55	48	34	32	24
4.7	518	182	77	60	48	41	31
10	1077	358	158	124	88	75	54
33	3593	1118	479	374	281	222	139
47	4714	1686	691	546	377	330	213
100	11050	3837	1582	1213	875	696	418

Css (nF)	Soft-Start Time (µs) 10% to 90%, V_{DD}=3.3V, C_{IN}=1µF, C_{OUT}=1µF, C_L=0.1µF, R_L=10Ω, Typical values are at T_A=25°C.						
	-	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.8V
0	-	40.1	17.0	15.9	12.5	11.4	10.6
1	-	169	44	31	26	22	18
2.2	-	325	81	54	41	35	26
3.3	-	492	126	84	60	52	38
4.7	-	680	177	109	81	68	52
10	-	1406	363	230	161	139	103
33	-	4509	1042	664	512	445	306
47	-	6201	1559	1026	743	621	462
100	-	14750	3628	2159	1630	1383	1017

Note5: The table Contains soft-start time values measured on a typical device. The soft-start times shown are only valid for the power-up sequence where V_{IN} and V_{DD} are already in steady state condition, and EN pin is asserted high.

Typical Application Circuit

Css (nF)	Turn On Delay Time (μs), V_{DD}=5V, C_{OUT}=1μF, C_{IN}=1μF, C_L=0.1μF, R_L=10Ω, Typical values are at T_A=25°C.						
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.8V
0	3.75	4.15	4.79	4.95	4.97	5.01	5.21
1	4.65	5.25	6.42	6.65	6.71	6.77	6.82
2.2	4.72	5.32	6.13	6.37	6.71	6.93	7.05
3.3	5.05	5.82	6.12	6.85	7.12	7.45	7.54
4.7	5.13	5.93	6.44	6.66	7.06	7.46	7.86
10	5.37	6.58	6.97	7.37	7.68	7.77	8.17
33	5.81	7.41	8.61	9.01	9.41	9.60	9.80
47	6.21	7.64	8.45	8.58	9.35	9.38	10.18
100	7.08	8.29	9.09	9.89	10.29	10.68	11.09

Css (nF)	Turn On Delay Time (μs), V_{DD}=3.3V, C_{OUT}=1μF, C_{IN}=1μF, C_L=0.1μF, R_L=10Ω, Typical values are at T_A=25°C.						
	-	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.8V
0	-	7.35	8.15	8.44	8.69	8.98	9.09
1	-	12.60	13.40	14.20	14.51	14.99	15.00
2.2	-	14.66	16.67	17.85	17.97	18.03	18.66
3.3	-	19.06	19.88	20.68	21.62	21.97	22.26
4.7	-	18.26	20.66	22.26	23.06	23.88	24.66
10	-	19.50	21.14	23.54	25.14	25.94	26.74
33	-	21.94	23.12	24.34	25.94	27.54	28.34
47	-	22.18	23.02	23.43	24.07	24.56	26.38
100	-	23.11	24.22	24.73	25.13	25.91	26.48

Function Description

VIN Under-voltage Lockout (UVLO)

A Under-Voltage Lockout (UVLO) circuit monitors the VDD pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the VDD supply voltages exceed rising UVLO voltage threshold during powering on.

Power Switch

The power switch is an N-channel MOSFET with a ultra-low $R_{DS(ON)}$. When IC is in shutdown state (V_{EN}=0V), the MOSFET prevents a reverse current flowing from the VOUT back to VIN. When IC is in UVLO state, the internal parasitic diodes connected from VOUT to VIN will be forward biased.

Soft-start

The APL3529A/B Provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground.

Enable Control

The APL3529A/B has a dedicated enable pin (EN or ENB). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high (EN) or low (ENB) signal re-enables the output through initiation of a new soft-start cycle.

Over-Temperature Protection (OTP)

When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Power Sequencing

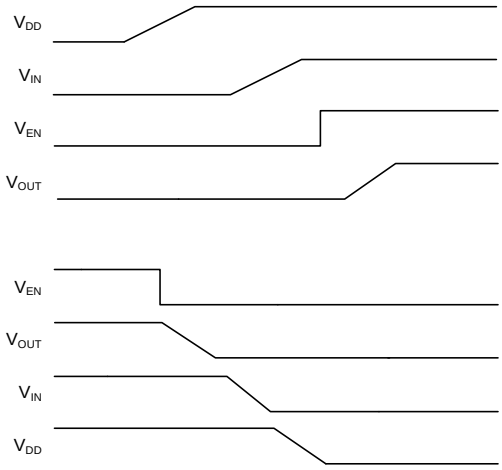


Figure 2. APL3529A/B Power Sequencing Diagram

The APL3529A/B has a built-in reverse current blocking circuit to prevent a reverse current flowing through the body diode of power switch from the VOUT back VIN pin when power switch disabled. The reverse current blocking circuit is not active before V_{DD} is ready. When IC is in UVLO state, the internal parasitic diodes of power switch connected from VOUT to VIN will be forward biased. Otherwise, VOUT should not be higher than VDD, and VDD must be higher than the voltage of any other input pin, the reason is that the internal parasitic diodes connected from VOUT to VDD will be forward biased.

Capacitor Selection

The APL3529A/B requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

For normal applications (except OTP or output short circuit has occurred), the recommended input capacitance of VIN is 1μF at least. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during load transient conditions. The output capacitance of VOUT is 1μF at least. Please place the capacitors near the APL3529A/B as close as possible.

A bulk output capacitor, placed close to the load, is recommended to support load transient current.

Thermal Consideration

The APL3529A/B maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air.

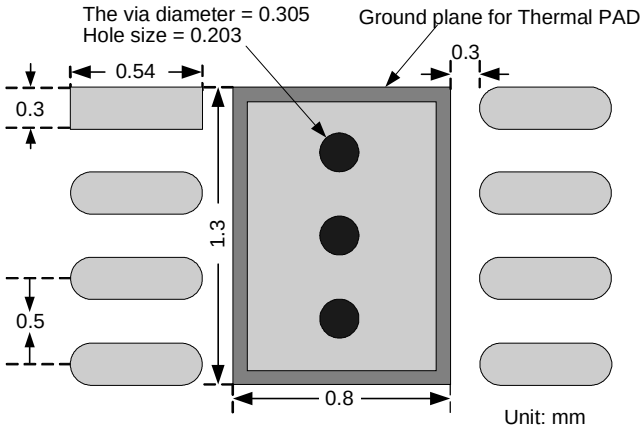
Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3529A/B and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep VIN and VOUT traces as wide and short as possible.

Application Information

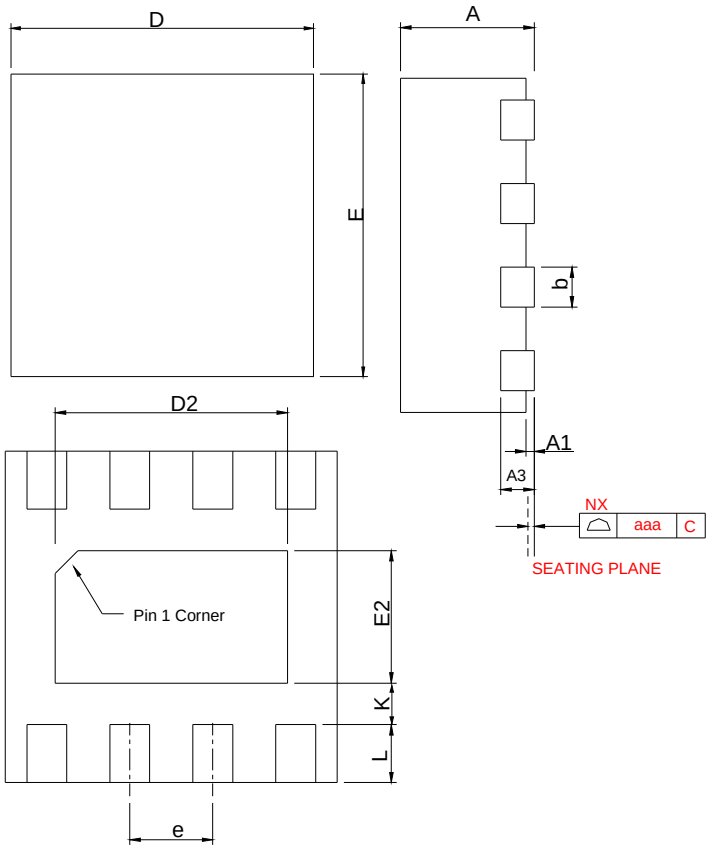
Recommended Minimum Footprint



TDFN2x2-8

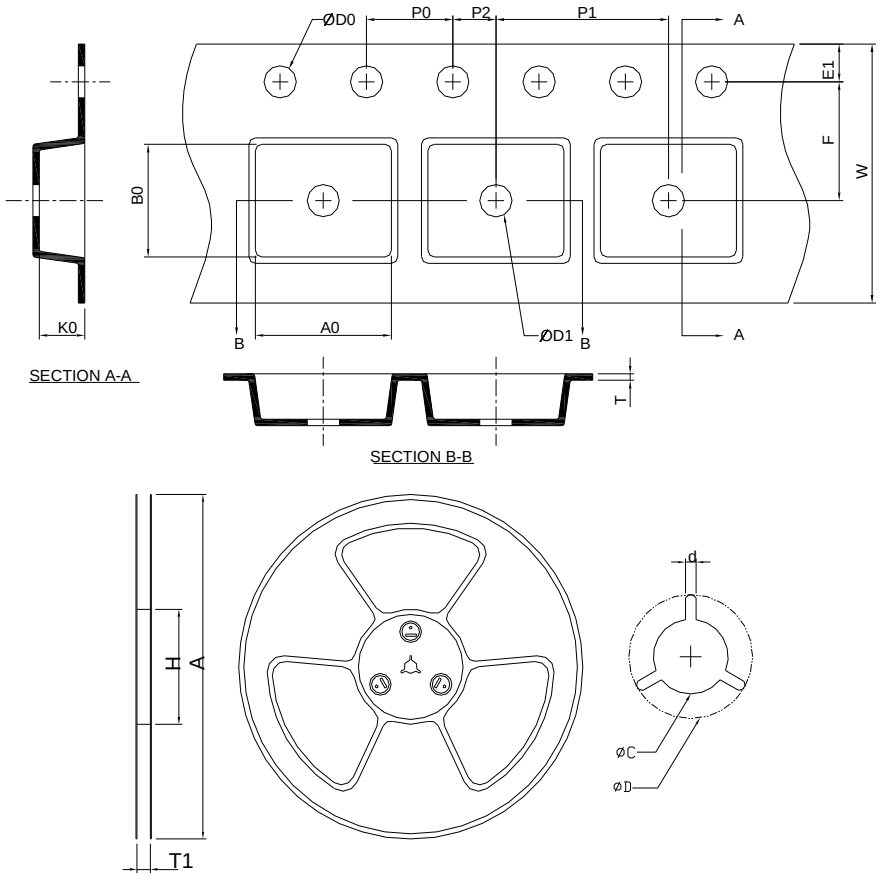
Package Information

TDFN2x2-8



SYMBOL	TDFN2x2-8					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.035	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.00	1.10	1.20	0.039	0.043	0.047
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.70	0.80	0.90	0.028	0.031	0.035
e	0.50 BSC			0.020BSC		
L	0.30	0.38	0.45	0.012	0.015	0.018
K	0.20			0.008		
aaa	0.08			0.003		

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	2.35 ±0.20	2.35 ±0.20	1.00±0.20

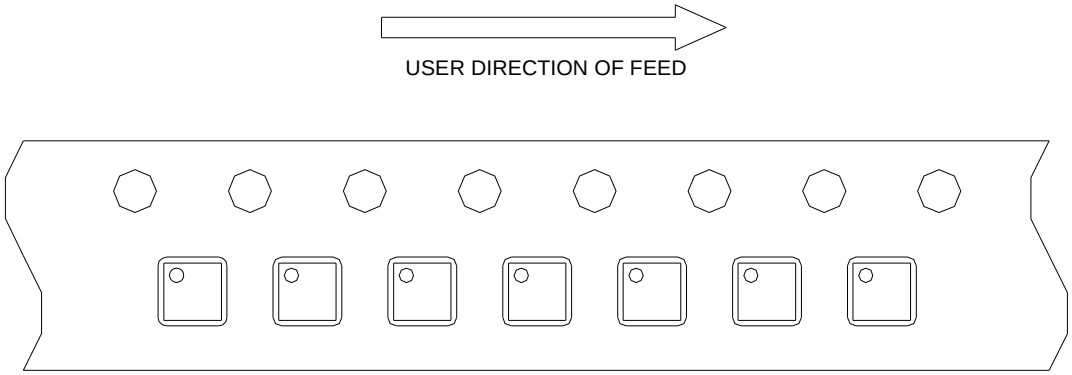
(mm)

Devices Per Unit

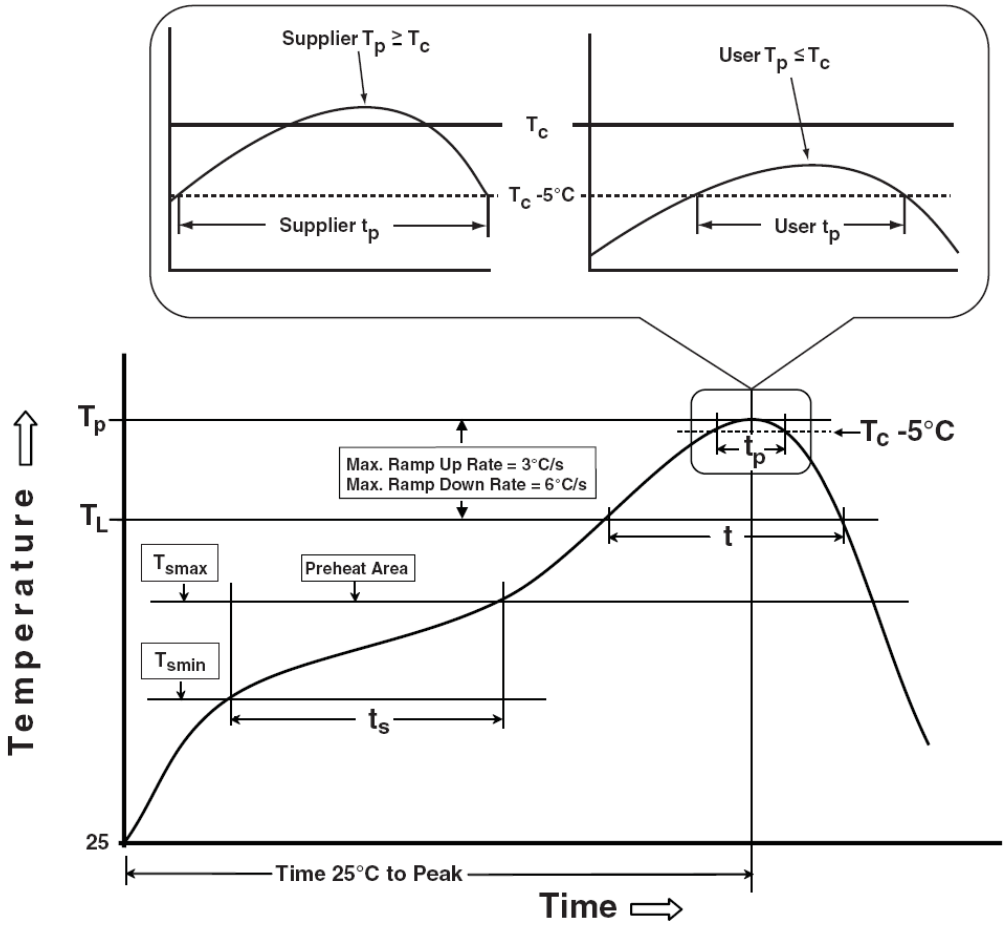
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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