USB Power-Distribution Switches

Features

- **VIN Input Voltage Range: 4.5 to 25V**
- **30V Absolute Ratings at VIN Pin**
- **15A Output Current Capability**
- **Adjustable Soft-start Time by SS pin**
- **Fast Over Current Protection Response Time**
- **Wrong VIN Input Voltage Protection**
- **Fault Report on ACOK Pin**
- **Built-in Surge Protection when Surge Voltage over 27V**
- **Built-in Thermal Shutdown Protection**
- **Built-in Enable / Shutdown Control by DPREN Pin**
- **Integrated Internal Charge Pump**
- **Built-in Programmable Short Circuit or Over Current Protection Threshold Setting by ALSET pin**
- **ESD Protection:**
  - EC61000-4-2 contact discharge over with 8kV
  - HBM with over 2kV
  - CDM with over 500V at VIN pin
- **Over-Temperature Protection**
- **TQFN4x4-24 Package**

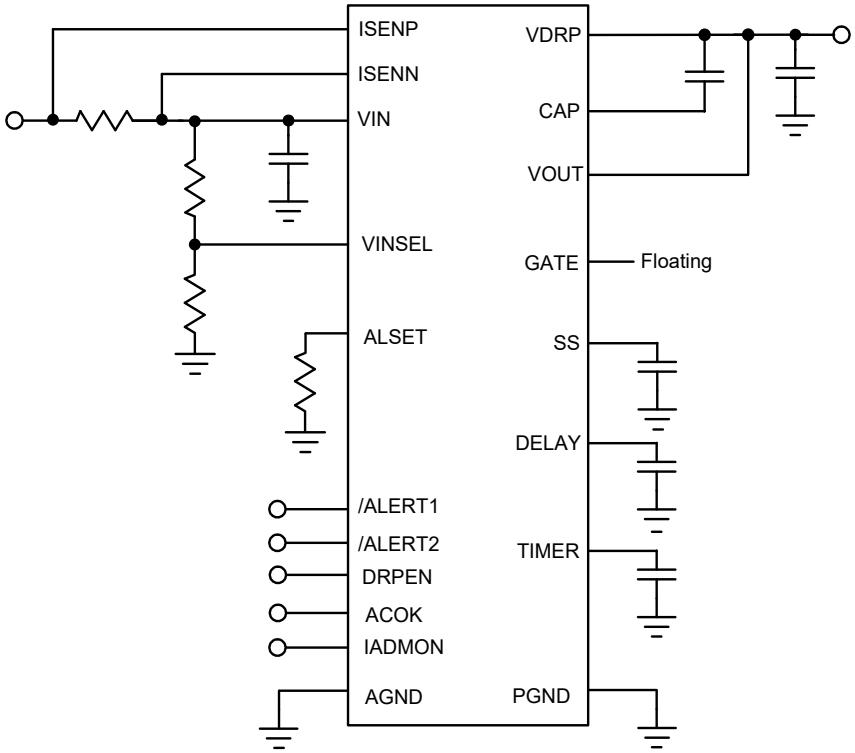
General Description

The APL3576A is designed for desktop adapter applications.
The low on resistance N-channel MOSFET power switch can satisfy the voltage drop requirements of USB specification.
Protection features include current-limit protection, short-circuit protection, over-temperature protection, wrong VIN input voltage protection, surge protection, and reverse current blocking.
Other features include a deglitched ACOK output to indicate the fault condition and an enable input to enable or disable the device.

Applications

- **Notebook and Desktop Computers**
- **High-side Power Protection Switches**

Simplified Application Circuit

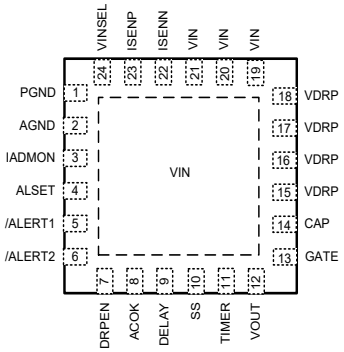


Ordering and Marking Information

APL3576A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-24F Operating Ambient Temperature Range I : -40 to 85 ℃ Handling Code TR : Tape & Reel Lead Free Code G : Green Part
APL3576A QB : A APL3576 XXXXX	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



TQFN4*4-24

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
VIN, VDRP, VOUT	VIN, VDRP, VOUT to GND	-0.3 ~ 30	V
VISENP/N	VISENP/N to GND	-0.3 ~ 30	V
VOUT, GATE	VOUT, VGATE to GND	-0.3 ~ 30	V
VVINSEL	VVINSEL to GND	-0.3 ~ 30	V
VDRPEN	DRPEN to GND	-0.3 ~ 30	V
V I/O	/ALERT1/2, ACOK, ALSET, IADMON.DELAY, TIMER, SS, CAP to GND Voltage	-0.3 ~ 6	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	25	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 2)	7	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 25	V
I_{DUT}	Output Current (continue)	0 ~ 15	A
C_{IN}	Input Capacitor range	22 ~ 100	µF
C_{OUT}	Output Capacitor range	20 ~ 100	µF
C_{SS}	SS pin external capacitor range	2.2 ~ 15	nF
C_{TIMER}	TIMER pin external capacitor range	10 ~ 100	nF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=20V, V_{DRPEN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APL3576A			
			Min.	Typ.	Max.	Unit
Supply Power						
V_{IN}	VIN Input Voltage		4.5	-	25	V
I_{VIN}	VIN Supply Current	No Load, VDRPEN=0V	-	40	-	μA
		No Load, VDRPEN=5V	-	300	-	μA
I_{VIN_OFF}	VDRP Off State Leakage Current	VIN=20V, VDRP=GND, VDRPEN=0V, TA=25°C	-	-	4	μA
Power On Reset (POR)						
V_{IN_UVLO}	Rising VIN POR Voltage	VIN Rising	3.6	3.8	4	V
	VIN UVLO Hysteresis		-	0.2	-	V
DRPEN Input Voltage						
V_{DRPEN}	Input Logic High		1.2	-	-	V
	Input Logic Low		-	-	0.5	V
	Inpur Current	VDRPEN=5V	-	-	1	μA
Soft Start Setup						
I_{SS}	SS Source Current		-	6	-	μA
$T_{D(ON)}$	Turn On Delay Time	Cout=0.1uF, CSS=Open	-	200	-	μs
$T_{D(OFF)}$	Turn Off Delay Time	Cout=0.1uF, CSS=Open	-	5	-	μs
T_{SS}	Soft Start Time	No Load, Vin=20V, Cout=10uF, CSS=2.7nF, Vout=10 to 90%	-	1	-	ms
		No Load, Vin=20V, Cout=10uF, CSS=Open, Vout=10 to 90%	-	230	-	μs
Power Switch Resistance						
$R_{DS(ON)}$	Power Switch On Resistance	Iout=5A, at 25 degree	-	7	10	mΩ
R_{DIS}	Discharge Resistance	VDRP Pin	-	600	-	Ω
Thermal Protection						
T_{SD}	Thermal Shutdown Threshold		-	150		°C
	Thermal Shutdown Hysteresis		-	30	-	°C
Wrong VIN Input Voltage Protection $ Surge Protection						
$V_{VINSEL(L)}$	VINSEL Low Detection Rising Vth	VVINSEL Rising, IC is On	0.7125	0.75	0.7875	V
	VINSEL Low Detection Falling Vth	VVINSEL Falling, IC is Latch Off	0.665	0.7	0.735	V
$V_{VINSEL(H)}$	VINSEL High Detection Rising Vth	VVINSEL Rising, IC is Off	1.045	1.1	1.155	V
	VINSEL High Detection Falling Vth	VVINSEL Falling, IC is On	0.95	1	1.05	V
	VINSEL Input Current	VVINSEL=25V	-	-	1	μA
V_{SURGE}	VIN Surge Protection Threshold		-	27	-	V
ACOK and /ALERT1/2 Output Pin						
	Output Low Voltage	Input current=5mA	-	-	0.4	V
	Leakage Current	Input Voltage=5V, MOS off	-	-	1	μA
	ALERT2 Debounce Time	Only for Alert2	-	1.15	-	ms
	ALERT2 Release Time	Only for Alert2	-	72	-	ms

Electrical Characteristics (Cont.)

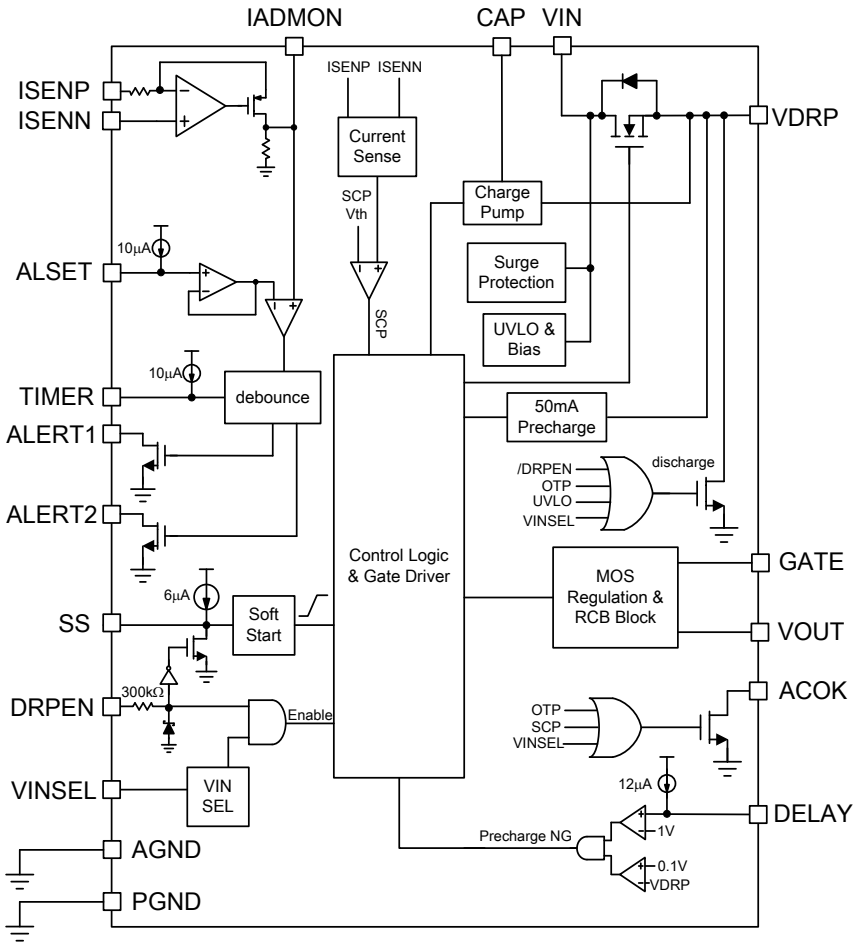
Unless otherwise specified, these specifications apply over V_{IN}=20V, V_{DRPEN}=5V and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Condition	APL3576A			
			Min.	Typ.	Max.	Unit
Input Current Report						
K	ISENP to ISENN Differential Voltage to IADMON Vltage Gain	VIN=20V	-	20	-	V/V
	IADMON Voltage Accuracy	VIN=20V, RSENSE=5mΩ, Load=5A	-3	-	3	%
		VIN=20V, RSENSE=5mΩ, Load=15A	-3	-	3	%
		VIN=20V, RSENSE=3mΩ, Load=5A	-6	-	6	%
		VIN=20V, RSENSE=3mΩ, Load=15A	-3	-	3	%
	IADMON Driving Capability		-	100	-	μA
I_{ALSET}	ALSET Internal Pull High Current	VALSET=1V	-	10	-	μA
I_{TIMER}	Timer Internal Pull High Current		-	10	-	μA
$V_{/ALERT1}$	/ALERT1 Threshold	VIADMON/V/ALSET1	-	1	-	V/V
$V_{/ALERT2}$	/ALERT2 Threshold	VIADMON/V/ALSET2	-	1.15	-	V/V
Reverse Current Block						
	Reverse Current Block Threshold	VOUT-VDRP	-	10	-	mV
	VDRP to Vout Regulation Voltage	VDRP-VOUT	-	20	-	mV
Over Current Protection						
I_{SCP}	Short Circuit Protection Threshold	RSENSE=5mΩ	33	-	-	A
	SCP Response Time		-	-	1	μs
T_{HICCUP}	Recovery Time During Hiccup Mode		-	7*Tdelay	-	ms
$I_{PRECHARGE}$	Pre-Charge Current		-	50	-	mA
	VDRP Pre-charge Threshold		-	0.2	-	V
I_{DELAY}	Delay Source Current		-	12	-	μA
	Delay Threshold Voltage		-	1	-	V

Pin Description

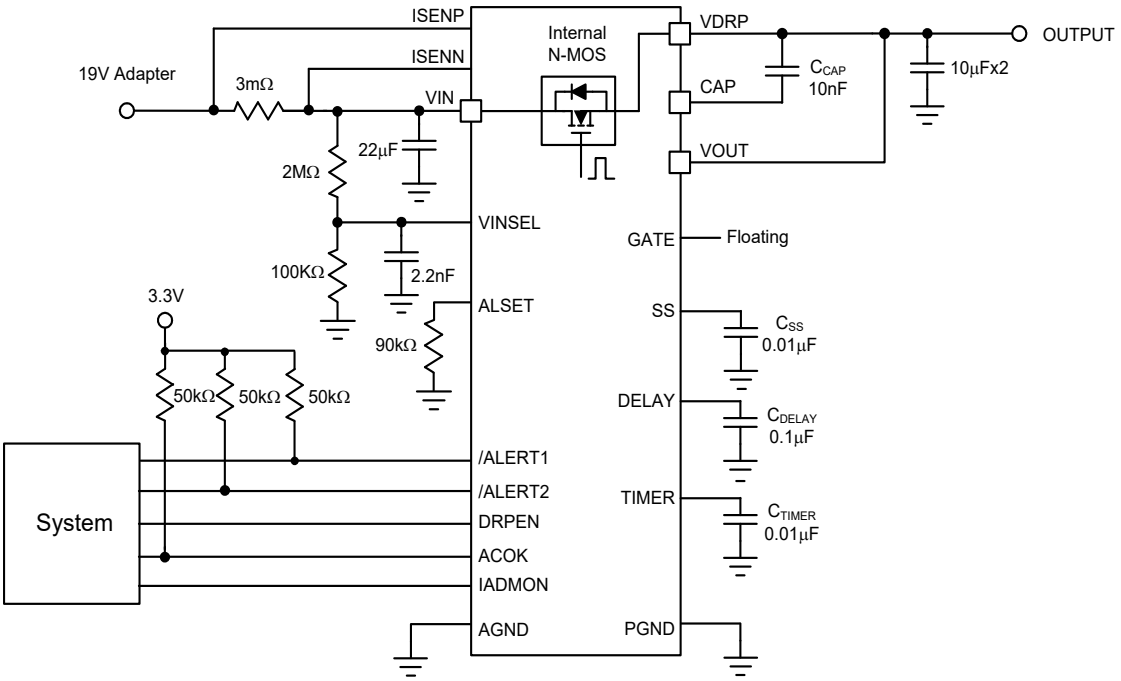
PIN		FUNCTION
NO. TQFN4x4-24F	NAME	
1	PGND	Power Ground for internal Surge MOS.
2	AGND	Signal Ground.
3	IADMON	VIN input current monitoring output pin.
4	ALSET	Current threshold setting for adapter power path.
5	/ALERT1	Alert output 1, when input OCP1 condition is detected, /ALERT1 goes low, otherwise /ALERT1 keeps high. Set the time through the Timer pin.
6	/ALERT2	Alert output 2, when input OCP2 condition is detected, /ALERT2 goes low, otherwise /ALERT2 keeps high. The time is fixed at 1ms.
7	DRPEN	Enable Input. Pulling this pin to high enables the device while pulling low disables the device. The DRPEN pin cannot be left floating.
8	ACOK	Fault Indication Pin. This pin goes low when SCP, VIN Wrong Voltage and OTP are detected.
9	DELAY	Delay time setting. Connecting a capacitor from this pin to ground sets the delay time which determines when precharge-not-ok protection is activated.
10	SS	VDRP Softstart Slew Rate Control. Connect this pin with a capacitor to ground to adjust VDRP softstart slew rate.
11	TIMER	Debounce time setting pin for /ALERT. When the event of OCP persists over the debounce time set by the TIMER pin, the APL3576A latches /ALERT at low level. Do not float this pin.
12	VOUT	Output Sense pin for Reverse Current Block function.
13	GATE	GATE control pin for external MOS.
14	CAP	Charge pump charge storage pin.
15 ~ 18	VDRP	Output Voltage Pin. The output voltage follows the input voltage. When DRPEN is low the output voltage is disconnected from input. It is recommended that the output capacitor be placed greater than 10uF*2.
19 ~ 21 Exposed Pad	VIN	Power Supply Input. Connect this pin to an external DC power supply. It is recommended that the input capacitor be placed greater than 22uF.
22	ISENN	Current Sense “–“ input pin.
23	ISENP	Current Sense “+“ input pin.
24	VINSEL	Input Voltage Sense Pin. Connect a resistive divider from VIN to VINSEL to GND to monitor the input voltage. Pull the pin low to disable the function.

Block Diagram

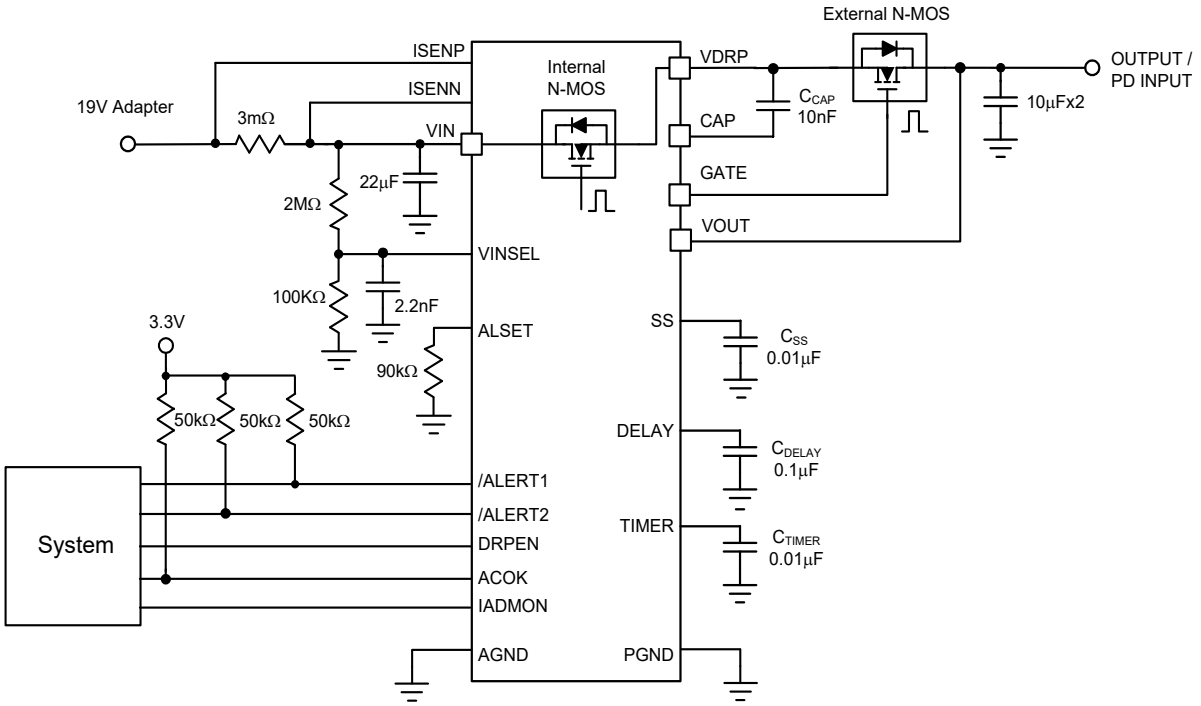


Typical Application Circuit

Single Switch :



Dual B-to-B Switch :



Function Description

Under-voltage Lockout (UVLO)

The APL3576A is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switches are N-channel MOSFETs with a low RDS(ON).

Soft-StartPrecharge and Softstart

When the APL3576A is enabled, the IC will start a precharge process to determine if there is a short-circuit at VDRP. In precharge process, a 50mA current source is activated to charge output capacitors while a 12uA current source is activated to charge CDELAY. (PS. DELAY pin must be connected a proper capacitor to ground).
The IC then initiates a softstart process to turn on internal power MOSFET. If a short circuit happens at VDRP during precharge process, the VDELAY will reach 1V before VVDRP reaches 0.2V. The IC then decides not to turn on power MOSFET and in turn enters hiccup mode. When short circuit event is gone, the IC can start a precharge and softstart process to raise up VVDRP voltage.
The relationship between VSS voltage and VVDRP voltage ratio is 0.125 times during softstart.
For example, the VVDRP voltage is equal to 20V when the VSS voltage is equal to 2.5V during softstart.
The softstart time can be calculated by the following equation:

$V_{SS}=V_{VDRP}*0.125$
$T_{SS}=(C_{SS}*V_{SS})/6uA(I_{SS})$

Short Circuit Protection

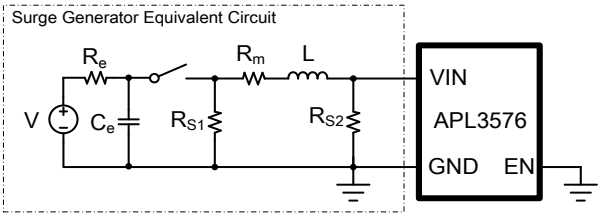
The APL3576A provides SCP protection against over load or short circuit conditions. When Output current above 33A (RSENCE=3mohm), SCP protection occurs and the APL3576A immediately shuts off the internal power MOSFET and then enters hiccup mode. In the hiccup mode, the output periodically executes soft start process until the fault event has disappeared.

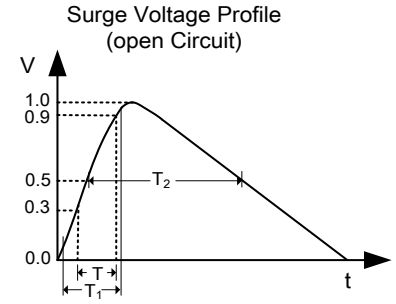
The SCP can be calculated by the following equation.
$I_{SCP}=1.98/20/RSENSE$

Surge Protection

The APL3576A implements a surge protection function in its VIN pin. When a sudden voltage spike appearing on VIN pin is high enough to trigger the surge protection, the APL3576A will limit this voltage at 27V (typical value) and conduct the surge current to ground through an internal low impedance path until the surge protection is no longer activated (namely, below 27V).
Please note that there is a limit of surge protection function: The surge protection function can only deal with transient voltage. If the surge protection function is activated for a long time, the APL3576A junction temperature will rise and eventually cause potential damage. Typically, the APL3576A can sustain a sudden surge when the total dissipating energy is below 32mJ. Please do not operate the APL3576A surge protection function beyond this limitation.
The APL3576A can deal with a surge up to V=100V. The capability of surge protection function was evaluated by the method as depicted as below diagram. We used an IEC61000-4-5 and IEC801-5 compliant surge generator to test the capability of surge protection function. The surge generator generates a voltage which is 1.2ms/50ms (open circuit) as shown in the profile below.

Evaluation Method of Surge Protection





T_1=1.67T=1.2μs±30%
T_2=50μs±20%

ACOK Output

The APL3576A provides an open-drain output to indicate that a fault has occurred. When SCP, VIN Wrong Voltage and OTP are detected, the ACOK goes low. Since the ACOK pin is an open drain output, connecting a resistor to a pull high voltage is necessary. Normally the pull high resistor is suggested between 2kΩ to 200kΩ.

Function Description (Cont.)

Enable/Disable

Pulling the DRPEN below 0.5V disables the device while pulling DRPEN above 1.2V enables the device. When the IC is disabled the supply current is reduced to a low level.
The enable input is compatible with both TTL and CMOS logic levels. The DRPEN pin cannot be left floating.

IADMON Current Report and /ALERT1/2 pin

The APL3576A reports the input current to IADMON output pin. Namely, the IADMON output voltage is proportional to input current as shown as the below equation:

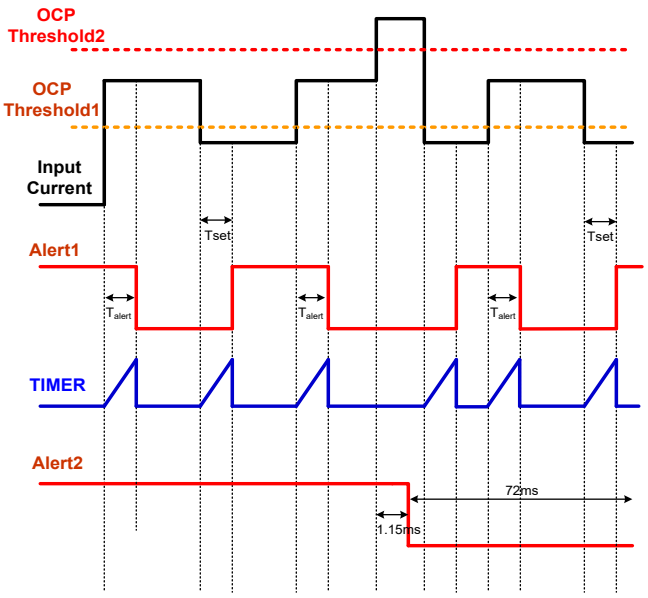
$V_{IADMON}=I_{VIN}*R_{SENSE}*K$

Where,
I_{VIN} is the input current flow into VIN pin.
R_{SENSE} is the sensing resistor which could either be the internal MOSFET A $R_{DS(ON)}$ or the external sense resistor, depending on how ISENN and ISENP is connected. Please refer to Typical Application Circuit.
K is a constant, which is 20.
When the event of $V_{IADMON}>V_{ALSET}$ persists over the debounce time set by the TIMER pin, the APL3576A latches /ALERT1 at low level. To reset /ALERT1 low state needs to toggle RESET pin a high level voltage whose pulse width is at least 1us.
The debounce time of /ALERT is set by a capacitor connected from TIMER pin to ground. The debounce time can be calculated by the following equation.

$t_{DEBOUNCE\_ALERT1}=C_{TIMER}/10uA$

Alert output 2, when input OCP2 (/ALERT2 Threshold) condition is detected, /ALERT2 goes low, The time is fixed at 1ms.
The VALSET voltage is determined by an external resistor connected from ALSET to ground. The VALSET can be calculated by the following equation.

$V_{ALSET}=10uA*R_{ALSET}$



Over-Temperature Protection

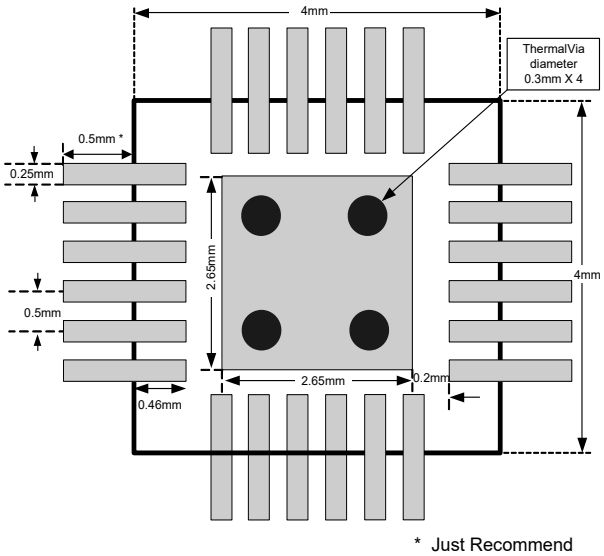
When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 30°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed TJ=+125°C.

Revere Current Block

The APL3576A provides reverse current block function or RCB to prevent current flowing from VDRP to VIN.
This function can emulate the external N-MOS as an ideal diode. In other words, the current is only allowed to flow from VIN to VDRP but forbidden from VDRP to VIN.
During normal operation, if a voltage higher then VDRP appears at VOUT, the reverse current could generate a voltage drop between VOUT and VDRP. When VOUT - VDRP>10mV is triggered, the RCB function is activated then. There is another scenario when RCB can be activated. In normal operation if a short circuit happens at VIN, the RCB function can stop current flowing from VDRP to VIN, too.
In light load or no load conditions, The VOUT is regulated at VDRP-20mV until load current is large enough to produce a voltage drop (=ILOAD*RDS(ON)) across VOUT to VDRP higher than 20mV.

Recommended Minimum Footprint (Cont.)

QFN4x4-24



Application and Implementation

Input Capacitor

A 22μF or higher ceramic bypass capacitor from VIN to GND, located near the APL3576A, is strongly recommended to suppress the ringing during short circuit fault event. When the load current trips the SCP threshold in an over load condition such as a short circuit, hot plugin or heavy load transient the IC immediately turns off the internal power switch that will cause VIN ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry.
Input capacitor is especially important to prevent VIN from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

Output Capacitor

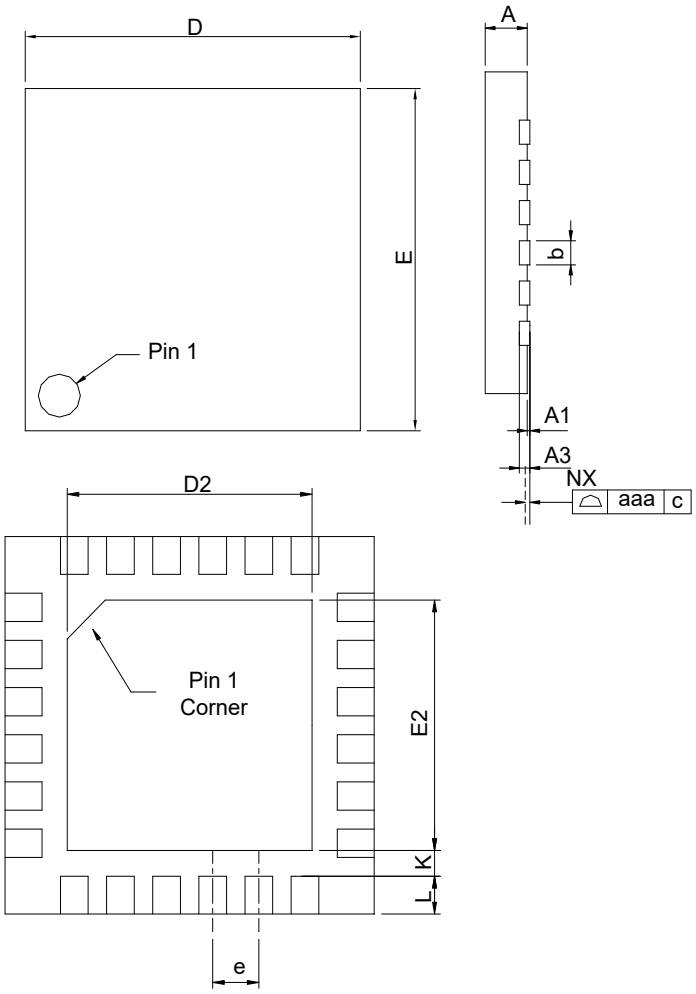
A low-ESR 22μFx2 between VDRP and GND is strongly recommended to reduce the voltage droop during hotattachment of downstream peripheral.
Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1μF ceramic capacitor improves the immunity of the device to short-circuit transients.

Input current V.S. IADMON voltage

The APL3576A is designed to enable easy configuration for monitoring adapter input current at all times. With external sensing resistor APL3576A would accurately report current through APL3576A to system via the formula, $V_{IADMON}=I_{VIN}*R_{SENSE}*K$. Besides, this device has over current protection as well when input current is more than adapter rated peak current and over current threshold could be programmable by ALSET pin. Connecting different resistance to ALSET pin could set up individual OCP threshold for different adapters.

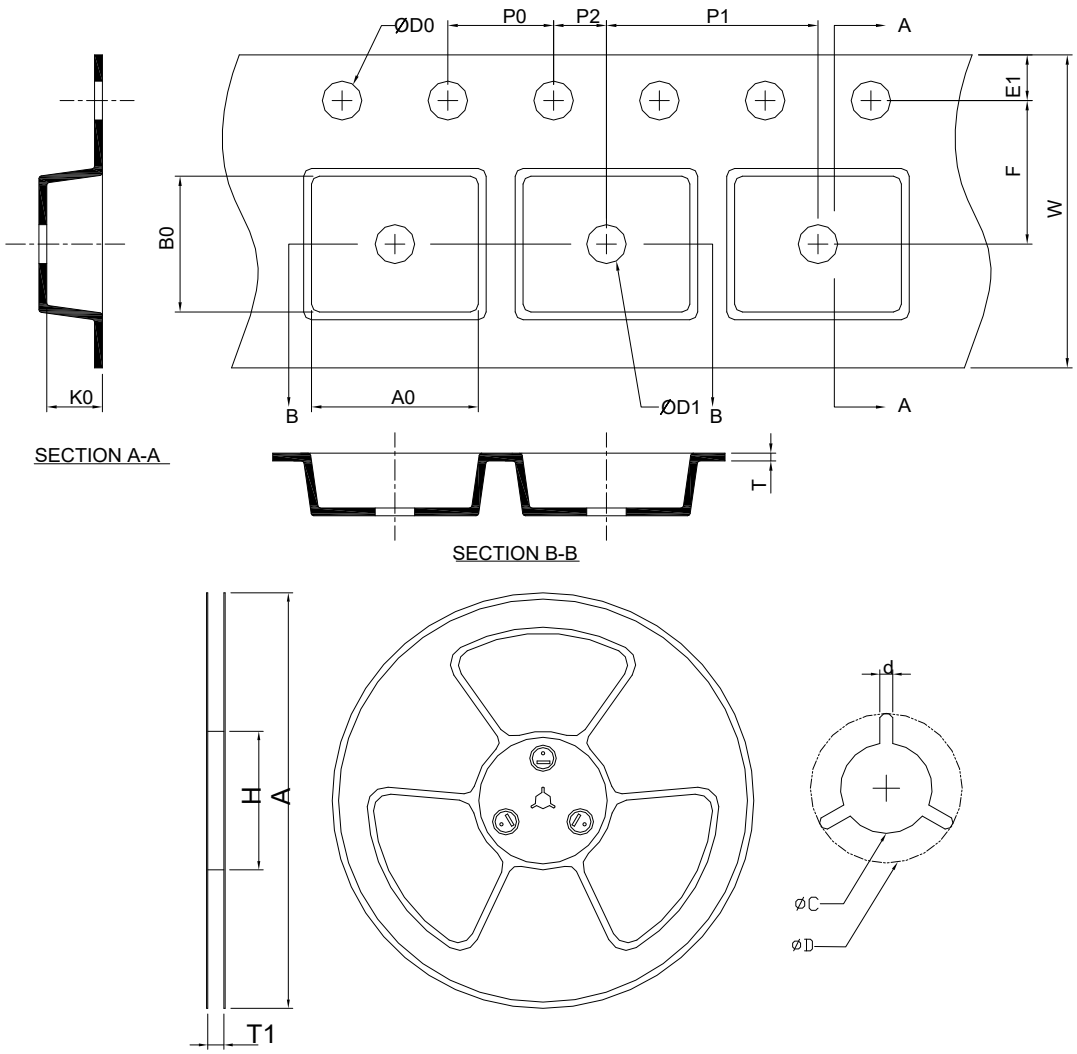
Package Information

TQFN4x4-24



SYMBOL	TQFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.50	2.80	0.098	0.110
E	3.90	4.10	0.154	0.161
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0+0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

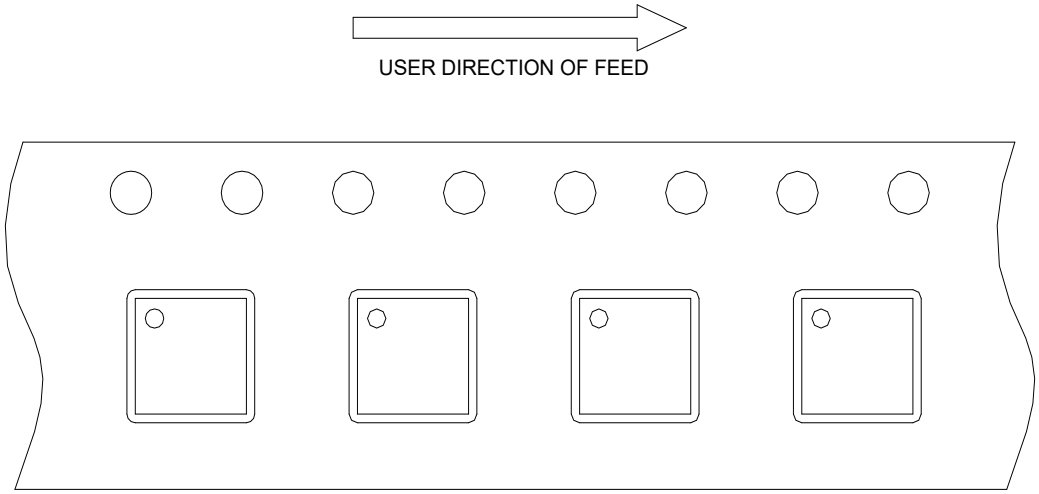
(mm)

Devices Per Unit

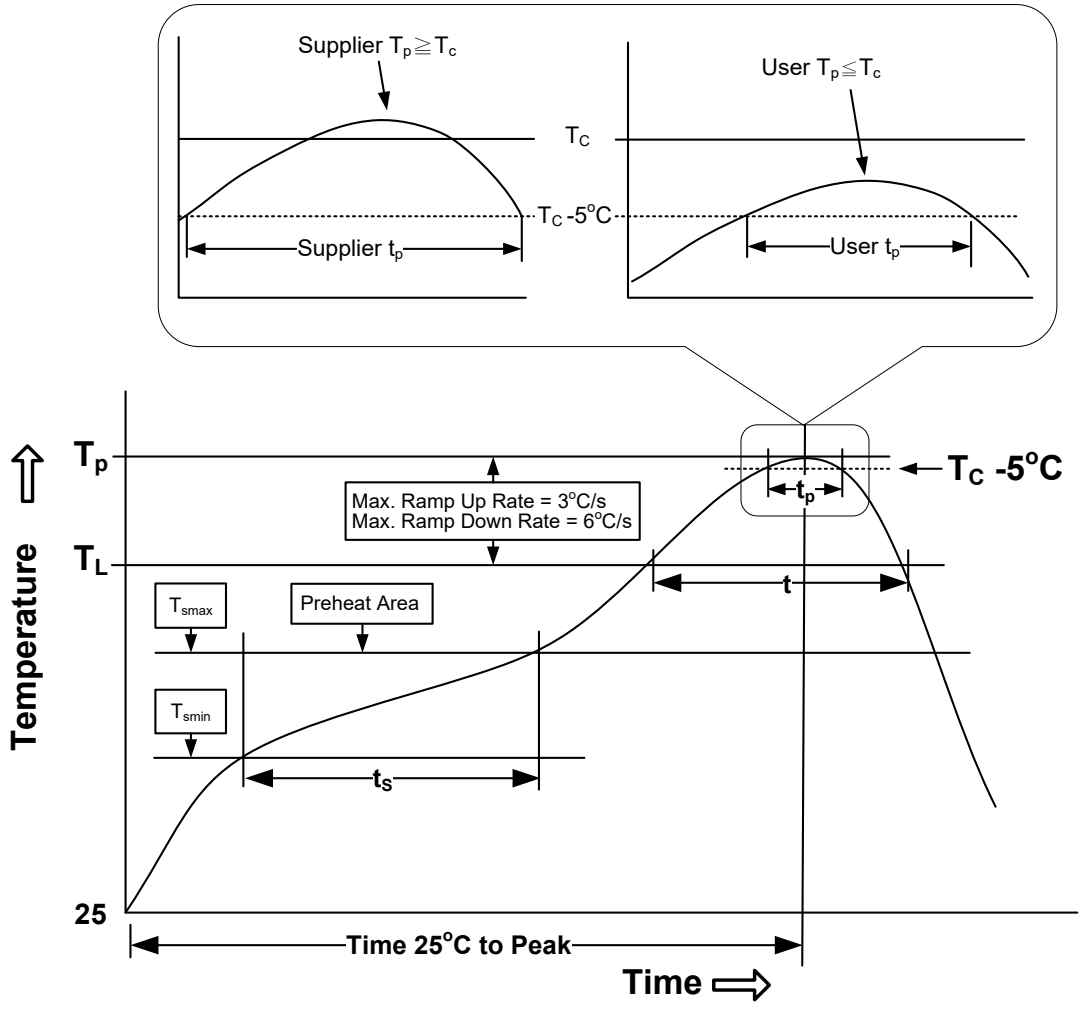
Package type	Packing	Quantity
TQFN 4*4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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