Dual Mode Display Port Interface IC

Features

- **V_{REF1} support range from 1V to 5.5V**
- **V_{REF2} support range from 1.6V to 5.5V**
- **Support DP_AUX mode or HDMI_DDC mode select function by SEL pin**
- **Support bi-directional level translation of DDC signals**
- **Leakage current between V_{REF1} and V_{REF2} limited to 100nA**
- **Built in V_{REF1} and V_{REF2} Back-drive Protection**
- **Build in Transient help for AUX2B+/- to V_{REF2} pull up voltage**
- **Support 2Mbs in DP AUX mode, 100kHz in HDMI_DDC mode**
- **Support with Display Port 2.0**
- **Support with HDMI 2.1**
- **VTQFN 2x2 - 12 Package**

General Description

APL3585A is a data selector with a built-in level shifter, which can be used for graphics cards, and can choose between HDMI DDC MODE and DP_AUX MODE through the SEL pin.

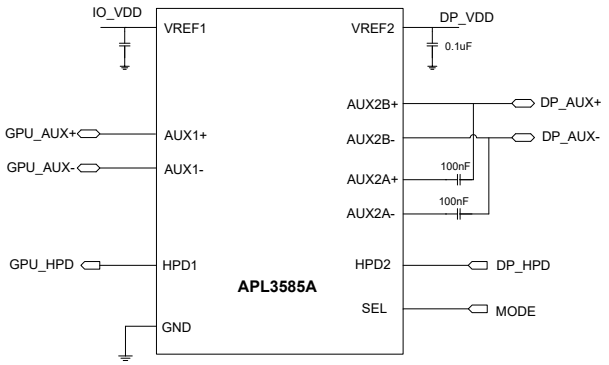
APL3585A has a transient help function in the HDMI DDC MODE, which can meet the I2C rising specifications to help data transmission without distortion.

APL3585A integrates the signal selection application circuit of the Graphics Card, which can reduce the cost and space of the Graphics Card.

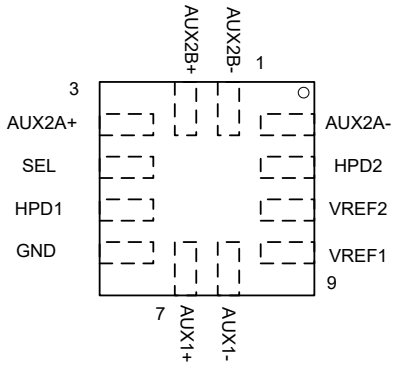
Applications

- **Display Port & HDMI AUX Signal Interface SW**
- **Graphics Card**

Simplified Application Circuit

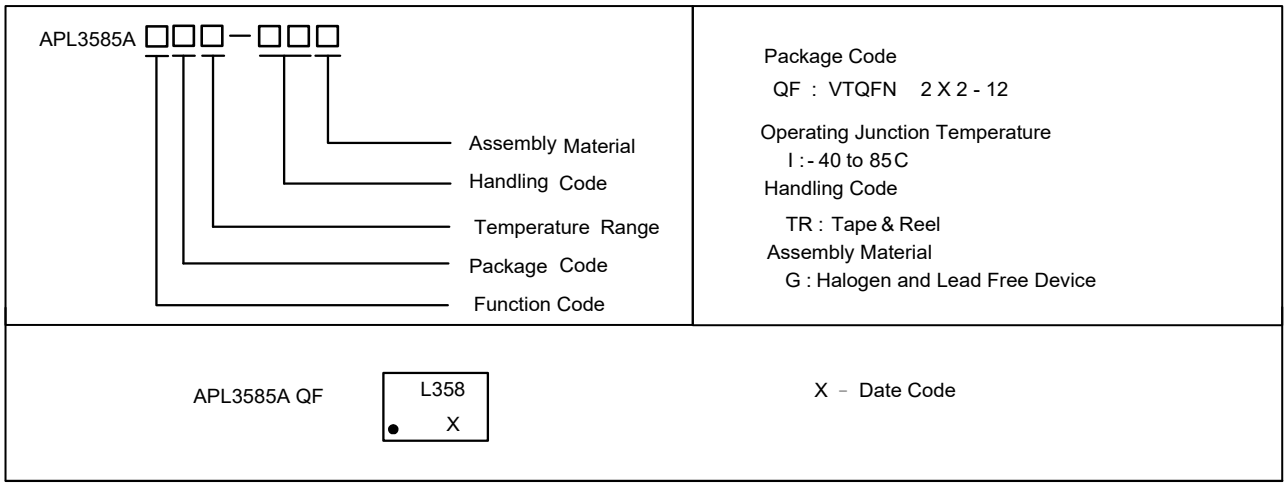


Pin Configuration (Top View)



APL3585A
VTQFN 2X2-12
(TOP View)

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
VREF1, VREF2	power input pin	-0.3 ~ 6	V
-	Other Pins	-0.3 ~ 6	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions"is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

Symbol	Parameter	Rating	Unit
V_{ESD}	Human Body Mode	4K	V
	Machine Mode (MM)	200	V
	Charge device Mode (CDM)	1K	V

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	VTQFN2x2-12	75	°C/W
θ_{JC}	Junction to Case Resistance in free air (Note 2)	VTQFN2x2-12	13	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{REF1}	VREF1 power input voltage (V_{REF2}>=V_{REF1})	1~ 5.5	V
V_{REF2}	VREF2 power input voltage (V_{REF1}>=1V)	1.6~ 5.5	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{REF1}=1.8V, V_{REF2}=3.3V, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test condition	APL3585A			Unit
			Min.	Typ.	Max.	
V_{REF1}		VREF2 >=VREF1	1	1.8	5.5	V
$V_{REF1\ POR}$		VREF2>=1.6V	0.65	0.8	0.95	V
$V_{REF1\ POR\_HYS}$		VREF2>=1.6V	0.05	0.1	0.16	V
IDD1	V_{REF1}	HPD2=0, AUX1,2A,2B N.C.	-	2.4	10	uA
		HPD2=VREF2, AUX1,2A,2B N.C.	-	53	200	uA
V_{REF2}		VREF2 >=VREF1	1.6	3.3	5.5	V
$V_{REF2\ POR}$		VREF1>=1V	1	1.25	1.5	V
$V_{REF2\ POR\_HYS}$		VREF1>=1V	0.05	0.12	0.25	V
IDD2	V_{REF2}	HPD2=0, AUX1,2A,2B N.C.	-	0.1	10	uA
		HPD2=VREF2, SEL=0, AUX1,2A,2B N.C.	-	53	200	uA
		HPD2=VREF2, SEL=1, AUX1,2A,2B N.C.	-	95	300	uA
Leakage Current	Between V_{REF1} and V_{REF2}	VREF1=0V or VREF2=0V	-	-	100	nA
AUX1	AUX1+ single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{REF1} +0.4	V
	AUX1- single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{REF1} +0.4	V
	AUX1+ , AUX1- Pull-down		60	80	100	kΩ
AUX2A	AUX2A+ single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{AUX1+}	V
	AUX2A- single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{AUX1-}	V
	AUX2A+/- Pull-up to V_{REF2}	SEL = 1 (DDC mode)	60	80	100	kΩ
	Resistance between AUX1 and AUX2A pins	SEL=0, AUX1= 0.845V VREF1=1.8V, VREF2=3.3V, 10mA into AUX2A	-	5	10	Ω
		SEL=0, AUX1=0.7V VREF1=1V, VREF2=2V, 0.1mA into AUX2A	-	15	50	Ω
		SEL=1	100	-	-	MegΩ
AUX2B	AUX2B+ single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{REF2}	V
	AUX2B- single-ended swing	VREF1>=1V, VREF2>=1.6V	0	-	V_{REF2}	V
	AUX2B+ Pull-down		60	80	100	kΩ
	AUX2B- Pull-up to V_{REF2}		60	80	100	kΩ
	Resistance between AUX1 and AUX2B pins	SEL=0	100	-	-	MegΩ
		SEL=1, AUX1= 0.3 x VREF1, VREF1=1V, VREF2=2V, 10mA into AUX2B	-	-	10	Ω
HPD1	Pull-up		28	38	50	kΩ
	V_{OL}	HPD2>2V, external Rup=10kohm to VREF1=1.8v	0	-	10% V_{REF1}	V
	HPD1 VREF1 POR	HPD2=2V, VREF2=0V, Vref1 ramps up unit HPD1 < 0.4V	0.6	0.81	0.95	V
	HPD1 VREF1 HYS	HPD2=2V, VREF2=0V, VREF1 ramps down until HPD1 > 0.4V	-	87	-	mV

Electrical Characteristics (Cont.)

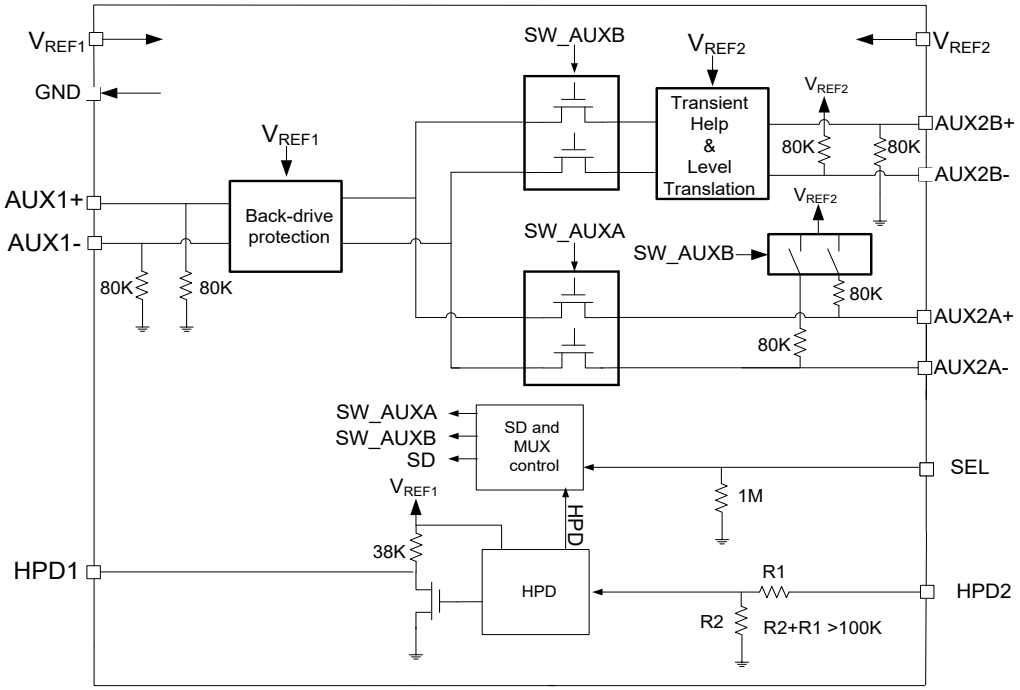
Unless otherwise specified, these specifications apply over V_{REF1}=1.8V, V_{REF2}=3.3V, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test condition	APL3585A			Unit
			Min.	Typ.	Max.	
HPD2	V_{IH}	logic High voltage	2	-	5.3	V
	V_{IL}	logic Low voltage	0	-	0.8	V
	Pull-down		100	135	200	kΩ
	Rising edge Delay	HPD2=0 ->2V,Tr=1ns HPD1=VREF1->0.1VREF1, CL=10pF	-	90	200	ns
	falling edge Delay	HPD2=2 ->0V,Tf=1ns HPD1=VREF1->0.9VREF1, CL=10pF	-	1100	2000	ns
	power saving debounce time	HPD2> 2V, enter to awake mode	10	20	30	ms
		HPD2< 0.8V, enter to standby mode	2	4	8	ms
SEL	VI_H	logic High voltage	70% V_{REF2}	-	-	V
	VI_L	logic Low voltage	-	-	30% V_{REF2}	V
	Pull-down		0.75	1	1.25	MegΩ
I^2C timing requirements in standard mode (I^2C specification, UM10204 rev.5)						
t_R	Rise time	AUX2B from VIL(0.3V_{REF2}) to VIH(0.7V_{REF2}) base on Cap of DDC line total=800pF	-	-	1000	ns
t_F	Fall time		-	-	300	ns
	C AUX2B	SEL=1 AUX2B+/-=0V Without PCB Parasitic capacitance	-	-	50	pF

Pin Descriptions

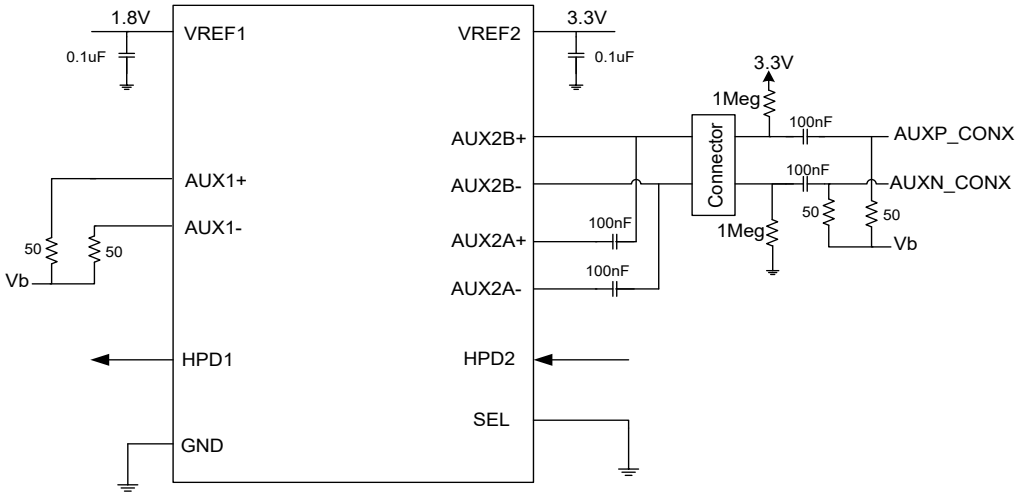
PIN		FUNCTION
NO. TQFN2x2	NAME	
1	AUX2B-	Connector side bi-directional AUX2B- signal.
2	AUX2B+	Connector side bi-directional AUX2B+ signal.
3	AUX2A+	Connecter side bi-directional AUX2A+ signal.
4	SEL	AUX2 A/B select input. (Low selects AUX2A, High selects AUX2B).
5	HPD1	HPD signal output to GPU.
6	GND	Ground.
7	AUX1+	GPU side bi-directional AUX1+ signal.
8	AUX1-	GPU side bi-directional AUX1- signal.
9	V_{REF1}	GPU side reference voltage input.
10	V_{REF2}	Connector side reference voltage input.
11	HPD2	HPD signal input from connector.
12	AUX2A-	Connecter side bi-directional AUX2A- signal.

Block Diagram

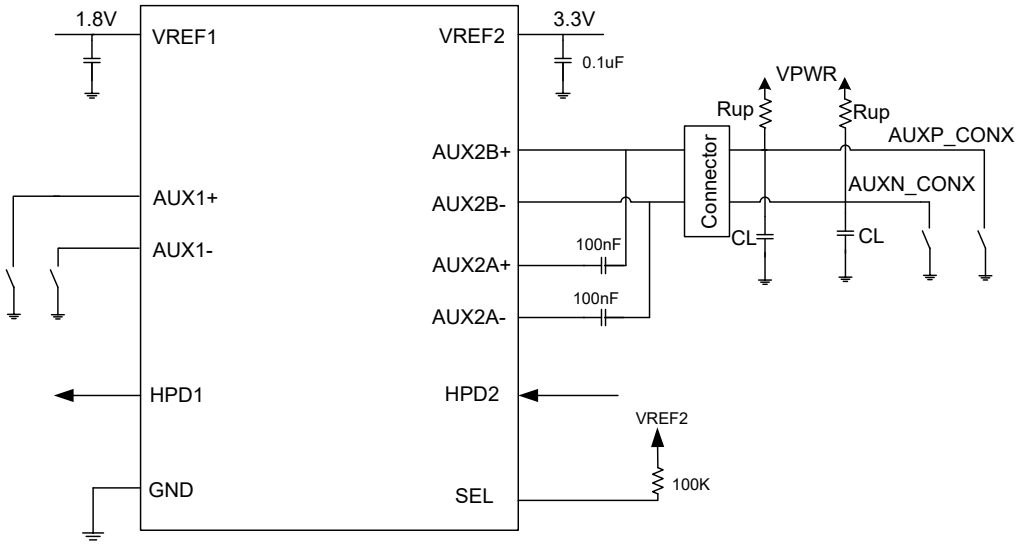


Typical Application Circuit

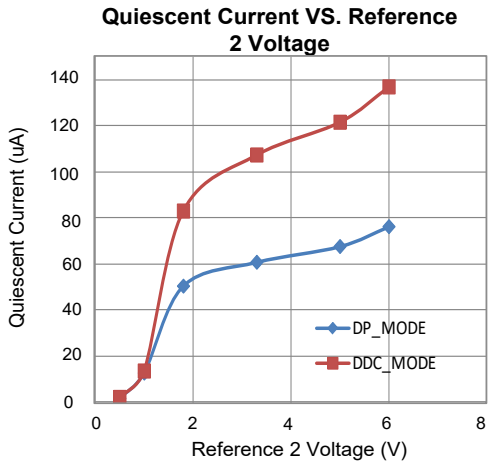
1. DP_AUX MODE

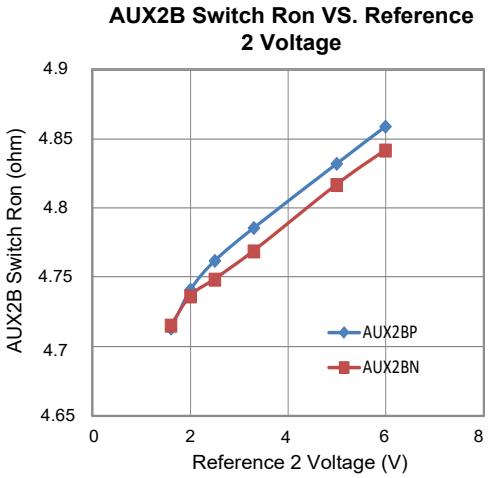


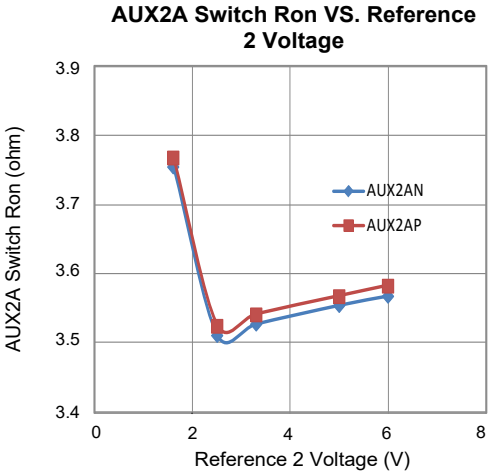
2. HDMI _ DDC MODE



Typical Operating Characteristics



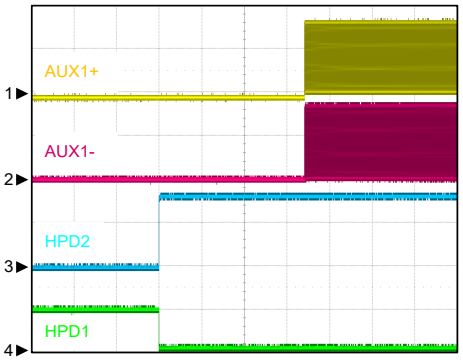




Operating Waveforms

Refer to the typical application circuit. The test condition is V_{REF1}=1.8V, V_{REF2}=3.3V, T_A= 25°C unless otherwise specified.

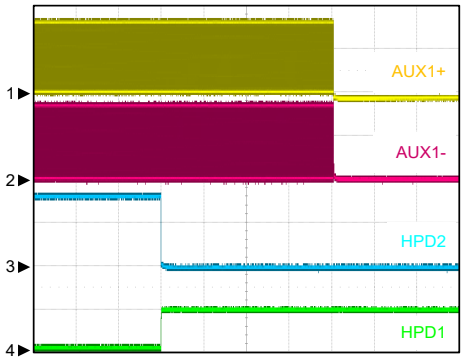
HPD Power On



SEL=Low; DP_AUX Mode

CH1: AUX1+, 0.5V/Div, DC
CH2: AUX1-, 0.5V/Div, DC
CH3: HPD2, 2V/Div, DC
CH4: HPD1, 2V/Div, DC
TIME: 5ms/Div

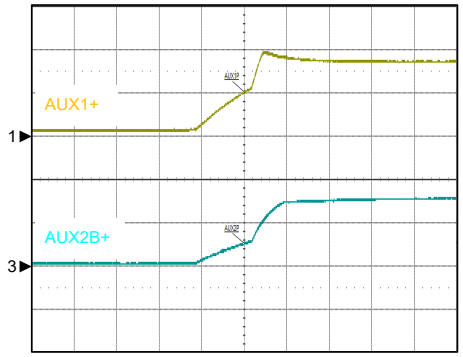
HPD Power Off



SEL=Low; DP_AUX Mode

CH1: AUX1+, 0.5V/Div, DC
CH2: AUX1-, 0.5V/Div, DC
CH3: HPD2, 2V/Div, DC
CH4: HPD1, 2V/Div, DC
TIME: 1ms/Div

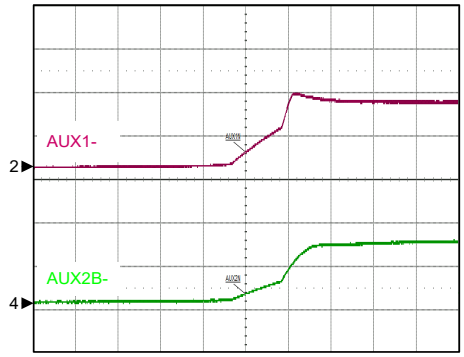
Transient Help Positive



SEL=High ; DDC_HDMI Mode

CH1: AUX1+, 1V/Div, DC
CH3: AUX2B+, 2V/Div, DC
TIME: 500ns/Div

Transient Help Negative



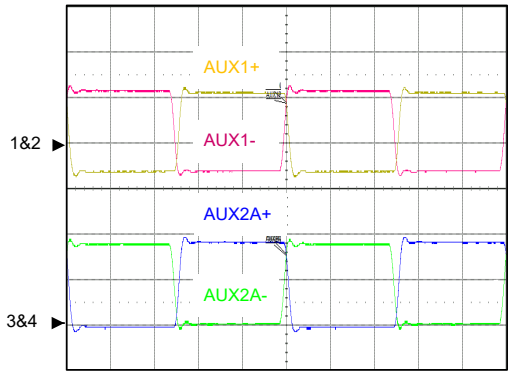
SEL=High ; DDC_HDMI Mode

CH2: AUX1-, 1V/Div, DC
CH4: AUX2B-, 2V/Div, DC
TIME: 500ns/Div

Operating Waveforms (Cont.)

Refer to the typical application circuit. The test condition is V_{REF1}=1.8V, V_{REF2}=3.3V, T_A= 25°C unless otherwise specified.

DP AUX Normal Operation



AUX2A+ 0~0.8,AUX2A- 0.8~0 ; 1MHz

CH1: AUX1+, 0.5V/Div, DC
CH2: AUX1-, 0.5V/Div, DC
CH3: AUX2A+, 0.5V/Div, DC
CH4: AUX2A-, 0.5V/Div, DC
TIME: 200ns/Div

Function Descriptions

Data Selector

When the SEL voltage level is V_{REF2}, the IC is in HDMI_DDC mode. AUX2B [+-] pins lead to AUX1 [+-] pins, and conduct signals in bi-directional, while AUX2A [+-] is in high impedance.
When the SEL voltage level is GND, the IC is in DP_AUX mode. AUX2A [+-] pins lead to AUX1 [+-] pins, and conduct signals in bi-directional, while AUX2B [+-] is in high impedance.

Level Translation

The AUX1/HDMI_DDC Interface IC shall provide bi-directional level translation between V_{REF1} to V_{REF2} levels on AUX2B signal path. The AUX2A signal path does not require level translation as the GPU will be driving CML when this path is selected.

VREF1 and VREF2 Back-drive Protection

When V_{REF1} or V_{REF2} of APL3585A is below the POR threshold, SW_AUXA/B will be turned off.
If V_{REF1} is below the V_{REF1_POR} threshold, HPD1 is pulled up to V_{REF1}.

Hot Plug Detection

When the APL3585A hot plug detection pin HPD2 is high, the IC will be woken up and enter the normal operating mode.
When HPD2 = H, HPD1 = L; HPD2 = L, HPD1 = H.

Transient Help

In standard mode, as shown in Figure 1, APL3585A has a transient help function to make the HDMI_DDC bus comply with I2C timing specifications. When the signal is transmitted from the GPU to the HDMI_DDC bus, this function can speed up the rise time of AUX2B.

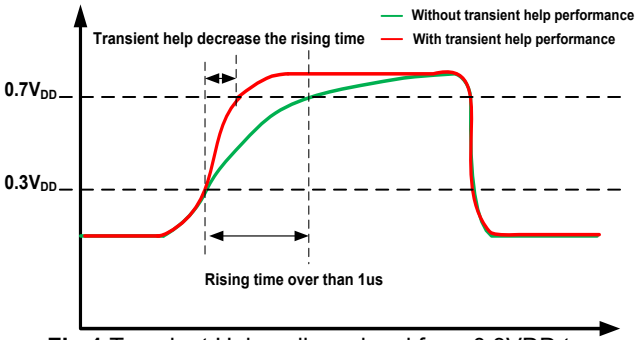
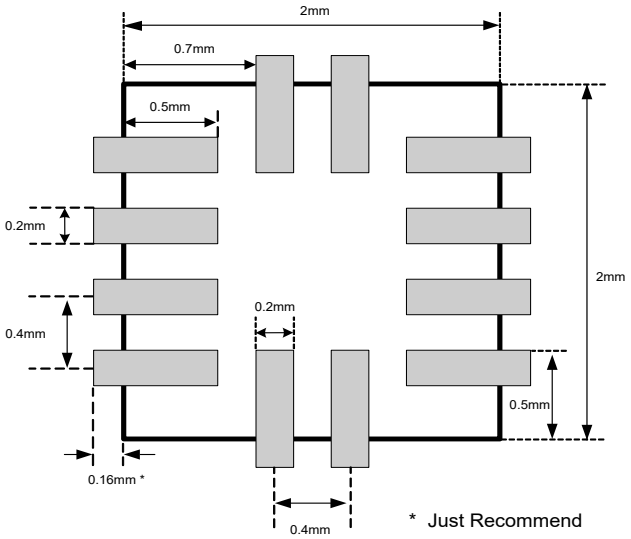


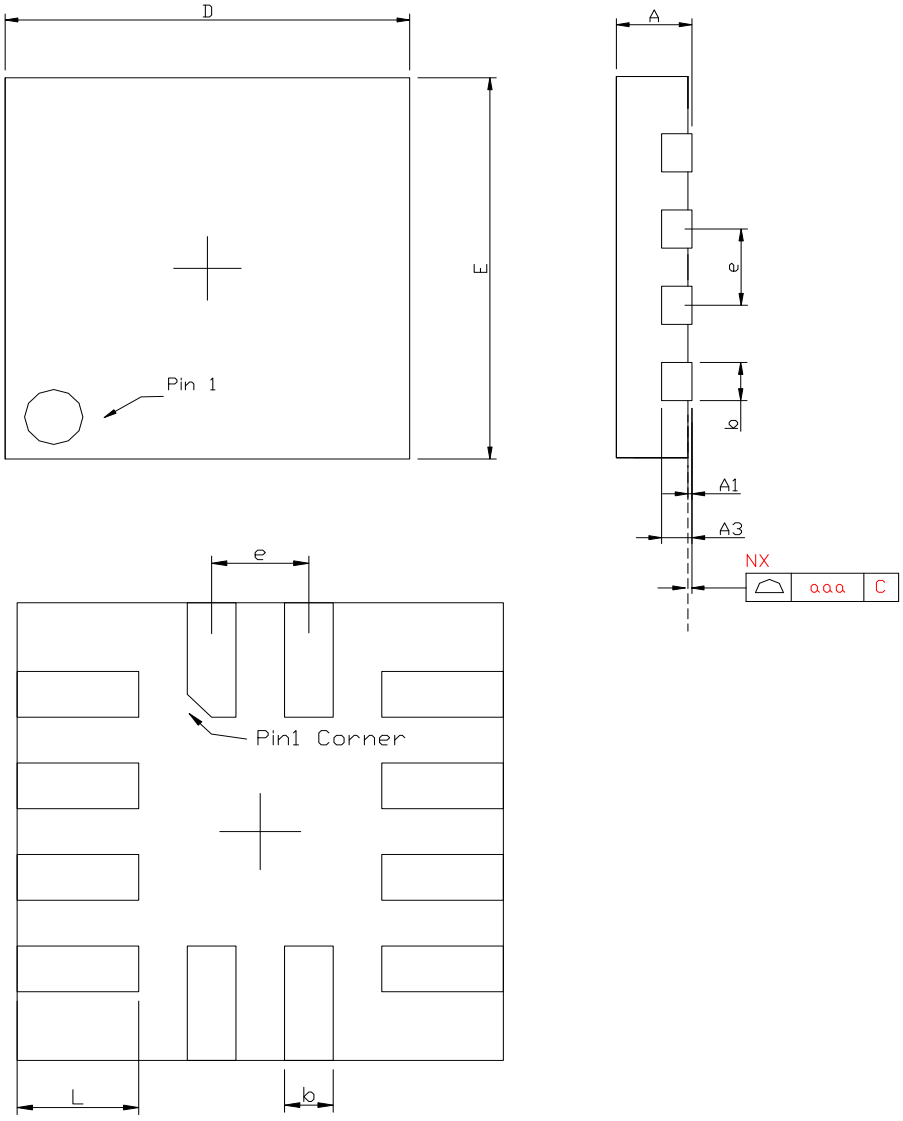
Fig.1 Transient Help pull up signal from 0.3VDD to 0.7VDD in 1us

Recommended Minimum Footprint



Package Information

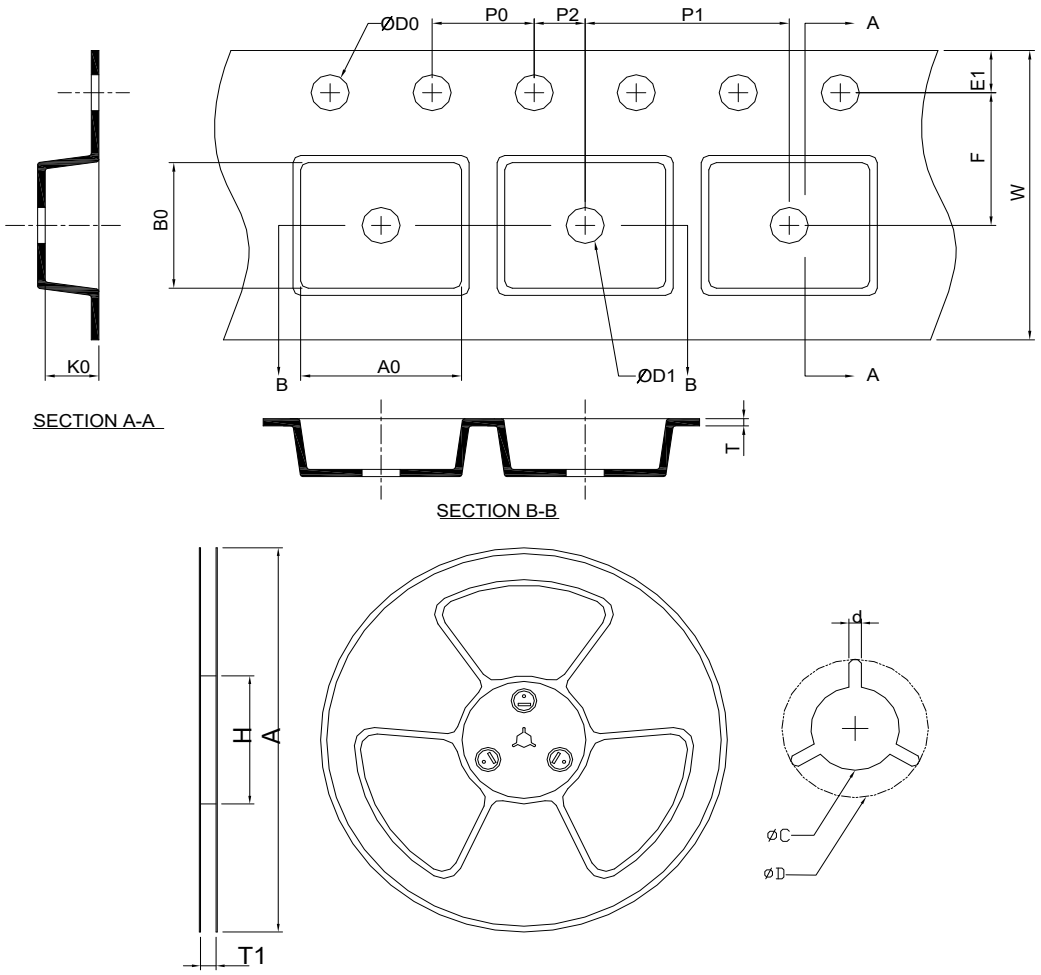
VTQFN2x2-12



Bottom View

SYMBOL	VTQ FN2*2-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.15	0.25	0.006	0.010
D	1.90	2.10	0.075	0.083
E	1.90	2.10	0.075	0.083
e	0.4 0 BSC		0.01 6 BSC	
L	0.45	0.55	0.018	0.022
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN(2x2)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20±0.15	2.20±0.15	0.75±0.05

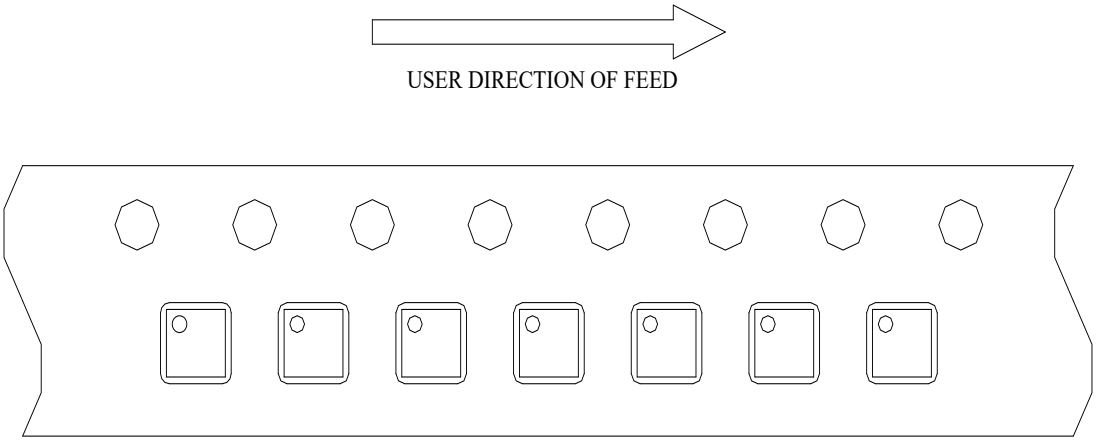
(mm)

Devices Per Unit

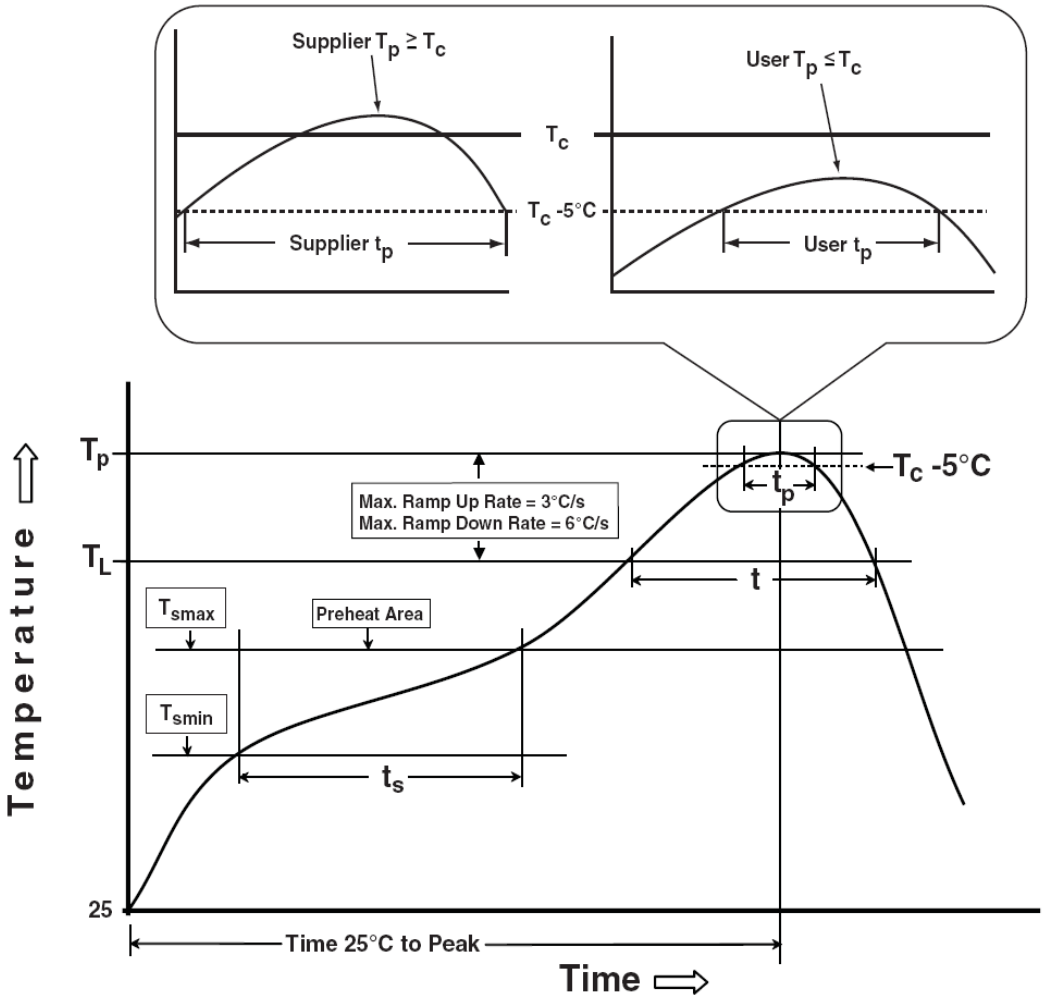
Package type	Packing	Quantity
VTQFN(2x2)	Tape & Reel	3000

Taping Direction Information

VTQFN2x2-12



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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