PMIC for LCD Bias Power

Features

- Input Voltage Range from 2.7V to 5.5V
- Positive & Negative Charge Pump for V_{GH} & V_{GL}
- High Performance Operation Amplifier
  - ±100mA Output Short Circuit Current
  - 13V/μs Slew Rate
  - 10MHz, -3dB Bandwidth
- Control Output for External P-MOSFET to Support Completely Disconnecting the Battery
- Adjustable Power Sequence by External Capacitor
- Internal Soft-start
- Cycle By Cycle Current Limit
- Multiple Overload Protection
- Over Temperature Protection
- Available in TQFN3x3-20 Package
- Halogen and Lead Free Available (RoHS Compliant)

General Description

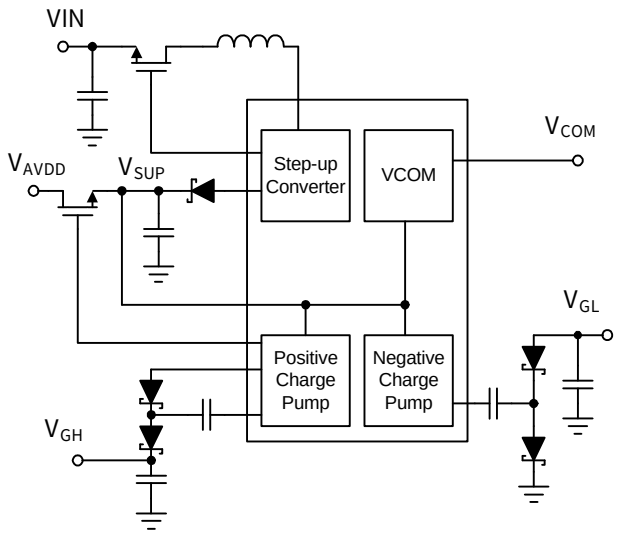
The APW7276 integrates with a high-performance step-up converter, two charge pump controllers and one high current operational amplifiers for TFT-LCD applications. The main step-up regulator is a current-mode, fixed-frequency PWM switching regulator. The 1.5MHz switching frequency allows the usage of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs.The charge pump controllers provide regulated the gate-driver of TFT-LCD V_{GH} and V_{GL} supplies.The amplifiers are ideal for V_{COM} applications, with 100mA output short circuit current drive, 10MHz bandwidth, and 13V/μs slew rate. All inputs and outputs are rail-to-rail.

The APW7276 is available in a tiny 3mm x 3mm 20-pin QFN package (TQFN3x3-20).

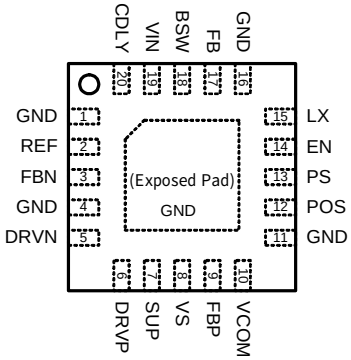
Applications

- Panel

Simplified Application Circuit



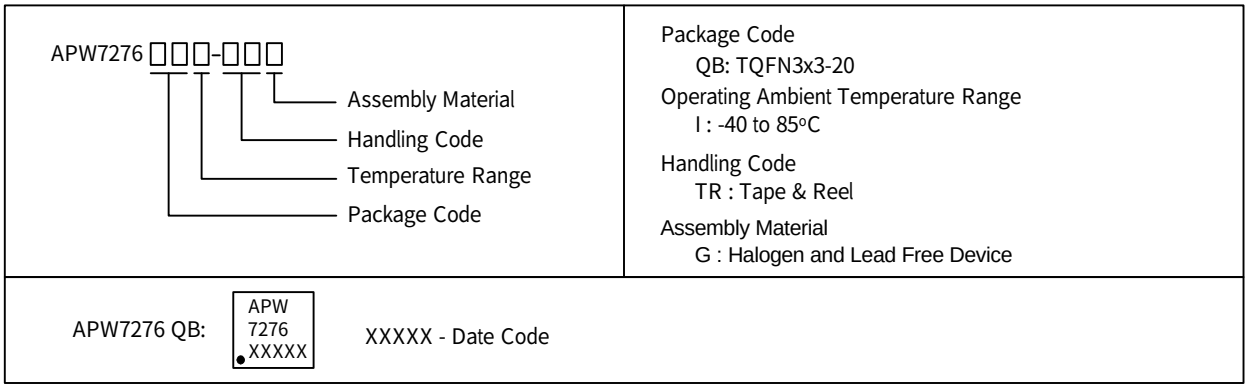
Pin Configuration



TQFN3x3-20
Top View

= Thermal Pad (connected to GND plane for better heat dissipation)

Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
VIN	Input Bias Supply Voltage (VIN to GND)	-0.3 ~ 6	V
	LX, DRP, DRN, PS, SUP, VS, POS, VCOM to GND Voltage	-0.3 ~ 20	V
	FB, FBP, FBN, BSW, CDLY, REF, EN to GND Voltage	-0.3 ~ 6	V
P_D	Power Dissipation	Internally Limit	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2) TQFN3x3-20	50	°C/W
θ_{JC}	Case-to-Ambient Resistance in free air (Note 2) TQFN3x3-20	12	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
VIN	Input Bias Supply Voltage (VIN to GND)	2.7 ~ 5.5	V
V_{SUP}	Main Step-up Converter Output Voltage	VIN ~ 15	V
V_{GH}	Positive Charge Pump Output Voltage	0 ~ 2*V_{SUP} -2	V
V_{GL}	Negative Charge Pump Output Voltage	-V_{SUP}+2 ~ V_{REF}	V
C_{IN}	Input Power Capacitor	4.7 ~	µF
L1	Inductor Range	1 ~ 10	µH
C_{VGH}	V_{GH} Capacitor	0.22 ~ 2.2	µF
C_{VGL}	V_{GL} Capacitor	0.22 ~ 2.2	µF
C_{REFF}	V_{REF} Capacitor	0.1 ~ 0.47	µF
R1	Feedback Resistance of V_{SUP}	0.1 ~ 1	MΩ
R4	Feedback Resistance of V_{GH}	0.1 ~ 1	MΩ
R6	Feedback Resistance of V_{GL}	0.1 ~ 0.54	MΩ
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7276			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
VIN	Input Voltage Range		2.7	-	5.5	V
I_{VIN}	VIN Supply Current	V_{FB} = 1V, switching	-	2	5	mA
		V_{FB} = 1.3V, no switching	-	300	-	µA
I_{SD}	VIN Shutdown Input Current	EN = GND	-	0.1	1	µA
UNDER VOLTAGE LOCKOUT (UVLO)						
VIN	UVLO Threshold Voltage		2.2	2.4	2.6	V
	UVLO Hysteresis Voltage		50	100	150	mV
STET-UP REGULATOR						
V_{REF}	Reference Voltage	VIN=2.7V~5.5V, T_A = -40 ~ 85°C, I_{REF} = 0 ~ 2mA	1.225	1.25	1.275	V
I_{REF}	Reference Voltage Output Current		2	-	-	mA
V_{FB}	FB Regulation Voltage	VIN=2.7V~5.5V, T_A = -40 ~ 85°C	1.225	1.25	1.275	V
F_{SW}	Switching Frequency	V_{FB} = 1.1V	1.25	1.5	1.75	MHz
R_{ON}	Power Switch On Resistance	VIN = 3.6V	-	0.5	-	Ω
I_{LIM}	Power Switch Current Limit		2.0	-	-	A
	LX Leakage Current	V_{EN} = GND, V_{LX}=0V or 5V, VIN = 5V	-1	-	1	µA
D_{MAX}	LX Maximum Duty Cycle		92	95	98	%
I_{FB}	FB Input Current		-50	-	50	nA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7276			Unit
			Min.	Typ.	Max.	
SOFT-START AND SHUTDOWN						
T_{SS}	Step-up Regulator Soft-start Duration	(Note 4)	-	2	-	ms
V_{TEN}	EN High Threshold	V_{EN} Rising	-	-	1	V
	EN Low Threshold	V_{EN} Falling	0.4	-	-	V
I_{EN}	EN Leakage Current	V_{EN} = 5V, VIN = 5V	-1	-	1	μA
I_{BSW}	BSW Pull-down Current		3	5	10	μA
	BSW to VIN Ron		-	200	-	Ω
I_{CDLY}	CDLY Charge Current		-	10	-	μA
	CDLY High Threshold	V_{GL} Soft-start without Delay from V_{SUP}	-	1	-	V
	PS to GND Leakage Current	V_{PS}=15V	-	-	100	nA
	PS to GND On Resistance		-	1k	-	Ω
INTERNAL SWITCH						
R_{VS}	SUP to VS On Resistance		-	50	-	Ω
	SUP to VS Leakage Current		-	-	100	nA
	VS Soft-start Duration	(Note 4)	-	2	-	ms
POSITIVE REGULATED CHARGE PUMP						
V_{FBP}	FBP Regulation Voltage	VIN=2.7V~5.5V, T_A = -40 ~ 85°C	1.225	1.25	1.275	V
I_{FBP}	FBP Input Current		-50	-	50	nA
I_{DRVP}	RMS DRVP Output Current	V_{SUP} = 12V	5	-	-	mA
	DRP On Resistance High		-	20	-	Ω
	DRP On Resistance Low		-	3.5	-	Ω
	Positive Charge Pump Frequency		400	500	600	kHz
T_{SSP}	Positive Charge Pump Soft-start Duration	(Note 4)	-	2	-	ms
NEGATIVE REGULATED CHARGE PUMP						
V_{FBN}	FBN Regulation Voltage	VIN=2.7V~5.5V, T_A = -40 ~ 85°C	-25	0	25	mV
I_{FBN}	FBN Input Current		-50	-	50	nA
I_{DRVN}	RMS DRVN Output Current	V_{SUP} = 12V	5	-	-	mA
	DRN On Resistance High		-	5	-	Ω
	DRN On Resistance Low		-	12	-	Ω
	Negative Charge Pump Frequency		400	500	600	kHz
T_{SSN}	Negative Charge Pump Soft-start Duration	(Note 4)	-	2	-	ms

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7276			Unit
			Min.	Typ.	Max.	
SEQUENCE						
T_{DEL1}	PS Delay Time	(Note 4)	-	15	-	ms
T_{DEL2}	Delay Time Between V_{AVDD} to V_{GL}	(Note 4)	1	-	15	ms
T_{DEL3}	Delay Time Between V_{GL} to V_{GH}	(Note 4)	-	15	-	ms
VCOMP BUFFER						
A_{OL}	Open Loop Gain	(Note 4)	-	110	-	dB
V_{OH}	Output Voltage High	I_{OUT}=100µA	V_{SUP}-15	V_{SUP}-3	-	mV
		I_{OUT}=5mA	V_{SUP}-150	V_{SUP}-80	-	mV
V_{OL}	Output Voltage Low	I_{OUT}=100µA	-	2	15	mV
		I_{OUT}=5mA	-	80	150	mV
I_{SC}	Short Circuit Current		50	70	-	mA
I_{VCOM}	Continuous Output Current		±40	-	-	mA
	VCOM discharge resistance		-	2	-	kΩ
PSRR	Power Supply Rejection Ratio	(Note 4)	60	-	-	dB
BW	-3dB Bandwidth	(Note 4)	-	10	-	MHz
GBWP	Gain Bandwidth Product	(Note 4)	-	8	-	MHz
SR	Slew Rate	(Note 4)	-	13	-	V/µs

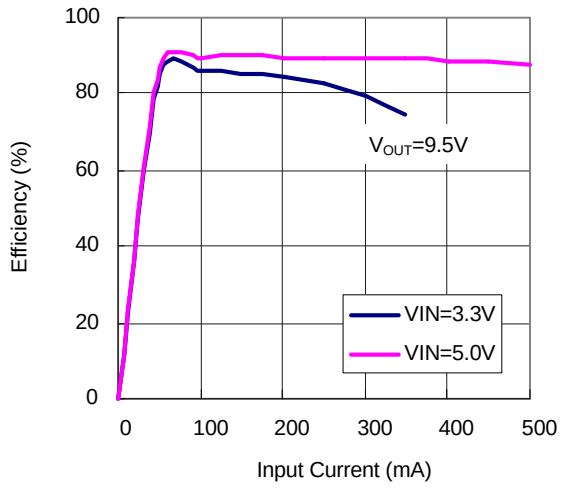
Note 4: Guarantee by design, not production test

Pin Description

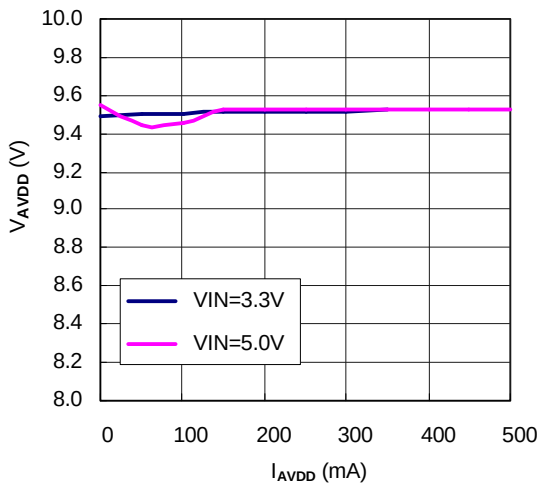
PIN		FUNCTION
TQFN3x3-20	NAME	
1,4,11,16	GND	Signal and Power ground. Connect these pins to exposed pad.
2	REF	Internal 1.25V reference voltage output. Connect 1μF capacitor to this pin.
3	FBN	Negative charge pump feedback input.
5	DRVN	Regulated charge pump driver for V_{GL}. Connect to flying capacitor.
6	DRVP	Regulated charge pump driver for V_{GH}. Connect to flying capacitor.
7	SUP	This is the supply pin of the positive and negative charge pump driver. Connected this pin to the output of the main step-up converter V_{SUP}.
8	VS	The supply voltage of positive charge pump regulator.
9	FBP	Positive charge pump feedback input.
10	VCOM	VCOM output.
12	POS	Non-inverting Input of VCOM.
13	PS	This is the gate drive pin which can be used to control an external P-channel MOSFET to provide input to output isolation of V_{SUP} or V_{AVDD}. See the Typical Application Section. PS is an open-drain output and is pulled low as soon as the delay time of CDLY setting is expired. PS goes high impedance when the EN is low.
14	EN	Enable pin. Logic high initiates power-up sequencing. Logic low disable the device.
15	LX	Step-up converter inductor/diode connection.
17	FB	Main step-up converter feedback input.
18	BSW	Bi-direction switch control pin. This switch disconnects VOUT from VIN during shutdown and any fault evens.
19	VIN	IC power input.
20	CDLY	Delay Setting Capacitor Connection Pin. Connecting a capacitor from this pin to GND allows the setting of delay time between V_{SUP} to V_{GL} during start-up. Pull this pin exceed 1V ignore the delay time.
Exposed Pad	GND	Signal and Power Ground.

Typical Operating Characteristics

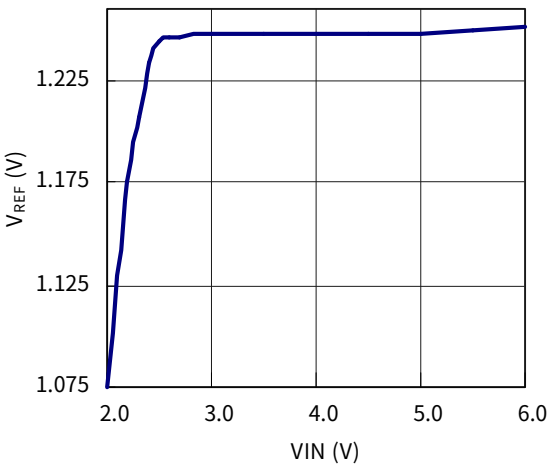
I_{AVDD} vs.Efferency



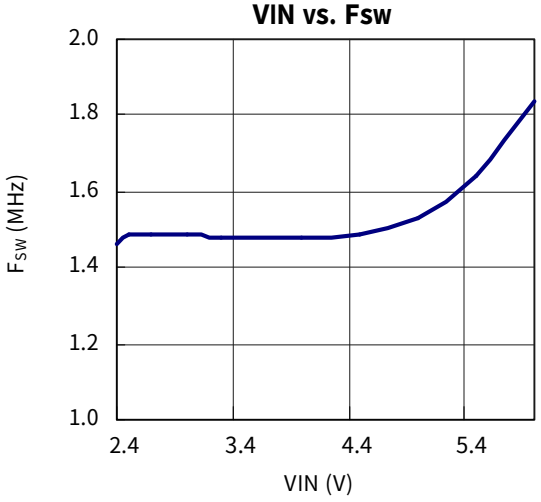
V_{AVDD} vs. I_{AVDD}



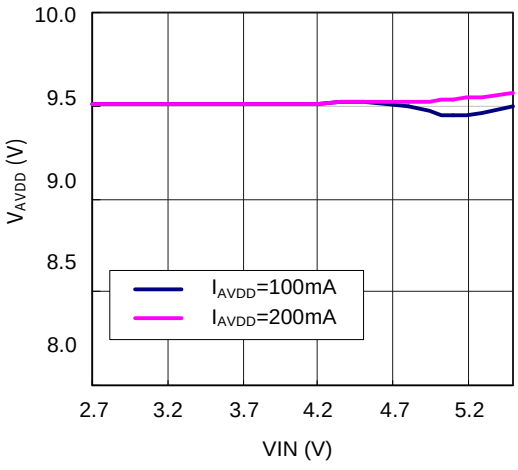
VIN vs. V_{REF}



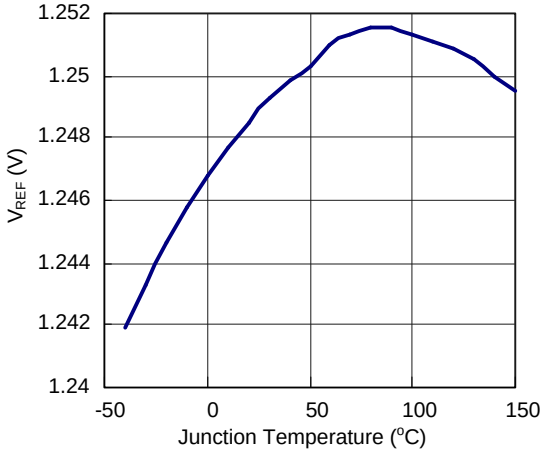
VIN vs. Fsw



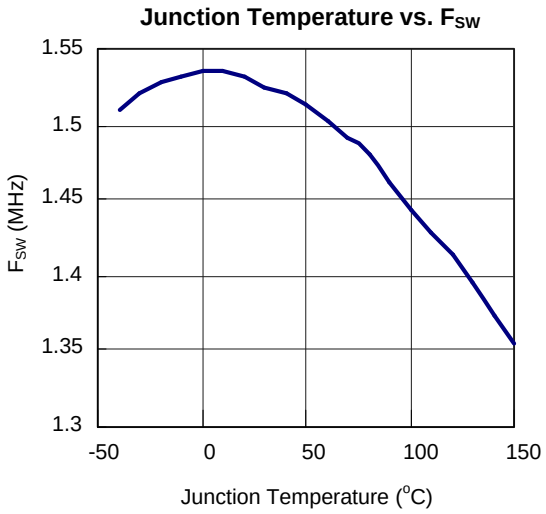
VIN vs. V_{AVDD}



Junction Temperature vs. V_{REF}



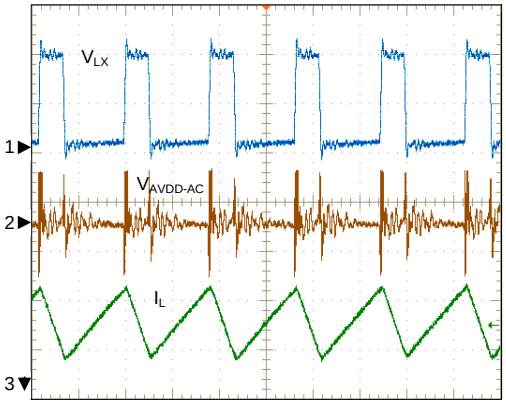
Typical Operating Characteristics



Operating Wavrforms

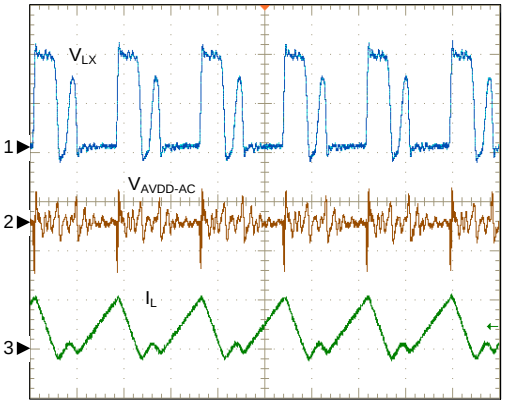
The test conditions are APW7276, VIN=3.3V, V_{AVDD}=9.5V, V_{GL}=-8.2V, V_{GH}=16.8V, V_{COM}=V_{AVDD}/2, T_A= 25°C unless otherwise specified.

Boost Converter
PWM continuous Mode: Heavy Load



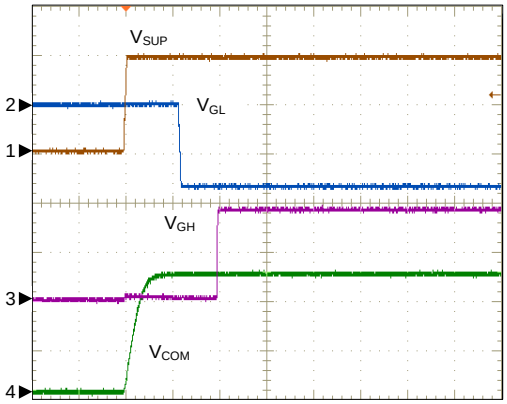
VIN=3.3V, V_{AVDD}=9.5V/300mA, L=2.2uH
CH1: V_{LX}, 5V/Div, DC
CH2: $V_{AVDD-AC}$, 100mV/Div, AC
CH3: I_L, 500mA/Div, DC
TIME: 400ns/Div

Boost Converter
PWM Discontinuous Mode: Light Load



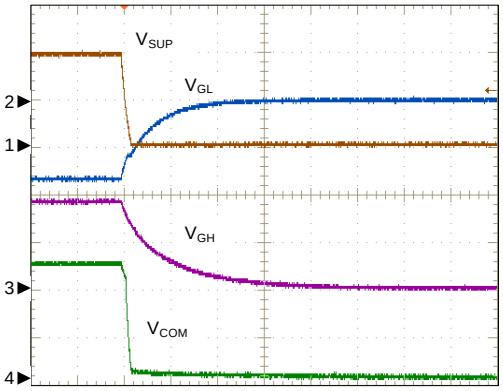
VIN=3.3V, V_{AVDD}=9.5V/50mA, L=2.2uH
CH1: V_{LX}, 5V/Div, DC
CH2: $V_{AVDD-AC}$, 100mV/Div, AC
CH3: I_L, 500mA/Div, DC
TIME: 400ns/Div

Power-On Sequence



VIN=3.3V, V_{AVDD}=9.5V/30mA,
V_{GL}=-8.2V/8.2kohm,V_{GH}=16.8V/18kohm, EN Power On
CH1: V_{SUP}, 5V/Div, DC
CH2: V_{GL}, 5V/Div, DC
CH3: V_{GH}, 10V/Div, DC
CH4: V_{COM}, 5V/Div, DC
TIME: 20ms/Div

Power-Off Sequence

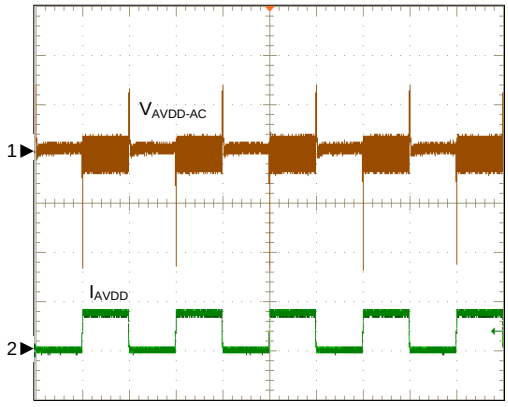


VIN=3.3V, V_{AVDD}=9.5V/30mA,
V_{GL}=-8.2V/8.2kohm, V_{GH}=16.8V/18kohm, EN Power On
CH1: V_{SUP}, 5V/Div, DC
CH2: V_{GL}, 5V/Div, DC
CH3: V_{GH}, 10V/Div, DC
CH4: V_{COM}, 5V/Div, DC
TIME: 20ms/Div

Operating Wavrforms

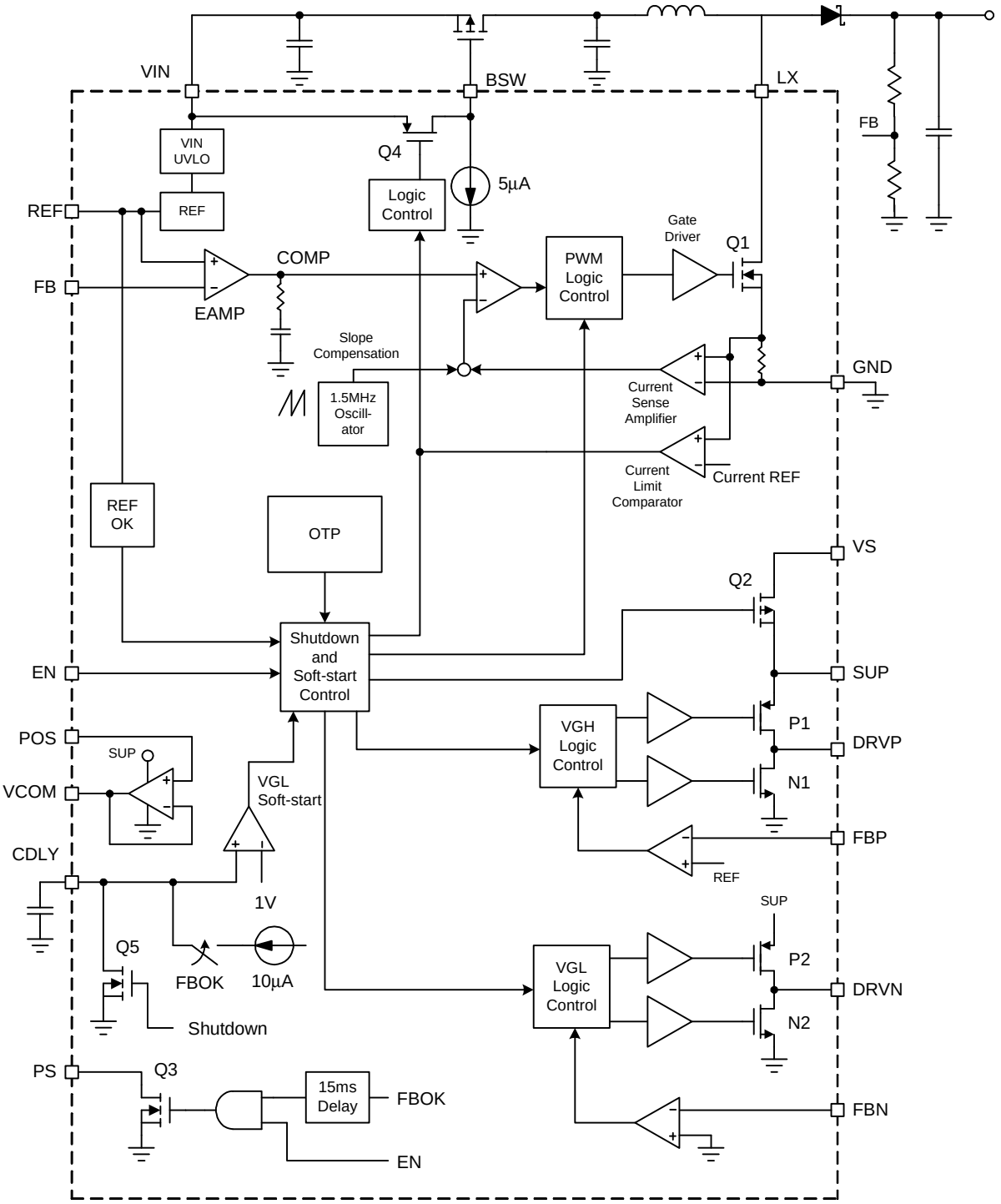
The test conditions are APW7276, VIN=3.3V, V_{AVDD}=9.5V, V_{GL}=-8.2V, V_{GH}=16.8V, V_{COM}=V_{AVDD}/2, T_A= 25°C unless otherwise specified.

Boost Converter
Load Transient Response

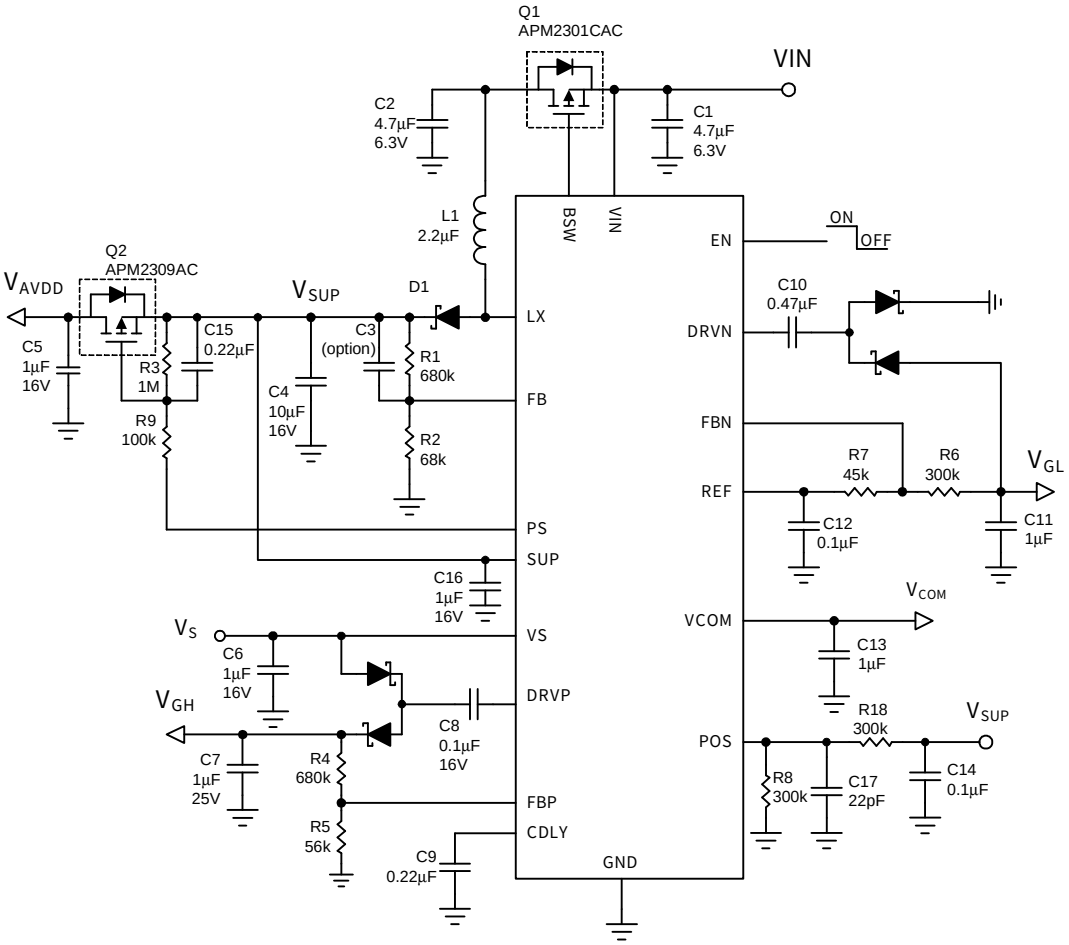


VIN=3.3V, V_{AVDD}=9.5V, L=2.2uH
CH1: $V_{AVDD-AC}$, 100mV/Div, AC
CH2: I_{AVDD}, 200mA/Div, DC
TIME: 10ms/Div

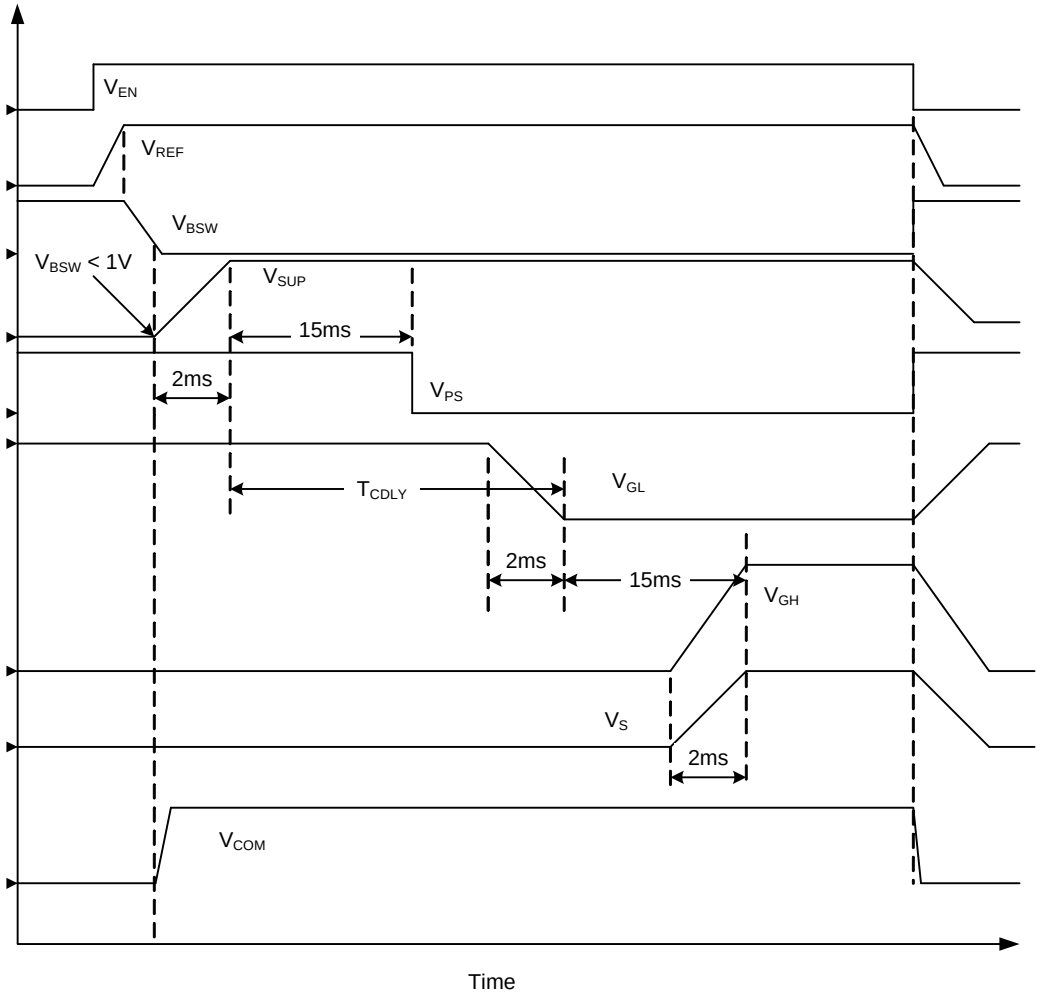
Block Diagram



Typical Application Circuit



Power On Sequence



The output voltage falling slew rate after shutdown depend on external resistance beside V_{COM}.

Function Description

VIN Under-Voltage Lockout (UVLO)

The Under-voltage lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Main Step-up Converter Control Loop

The APW7276 is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal main switch (Q1) is turned on each cycle. The peak inductor current at which EAMP turn off the Q1 is controlled by the voltage on the COMP node which is the output of the error amplifier (EAMP).

An external resistive divider connected between V_{SUP} and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slightly decrease in V_{FB} relative to the reference voltage, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current. At light load current, the COMP voltage is low. The APW7276 auto skips pulse.

Pulse Skip Modulation

APW7276 auto skip pulse at light load.

Main Step-up Converter Current Limit

The APW7276 integrated a current-limit-comparator in main step-up converter. It monitors the inductor current, flows through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the APW7276 from damaging during overload or short-circuit conditions.

V_{REF}

The V_{REF} initiates soft-start process after POR and EN goes high. Shutdown if POR and EN goes low.

CDLY

Connecting a capacitor from this pin to GND allows the setting of delay time between V_{GL} and V_{SUP}. Once the V_{SUP} soft-start process enabled, an internal 10μA current source starts to charge C_{DLY}, the V_{GL} channel initiates soft-start process once V_{CDLY} exceed 1V. If the V_{CDLY} exceeds 1V before V_{SUP} start up, the V_{SUP} and V_{GL} start up simultaneously.

BSW

Once V_{REF} is within 8% of its normal regulated output voltage, an internal current source from the BSW to GND to pull BSW low. Once the V_{BSW} below 1V, the step-up converter initiates soft-start process. The V_{BSW} pull to VIN if main step-up current limit detected without delay, EN pull low or VIN below POR.

PS

This is the gate drive pin which can be used to control an external MOSFET switch to provide input to output isolation of V_{SUP} or V_{AVDD}. See the Typical Application Section. PS is an open-drain output and is latch low as soon as the step-up converter is within 10% of its normal regulated output voltage for 15ms. GD goes high impedance when the EN input voltage is cycle low.

An Isolation Switch from VSUP to VS (Q2)

The VS is the voltage source of positive charge pump, V_{GH}. As soon as the V_{GL} start-up for 15ms, the P-FET, Q2, switch soft on. The Q2 fully turns on after 2ms. The Q2 turns off at Q1 current limit detected and EN goes low.

Operational Amplifier

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. They feature ±100mA output short-circuit current, 13V/μs slew rate, and 8MHz bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Function Description (Cont.)

Positive Charge Pump

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external Resistive voltage-divider from its output to GND with the midpoint connected to FBP. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer as shown in Figure 1. During the first half-cycle, N1 turns on and charges flying capacitors C8 (Figure 1). During the second half cycle, N1 turns off and P1 turns on, level shifting C8 by V_{SUP} volts. The amount of charge transferred to the output is determined by the error amplifier that controls P1's on-resistance. The positive charge-pump regulator's startup can be delayed from negative charge pump after 15ms, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V. The soft-start period is 2ms (typ). The soft-start feature effectively limits the inrush current during startup.

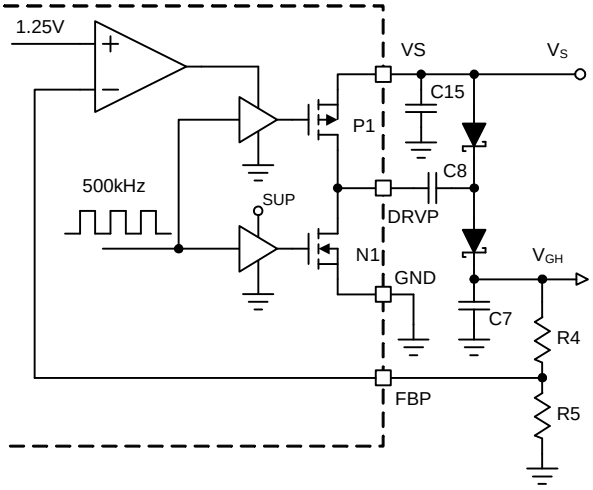


Fig1. Positive Charge Pump Regulator Block Diagram

Negative Charge Pump

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 2.

During the first half cycle, P2 turns on, and flying capacitor C10 charges to V_{SUP} minus a diode drop (Figure 2). During the second half cycle, P2 turns off, and N2 turns on, level shifting C10. This connects C10 in parallel with reservoir capacitor C11. If the voltage across C11 minus a diode drop is greater than the voltage across C10, charge flows from C11 to C10 until the diode (D5) turns off. The amount of charge transferred from the output is determined by the error amplifier, which controls N2's on-resistance.

The negative charge-pump regulator is enabled when the step-up regulator reaches regulation and V_{CDLY} exceed 1V. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 0mV. The soft-start period is 2ms typically. The soft-start feature effectively limits the inrush current during startup.

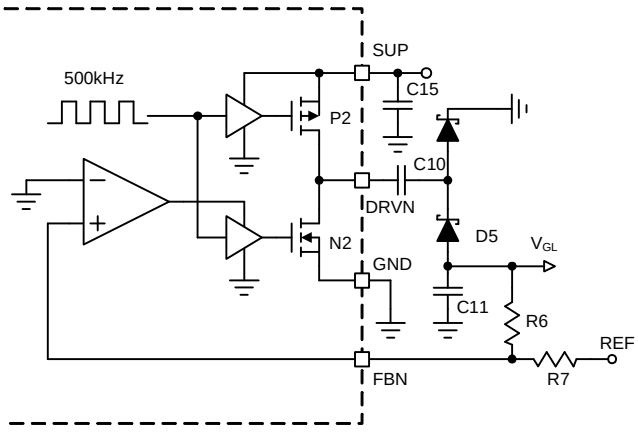


Fig2. Negative Charge Pump Regulator Block Diagram

Function Description (Cont.)

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7276. When the junction temperature exceeds 160°C, a thermal sensor turns off the power MOSFET allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulates the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions increasing the lifetime of the device.

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor C1 and C16 should be placed close to the VIN/SUP and GND. Connecting the capacitor with VIN/SUP and GND pins by short and wide tracks for filtering and minimizing the input voltage ripple.
2. The inductor and Schottky diode should be placed as close as possible to the LX pin to minimize length of the copper tracks as well as the noise coupling into other circuits.
3. A star ground connection or ground plane minimizes ground shifts and noise is recommended.
4. Since the feedback pin (FBx) and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

TQFN3x3-20

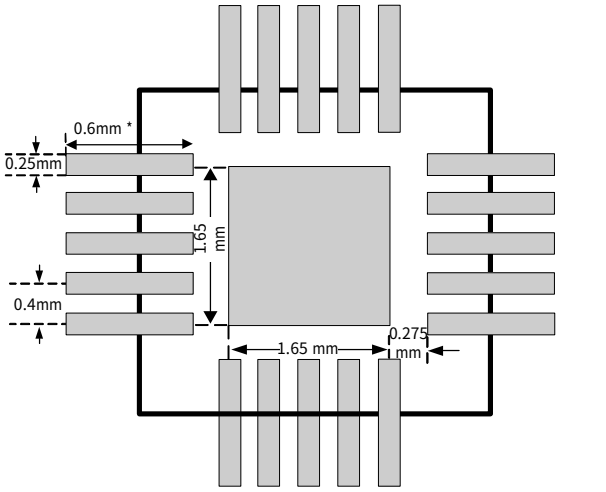
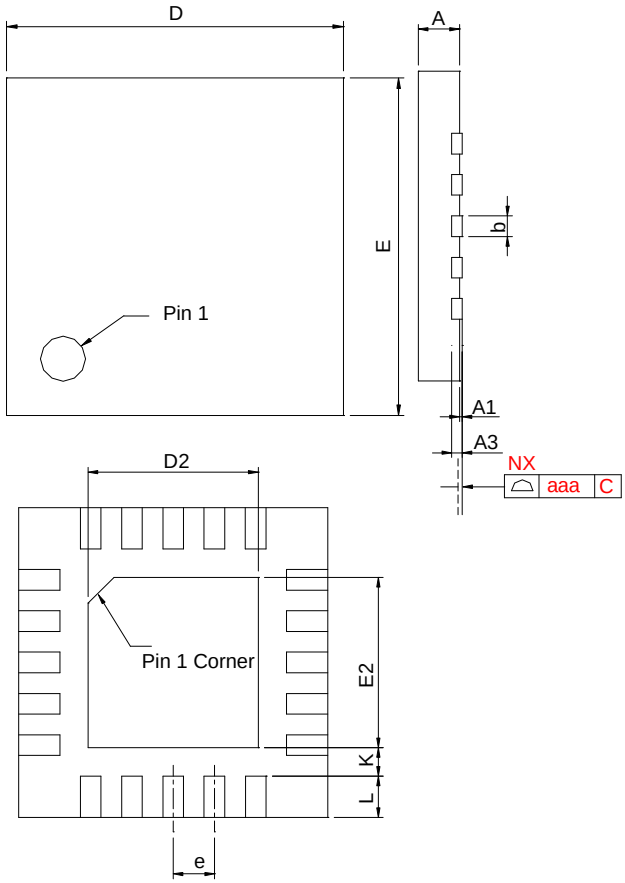


Figure 3. Recommended Minimum Footprint

Package Information

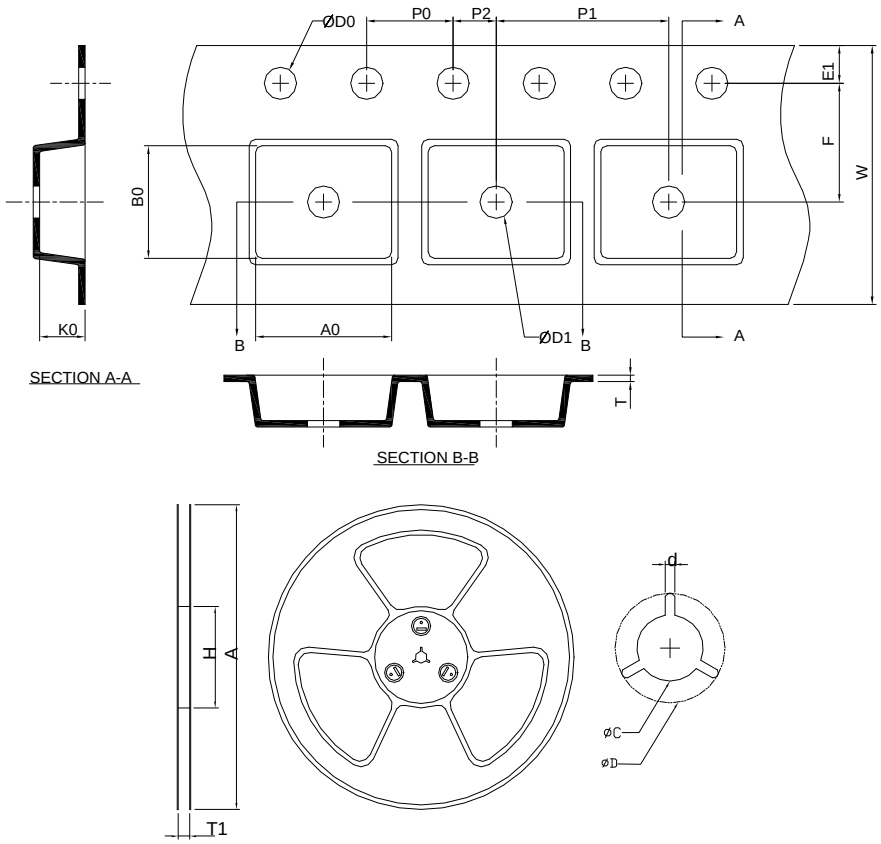
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

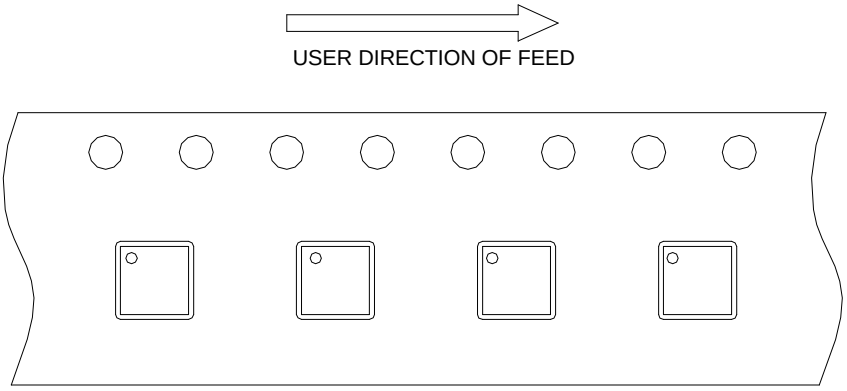
(mm)

Devices Per Unit

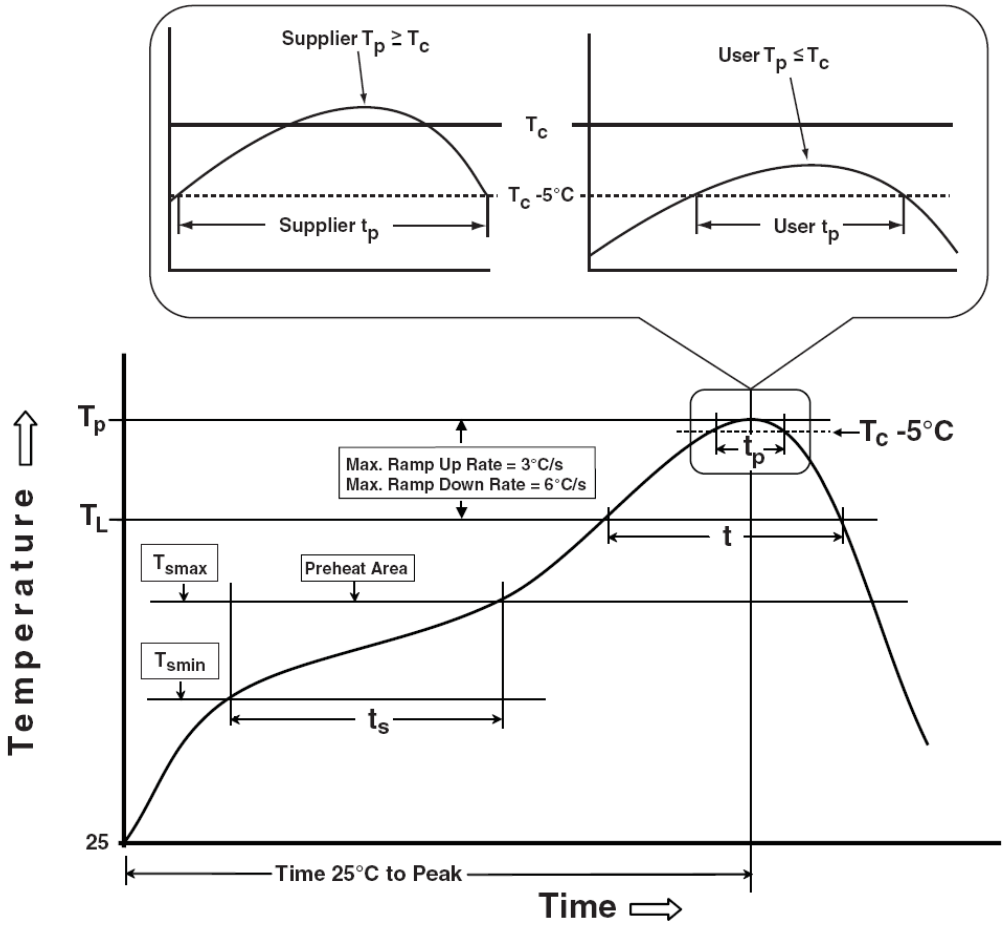
Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838