APW7564

5V/0.3A, Ultra Low Iq Buck Converter

Features

- **Wide Input Voltage from 2.7V to 5.5V**
- **3uA Low Quiescent Current at Switching State**
- **2% Output Voltage Accuracy**
- **Output Discharge Function**
- **Over Temperature Protection**
- **Hiccup Short-Circuit Protection**
- **I^2C Interface**
  - **Programmable Output Voltage from 0.5V to 1.13V (10mV/Step)**
  - **Adjustable Output Voltage Ramp Slew Rate**
- **Tiny WLCSP 0.8x1.14-6 Package**

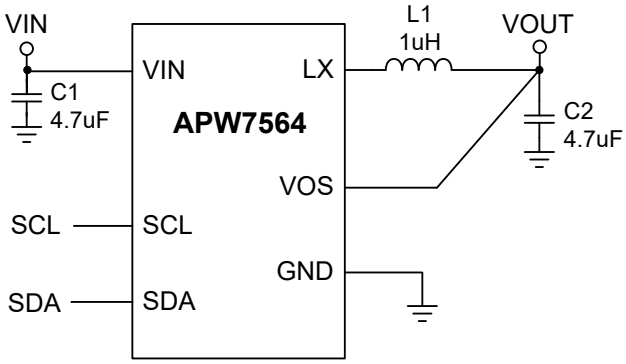
General Description

APW7564 is a high-frequency synchronous buck converter with I^2C Interface. The APW7564, design with a COT control scheme, can convert wide input voltage of 2.7V to 5.5V to the output voltage adjustable from 0.5V to 1.13V by I2C to provide an efficient, flexible DC/DC solution.

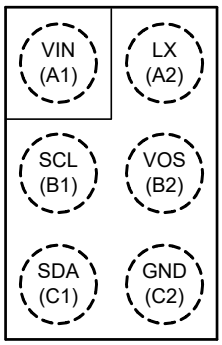
The APW7564 is equipped with an automatic PFM/PWM mode operation. At light load, the IC operates in the PFM mode to reduce the switching losses. At heavy load, the IC works in PWM mode.

The APW7564 is also equipped with Power-On-Reset, Soft Start, Enable/Shutdown and whole protections (under-voltage, current-limit and over-temperature) into a tiny package. This device, available WLCSP 0.8x1.14-6 package and provides a very compact system solution external components and PCB area.

Simplified Application Circuit



Simplified Application Circuit

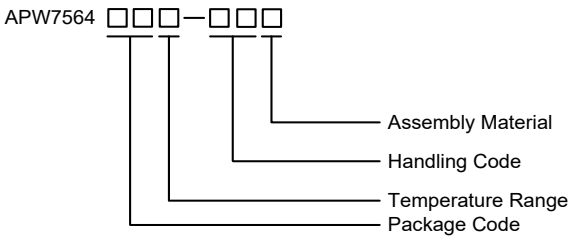


WLCSP 0.8x1.14-6
(Top View)

Applications

- **Portable Electronics**
- **TWS Applications**
- **Wearable Electronic**
- **Mobile Phones**

Ordering and Marking Information



Package Code
HA : WLCSP 0.8x1.14-6
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Green Part

X - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 7	V
V_{LX}	LX to GND Voltage	-0.3 ~ 7	V
Other Pins	VOS, SCL and SDA to GND Voltage	-0.3 ~ 7	V
T_J	Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	100	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN to GND Voltage	2.7 ~ 5.5	V
V_{OUT}	Adjustable Output Voltage Range	0.5 ~ 1.13	V
I_{OUT}	Converter Output Current	0 ~ 300	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.8V at T_A=25°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
APPLICATION RANGE						
V_{IN}	Input Voltage Range		2.7	-	5.5	V
V_{OUT}	Range of Output Voltage		0.5	-	1.13	V
I_{OUT}	Range of Output Current		-	-	300	mA
	Voltage Setting Step Value		-	10	-	mV
	Dynamic Voltage Rising Slew Rate	Rising Slew Rate Per 10mV/step	-	10	-	us
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	VIN=3.8V, Enable Bit=1, Switching	-	3	-	uA
I_{VIN_SDH}	VIN Shutdown Supply Current	Enable Bit=0, VIN=3.8V	-	0.7	1	uA
POWER-ON-RESET						
$V_{IN\_POR\_R}$	VIN POR Voltage Threshold	VIN Rising	-	2.3	2.5	V
$V_{IN\_POR\_Hys}$	VIN POR Hysteresis		-	200	-	mV
OUTPUT VOLTAGE						
V_{OS}	Output Voltage	VIN=3.8V, No Load, 25°C	-	0.9	-	V
		VIN=3.8V, IOUT=100mA, All Temperature	0.882	0.9	0.918	V
	VOS Leakage Current	VOUT=0.9V	-	0.5	-	uA
	Load Regulation	VIN=3.8V, IOUT=0A to 300mA	-	0.3	-	%/A
	Line Regulation	VIN=2.7 to 5.5V, IOUT=300mA	-	0.4	-	%/V
	Load Transient	Load current from 50mA to 300mA, Load Transient Slew Rate=300mA/us, VIN=3.8V, VOUT=0.9V	-	5	-	%
POWER MOSFET						
	High Side P-MOSFET Resistance	VIN=3.8V, ILX=0.1A, TA=25°C	-	300	-	mΩ
		VIN=3.8V, ILX=0.1A, TA= -40 ~ 85°C	-	400	-	mΩ
	Low Side N-MOSFET Resistance	VIN=3.8V, ILX=0.1A, TA=25°C	-	150	-	mΩ
		VIN=3.8V, ILX=0.1A, TA= -40 ~ 85°C	-	200	-	mΩ
ILX_H	High Side MOSFET Leakage Current	VIN=5V, VLX=0V, Enable Bit=0	-	-	1	uA
ILX_L	Low Side MOSFET Leakage Current	VIN=5V=VLX, Enable Bit=0	-	-	1	uA
PROTECTIONS						
I_{LIM_VAL}	Valley Current Limit		-	200	-	mA
T_{OTP}	Over-Temperature Trip Point		-	150	-	°C
	Over-Temperature Hysteresis		-	20	-	°C
	Under-Voltage Protection Threshold	VOUT Falling	-	60	-	%V_{OUT}
	Released Under-Voltage Protection	VOUT Rising	-	70	-	%V_{OUT}
	Hiccup Time	at UVP or Short Output Condition	-	3.4	-	ms
SOFT_START, INPUT CURRENTS and COMPONENTS						
T_{SS}	Soft-Start Time	From 0% of V_{OUT} to 95% of V_{OUT}, V_{OUT}=0.9V	-	100	-	us
V_{ZC}	ZC Offset		-	±5	-	mV
	Output Discharge Resistance	Enable Bit=0, UVP or OTP	-	100	-	Ω
	Input Capacitor		-	4.7	-	µF
	Output Capacitor		-	4.7	-	µF
	External Inductor		1	-	-	µH

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=3.8V at T_A=25°C.

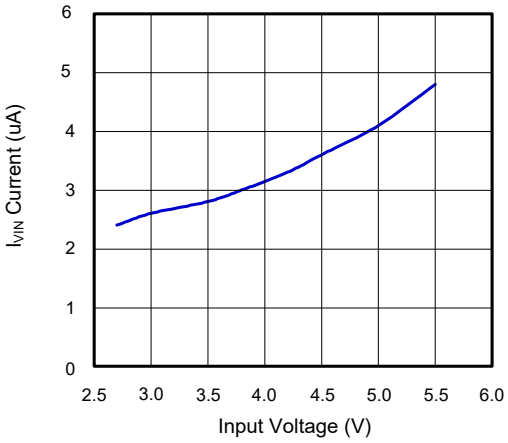
Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
I/O PIN CHARACTERISTICS (SDA, SCL)						
V_{IL}	Input Low Voltage	Include SDA, SCL	-	-	0.25	V
V_{IH}	Input High Voltage	Include SDA, SCL	1.5	-	-	V
I_{BIAS_IO}	High Level Leakage Current	Pull up to 5V, Include SDA, SCL Input Pins	-	-	1	μA
f_{SCL}	SCL Clock Frequency		100	-	400	kHz

Pin Description

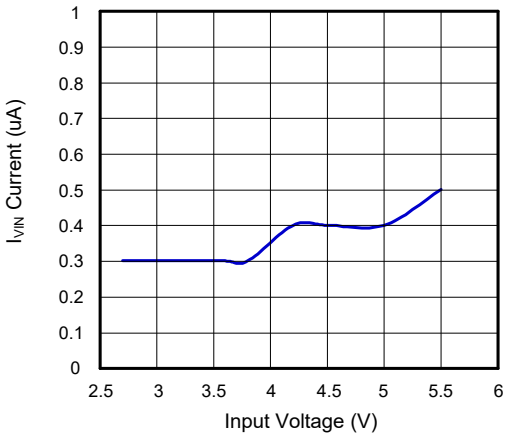
PIN		FUNCTION
NO.	NAME	
A1	VIN	Input Power. In order to get better thermal dissipation, all layers, top to bottom, below to VIN PAD define as VIN plane and connected by via holes. It is also to recommend having larger area than VIN PAD as shown in the layout example. A high frequency 4.7uF ceramic, X5R type or better must be placed as close to these pins as possible connected to GND pin.
B1	SCL	Digital Clock.
C1	SDA	Digital Data.
A2	LX	Power switching output. It is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
B2	VOS	Output sense pin.
C2	GND	Power and signal ground.

Typical Operating Characteristics

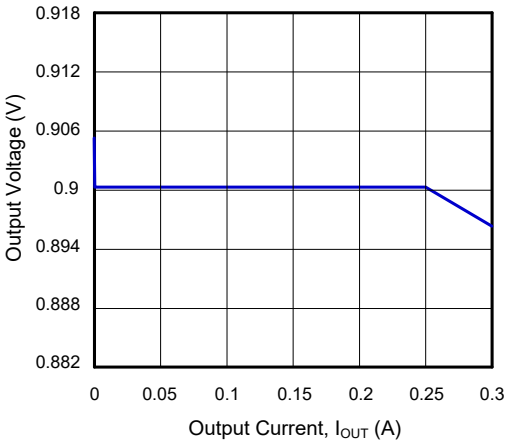
Switching Current, No Load
EN bit = 1



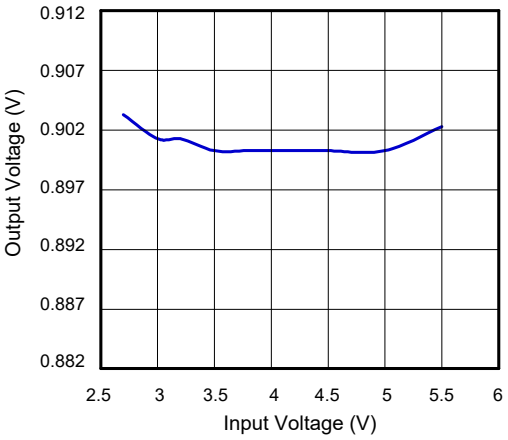
Shutdown Current
EN bit = 0



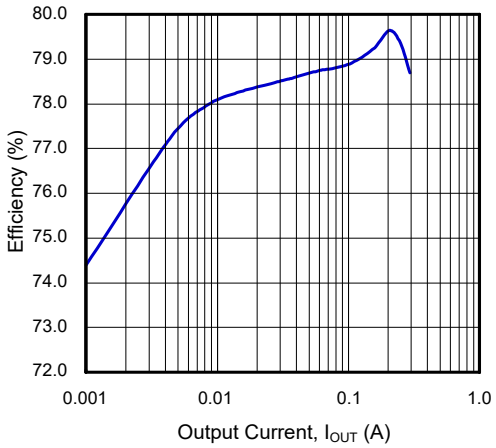
Load Regulation



Line Regulation

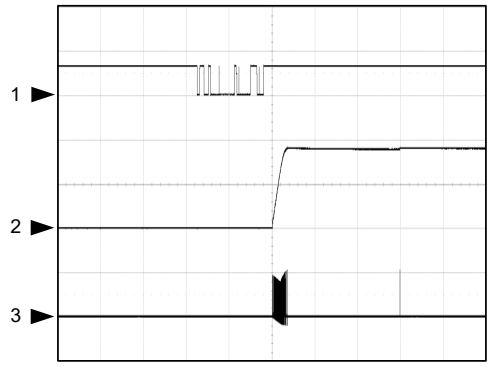


Efficiency vs. Output Current



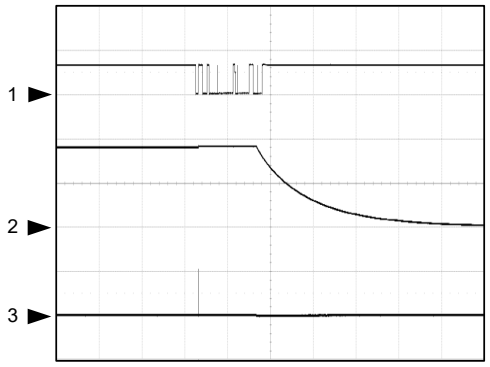
Operating Waveforms

Enabled by I2C



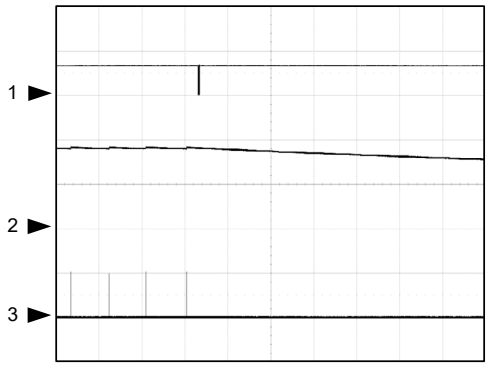
CH1: V_{SDA} (5V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 500μs/div

Shutdown by I2C with Discharge



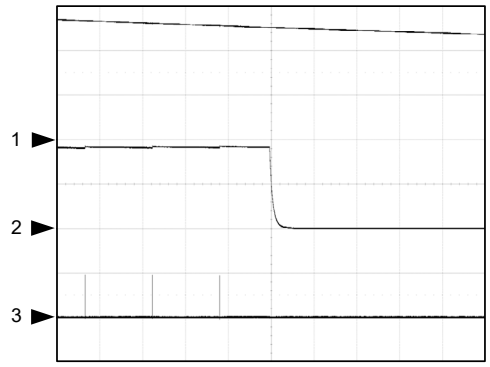
CH1: V_{SDA} (5V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 500μs/div

Shutdown by I2C with No Discharge



CH1: V_{SDA} (5V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 20ms/div

Power Off VIN with Discharge



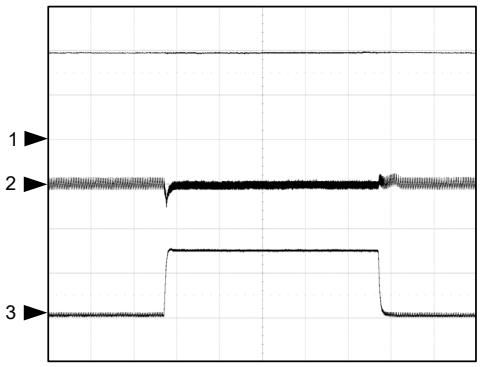
CH1: V_{IN} (1V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 10ms/div

Operating Waveforms (Cont.)

Short VOUT to GND

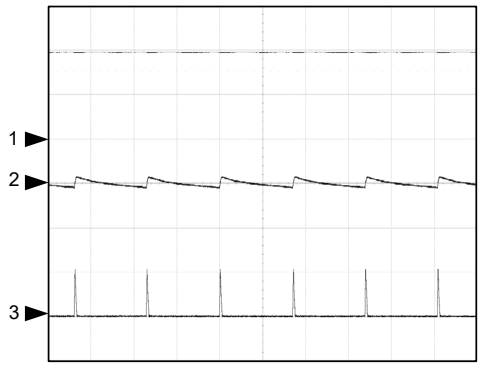
CH1: V_{IN} (2V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 1ms/div

Load Transient, 0A ←→ 300mA



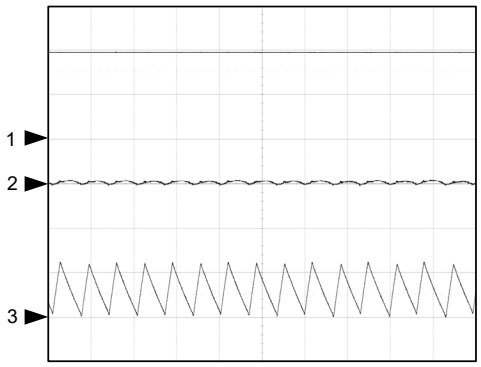
CH1: V_{IN} (2V/div)
CH2: V_{OUT} (AC,100mV/div)
CH3: I_{OUT} (200mA/div)
Time: 200µs/div

VOUT Ripple, IOUT=10mA



CH1: V_{IN} (2V/div)
CH2: V_{OUT} (AC,100mV/div)
CH3: I_L (500mA/div)
Time: 5µs/div

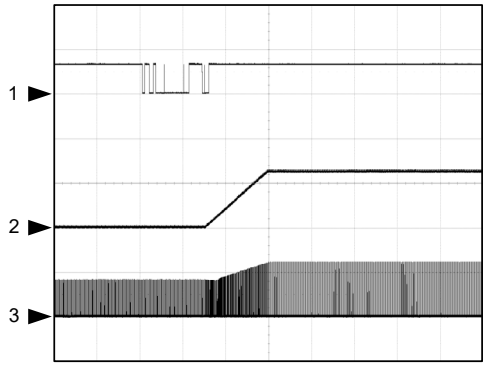
VOUT Ripple, IOUT=300mA



CH1: V_{IN} (2V/div)
CH2: V_{OUT} (AC,100mV/div)
CH3: I_L (500mA/div)
Time: 500ns/div

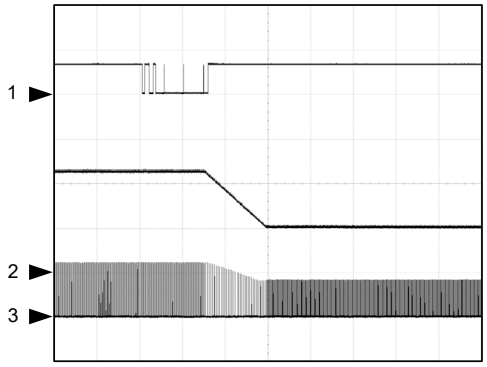
Operating Waveforms (Cont.)

DAC, VOUT from 0.5V to 1.13V,
IOUT=10mA



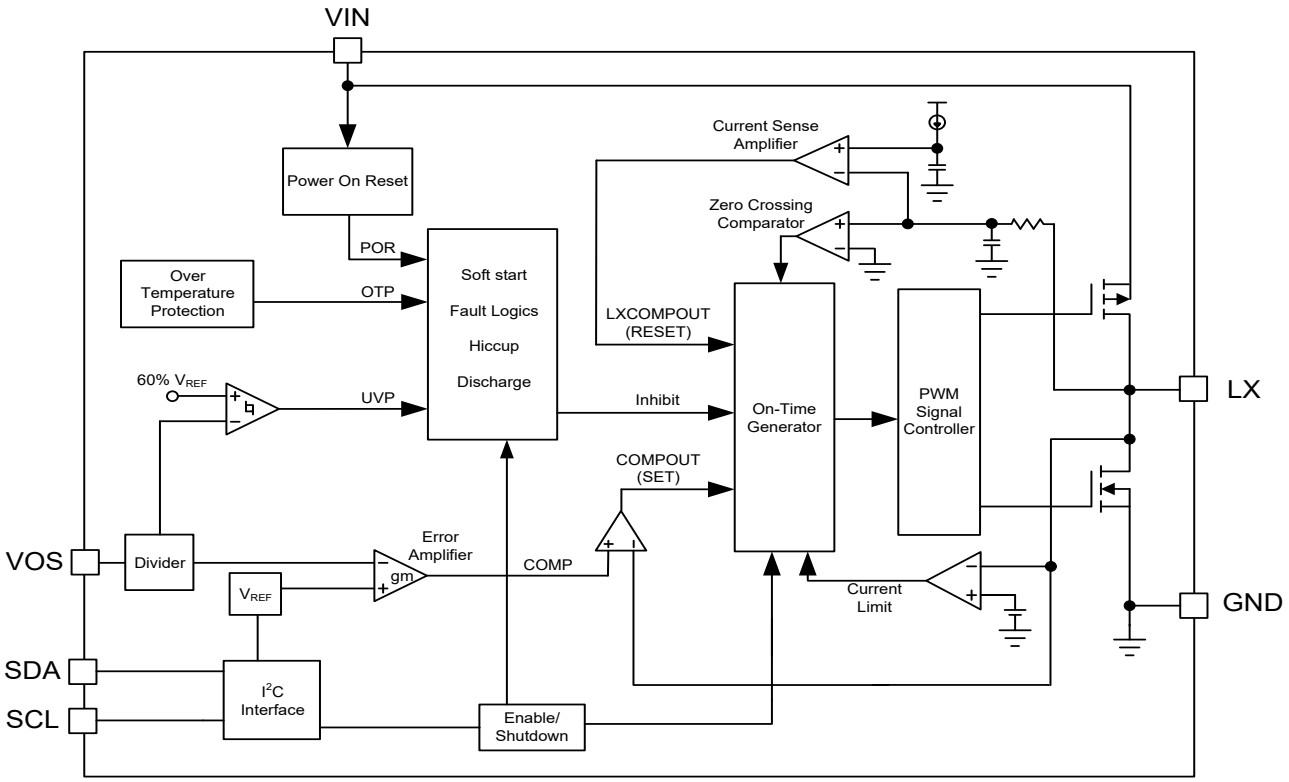
CH1: V_{SDA} (5V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 500μs/div

DAC, VOUT from 1.13V to 0.5V,
IOUT=10mA

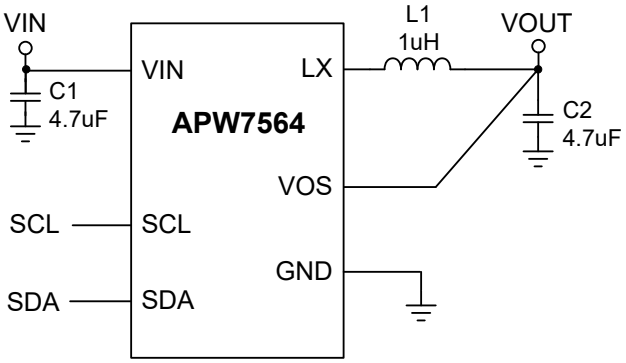


CH1: V_{SDA} (5V/div)
CH2: V_{OUT} (500mV/div)
CH3: I_L (500mA/div)
Time: 500μs/div

Block Diagram



Typical Application Circuit



Function Description

The APW7564 is a high-frequency synchronous step-down converter with ultra-low quiescent current consumption and flexible output voltage by I²C interface. It offers the lowest total solution cost that can provide up to 300mA continuous output current over wide input supply range. Input voltage range of the PWM converter is 2.7V to 5.5V. The output voltage is adjustable from 0.5V to 1.13V to provide the best solution of DC/DC.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The COT control mode can support output MLCC capacitor application currently through internal circuit designed. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage.

In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

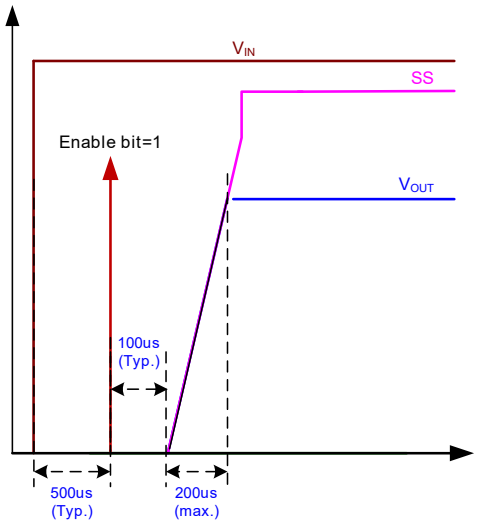
Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VIN voltage is low. The POR function continually monitors the input supply voltage on the VIN pin. When the rising VIN voltage reaches the rising POR voltage threshold (2.3V Typical), the POR signal goes high and the chip initiates I²C operations. There is a hysteresis to POR voltage threshold (about 200mV Typical). When VIN voltage drops lower than 2.1V (Typical), the POR disables the chip.

Soft-Start

The APW7564 has soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate.

It shows V_{OUT} soft-start sequence as below chart. When the Enable bit=1 and VIN is above the rising POR threshold, the device initiates a soft-start process to ramp up the output voltage.



Before the internal power good signal goes high, the under voltage protection is prohibited. The current limit protection function is enabled. If the output capacitor has residue voltage before startup, both internal low-side and high-side MOSFETs are in off-state until the internal soft start voltage equal the VOUT voltage. This will ensure the output voltage starts from its existing voltage level.

Under Voltage Protection

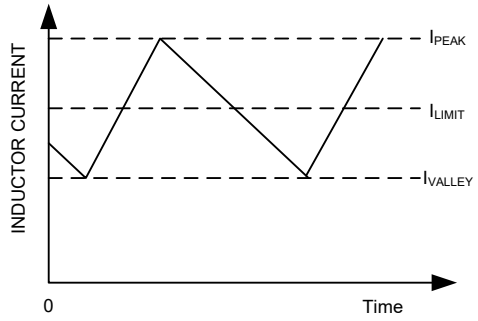
In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after internal soft start signal is okay. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (60% of normal output voltage), the APW7564 enters hiccup mode to periodically restart the part (wait for 3.4ms). This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The APW7564 exits the hiccup mode once the output voltage V_{OS} bigger than UVP Hysteresis (Typical: 10%).

Function Description (Cont.)

PWM Converter Current Limit

The current-limit circuit employs a “valley” current-sensing algorithm (See Figure 2). The APW7564 uses the low-side MOSFET’s RDS(ON) of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at LX pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

The PWM controller uses the low-side MOSFETs on-resistance RDS(ON) to monitor the current for protection against shortened outputs. The MOSFET’s RDS(ON) is varied by temperature and gate to source voltage, the user should determine the maximum RDS(ON) in manufacture’s datasheet.



Over Temperature Protection

An over-temperature protection circuit limits the junction temperature of APW7564. When the junction temperature exceeds +150°C, PWM converter is shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 20°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

I²C Programming

I²C Serial Control Interface

The APW7564 has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz) and fast mode (400-kHz) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.
The DAP supports the standard-mode I²C bus operation (100kHz maximum) and the fast I²C bus operation (400kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system.
Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.
The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The APW7564 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.
Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

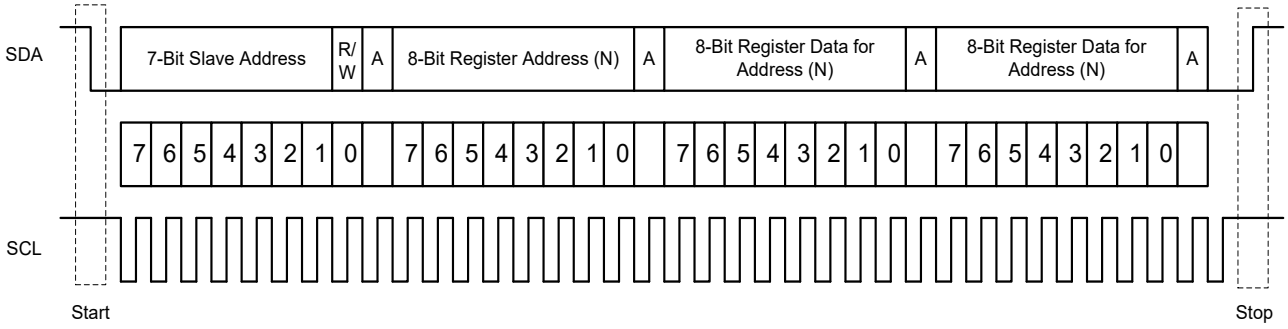


Figure 1. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. **The device 7-bit address is defined as "1100100" (64H).**

Single-Byte Transfer

The serial control interface supports single-byte read/write operations for sub-addresses 0x00 to 0xFF.
Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7564 also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7564. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

I²C Programming (Cont.)

Single-Byte Write

As shown in Figure 2, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7564 internal memory address being accessed. After receiving the address byte, the APW7564 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7564 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

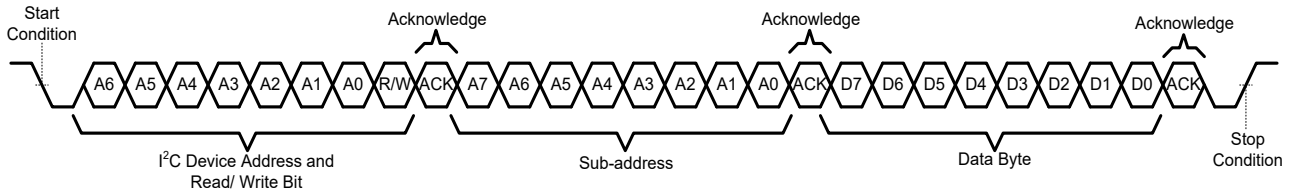


Figure 2. Single-Byte Write Transfer

Single-Byte Read

As shown in Figure 3, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read.
As a result, the read/write bit becomes a 0. After receiving the APW7564 address and the read/write bit, APW7564 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7564 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the APW7564 again responds with an acknowledge bit. Next, the APW7564 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

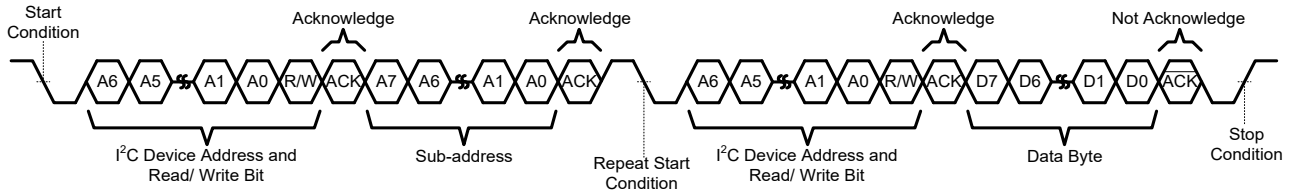


Figure 3. Single-Byte Read Transfer

I²C Programming (Cont.)

I²C Control Timing			Min.	Typ.	Max.	Unit
	SDA and SCL Leakage Current		-	0.01	1	μA
F_{I2C}	I²C Operating Frequency		-	-	100 400	kHz
T_{BUF}	I²C Free Time Between Stop and \Start Condition	SCL=100kHz SCL=400kHz	4.7 1.3	- -	- -	μs
$T_{\_HD\_STA}$	Hold Time After Start Condition	After this period, the first clock is generated SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
$T_{\_SU\_STA}$	Repeated Start Condition Setup Time	SCL=100kHz SCL=400kHz	4.7 0.6	- -	- -	μs
$T_{\_SU\_STO}$	Stop Condition Setup Time	SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
$T_{\_HD\_DAT}$	Data Hold Time	SCL=100kHz SCL=400kHz	0 0	- -	- -	ns
$T_{\_SU\_DAT}$	Data Setup Time	SCL=100kHz SCL=400kHz	250 100	- -	- -	ns
$T_{\_LOW}$	Clock Low Period	SCL=100kHz SCL=400kHz	4.7 1.3	- -	- -	μs
$T_{\_HIGH}$	Clock High Period	SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
T_F	Fall Time of I²C SDA	SCL=100kHz SCL=400kHz	0 0	- -	300 300	ns
T_F	Fall Time of I²C SCL	SCL=100kHz SCL=400kHz	0 0	- -	300 300	ns
T_R	Rise Time of I²C SDA	SCL=100kHz SCL=400kHz	- 20+0.1 C_b	- -	1000 300	ns
T_R	Rise Time of I²C SCL	SCL=100kHz SCL=400kHz	- 20+0.1 C_b	- -	300 300	ns
C_b	Capacitive Load for Each Bus Line	SCL=100kHz SCL=400kHz	- -	- -	400 400	pF

Timing Diagram

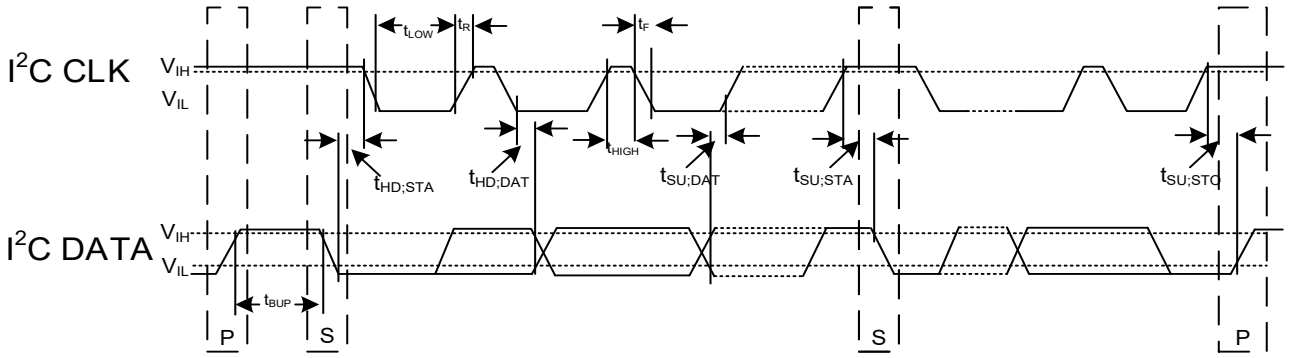


Figure 4: I²C Common AC Specification

Register Map

Address	Name	Default Value
00h	OUTPUT VOLTAGE CODE	0x28
01h	CONTROL LOGIC	0x06
02h	IC PRODUCT ID/ IC VERSION	0x1X

REG0x00

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED		VOS VOLTAGE[0:5]					
Read/Write	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			1	0	1	0	0	0

Bit Name	Bit Definition
RESERVED[6:7]	No Used.
VOS VOLTAGE[0:5]	VOS Output Voltage Code, 10mV/step. 000000 : 0.5V 000001 : 0.51V 000010 : 0.52V 000011 : 0.53V . . . **101000 : 0.9V (Default)** . . . 111111 : 1.13V

REG0x01

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED				TRS[2:3]		DISCHARGE	ENABLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	1	0

Bit Name	Bit Definition
RESERVED[4:7]	No Used.
TRS[2:3]	Output Ramp Seed Time Setting. 00 : VOS ramp speed time=20us/step, 1step=10mV **01 : VOS ramp speed time=10us/step, 1step=10mV (Default)** 10 : VOS ramp speed time=2usV/step, 1step=10mV 11 : VOS ramp speed time=1us/step, 1step=10mV
DISCHARGE[1]	Output Voltage Discharge Bit. 0 : Output Discharge Disable **1 : Output Discharge Enable (Default)**
ENABLE[0]	IC Enable-Shutdown Bit. **0 : IC Shutdown (Default)** 1 : IC Enable

Register Map (Cont.)

REG0x02

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PRODUCT ID[4:7]				IC REVISION[0:3]			
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	1	X	X	X	X
Bit Name	**Bit Definition**							
PRODUCT ID[4:7]	**APW7564 – 0001 (Default)**							
IC REVISION[0:2]	IC Revision. 0001 – revision 1 0010 – revision 2 0011 – revision 3 0100 – revision 4 . . .							

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes.

Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\times \Delta I_L}$$

$$I_{L(MAX)}=I_{OUT(MAX)}+\frac{1}{2}\Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT}=\frac{I_{RIPPLE}}{8_{COUT}\times F_{SW}}$$

$$R_{ESR}=I_{RIPPLE}\times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered. To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.

2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.

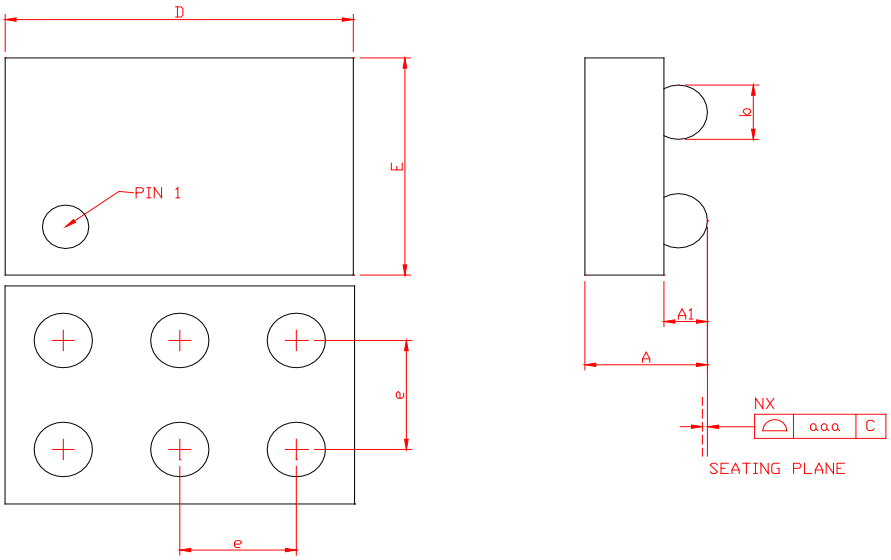
3. The output capacitor should be place closed to converter V_{OUT} and GND.

4. Since the feedback network is a high impedance circuit, the feedback network should be routed away from the inductor. The feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

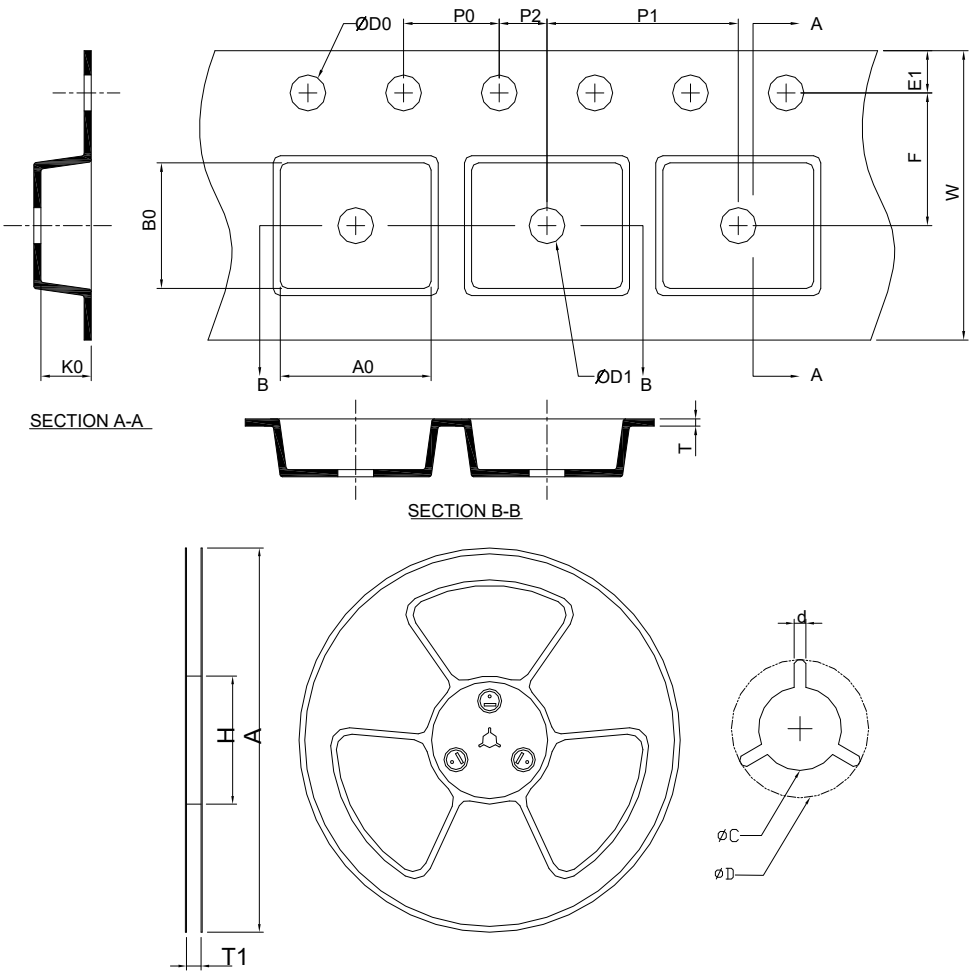
Package Information

WLCSP 0.8x1.14-6



SYMBOL	WLCSP 0.8x1.14-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.45	0.60	0.018	0.024
A1	0.15	0.25	0.006	0.010
b	0.22	0.30	0.009	0.012
D	1.14	1.20	0.045	0.047
E	0.80	0.86	0.031	0.034
e	0.40 BSC		0.016 BSC	
aaa	0.03		0.001	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP 0.8x1.14	178.0±2.00	50 MIN.	9.0+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.20	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.3 MIN.	0.2±0.05	0.98±0.05	1.48±0.05	0.68±0.05

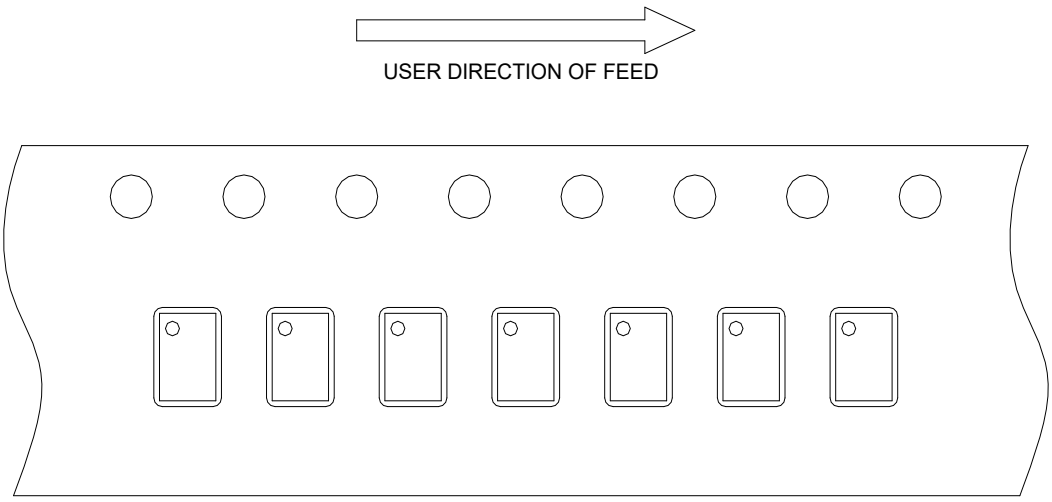
(mm)

Devices Per Unit

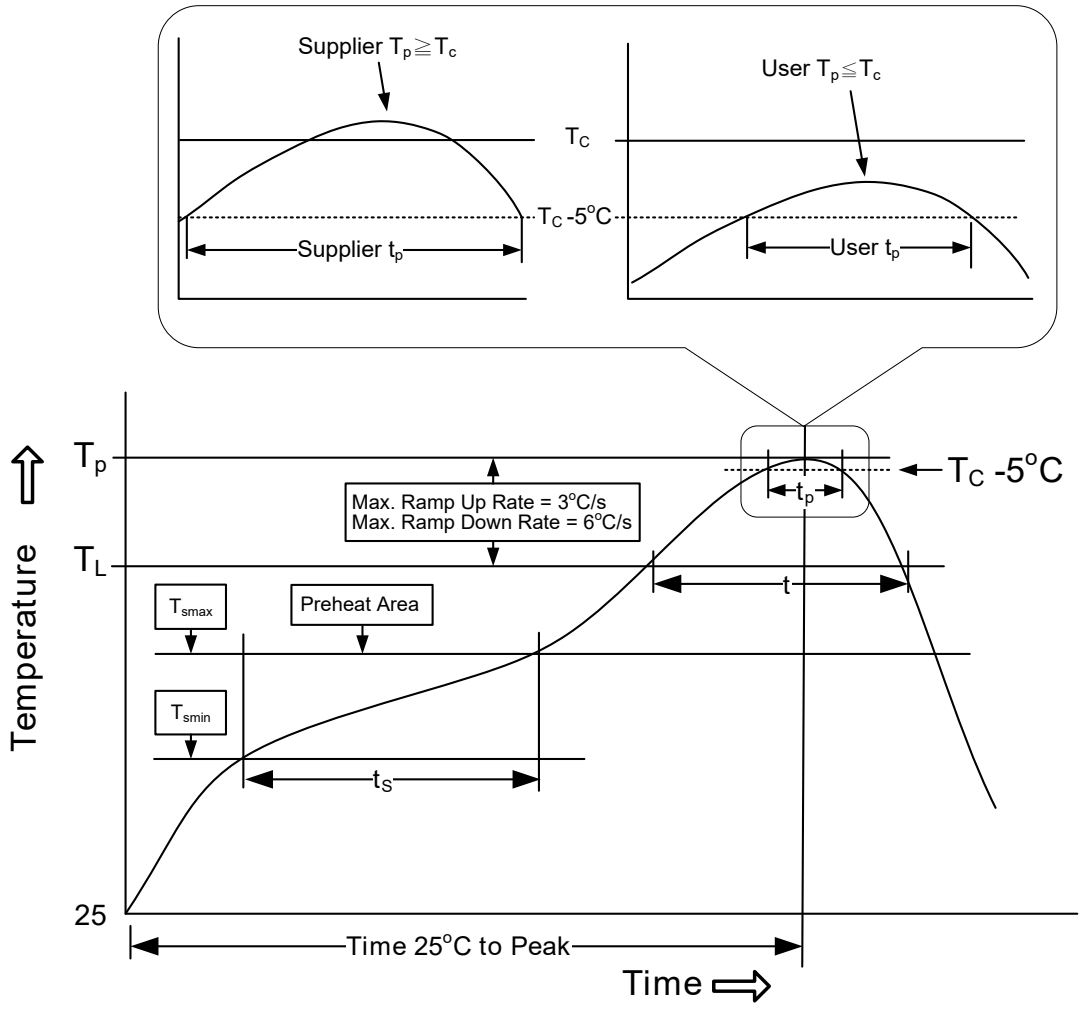
Package Type	Packing	Quantity
WLCSP 0.8x1.14	Tape & Reel	3000

Taping Direction Information

WLCSP 0.8x1.14-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test Item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD-78	10ms, 1_{tr} ≧ 100mA

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