1.5MHz PMIC for DVR with I²C Controller

Features

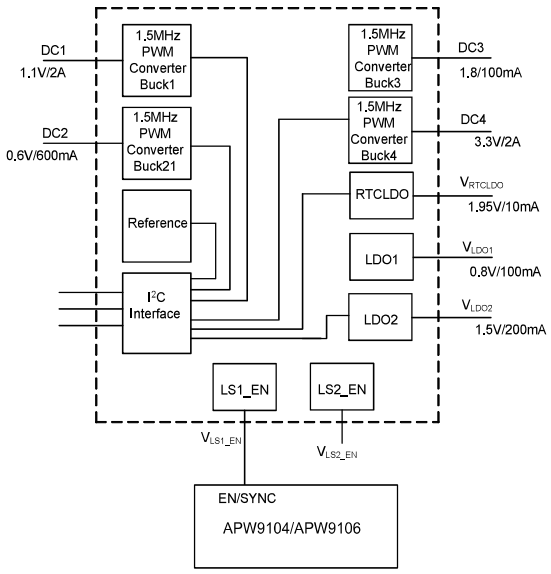
■ Voltage Rail

- **Provide 4 Buck Single Phase PWM Converters**
  - **DC1: 0.6V - 1.5V at 2.5A**
  - **DC2: 0.6V - 3.3V at 1.5A**
  - **DC3: 0.6V - 3.3V at 1A**
  - **DC4: 0.6V - 3.3V at 2A**
- **Provide 3 LDO Output**
  - **RTCLDO 1.5V-3.05V, 10mA**
  - **LDO1 0.6V-3.3V, 150mA, Reference=0.6V**
  - **LDO2 1.5V-3.05V, 300mA, Controlled by I²C**
- **Provide 2 Load Switches Enable Signal**
- **Current Limit Protection**
- **Output Under-Voltage Protection**
- **Output Over-Voltage Protection for Bucks**
- **Thermal Shutdown Protection**
- **TQFN 5x5-40B Package**

General Description

The APW7704C is a Power Management IC (PMIC) designed to provide complete Power Management solution for the driving video recorder (DVR) applications. The APW7704C is designed to provide maximum number of regulators in the smallest available cost effective package. Included in the IC are: Four Synchronous Buck Converters for DC1 ~ DC4; Three LDOs with one for RTC application, and Two Load Switch Enable Signal Control for external load switches application. For the Bucks, the IC is equipped with all the standard protection features such as current limit, over voltage and internal under voltage protection as well as thermal shutdown. The serial interface is an I²C communication interface. The I²C interface also allows for adjustability of VRs' voltage. Also, the power sequence is defined by strobes and delay times under I²C Control. The device is available in a 40-pin, 5x5 mm² thin QFN package for best thermal performance while optimizing the cost.

Simplified Application Circuit



Applications

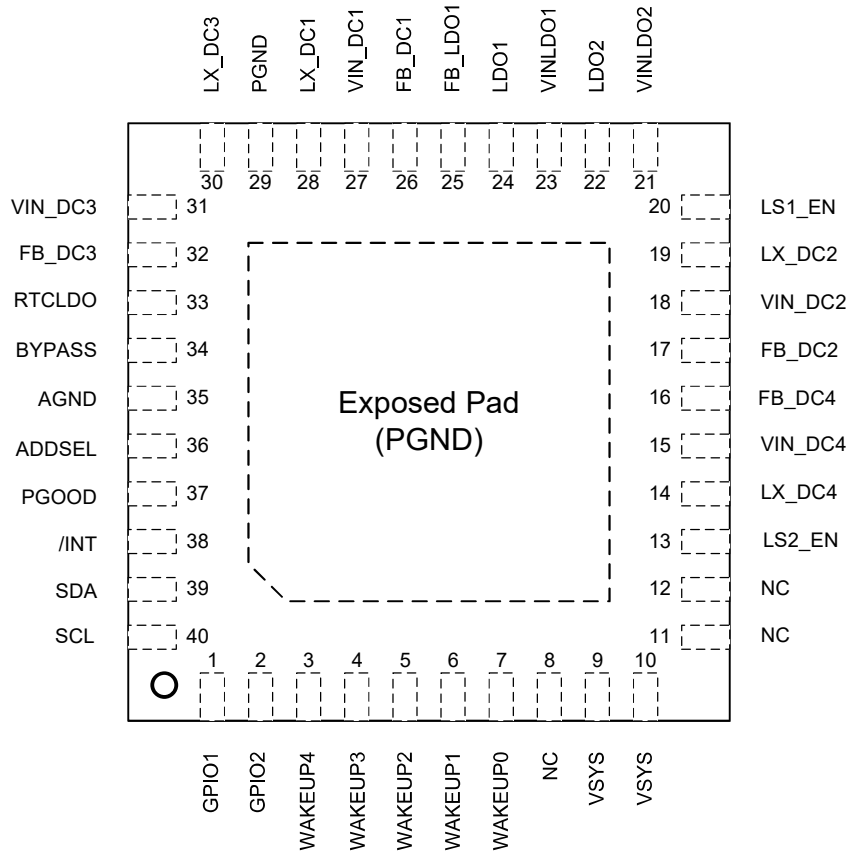
- **IP-Cam**
- **Drone**
- **Sport-Cam**
- **Car-Recorder**
- **Security**

Ordering and Marking Information

APW7704C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN5x5-40B Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW7704C QB : 7704C XXXXX	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VSYS}	VSYS to GND Voltage	-0.3 ~ 6.5	V
	VIN_DC1, VIN_DC2, VIN_DC3, VIN_DC4, VINLDO1, VINLDO2, LS1_EN, LS2_EN to GND Voltage	-0.3 ~ 6.5	V
	LX_DC1, LX_DC2, LX_DC3, LX_DC4 to GND Voltage	-0.3 ~ 6.5	V
	FB_DC1, FB_DC2, FB_DC3, FB_DC4, RTCLDO, LDO1, LDO2, FB_LDO1 to GND Voltage	-0.3 ~ 6.5	V
	All other pins to GND Voltage	-0.3 ~ 6.5	V
	PGND to AGND	-0.3 ~ 0.3	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	30	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5x5-40B is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VSYS}	Input Voltage	3.9 ~ 5.5	V
V_{DC1}	Buck1 Output Voltage	0.6 ~ 1.5	V
I_{DC1}	Buck1Output Current	~ 2.5	A
V_{DC2}	Buck2 Output Voltage	0.6 ~ 3.3	V
I_{DC2}	Buck2 Output Current	~ 1.5	A
V_{DC3}	Buck3 Output Voltage	0.6 ~ 3.3	V
I_{DC3}	Buck3 Output Current	~ 1	A
V_{DC4}	Buck4 Output Voltage	0.6 ~ 3.3	V
I_{DC4}	Buck4 Output Current	~ 2	A
V_{RTCLDO}	RTCLDO Output Voltage	1.5 ~ 3.05	V
I_{RTCLDO}	RTCLDO Output Current	~ 10	mA
V_{LDO1}	LDO1 Output Voltage	0.6 ~ 3.3	V
I_{LDO1}	LDO1 Output Current	~ 150	mA
V_{LDO2}	LDO2 Output Voltage	1.5 ~ 3.05	V
I_{LDO2}	LDO2 Output Current	~ 300	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VSYS}=5V and T_A=25°C.

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
QUIESCENT CURRENTS						
I_{SYS}	Input Supply Current (VSYS)	RTCLDO enabled, All other rails disable. No Load, T_A=25°C	-	50	-	μA
INPUT POWER						
	VSYS UVLO Voltage Threshold	VSYS Rising	2.9	3.0	3.1	V
	VSYS UVLO Voltage Threshold	VSYS Falling	2.7	2.8	2.9	V
	VSYS UVLO Voltage Hysteresis		-	0.2	-	V
THERMAL SHUTDOWN						
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing	-	160	-	°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis		-	30	-	°C
I/O PIN CHARACTERISTICS (SDA, SCL, /INT, ADDSEL, WAKEUP0/1/2/3/4, PGOOD)						
V_{IL}	Input Low Voltage	Include SDA, SCL, /INT, WAKEUP0/1/2/3/4 Input Pins	-	-	0.4	V
V_{IH}	Input High Voltage	Include SDA, SCL, /INT, WAKEUP0/1/2/3/4 Input Pins	1.5	-	-	V
V_{O_LOW}	Output Low Saturation Voltage	Sink current=5mA Include PGOOD, /INT Pins	-	-	0.4	V
I_{BIAS_IO}	High Level Leakage Current	Pull up to 5V, Include SDA, SCL, Input Pins	-	-	1	μA
		Pull up to 5V, Include WAKEUP0/1/2/3/4 Pins	-	50	-	μA
		Pull up to 5V, Include PGOOD and /INT Input Pins	-	-	0.2	μA
T_{INT_L}	/INT Pulled Low Time	/INT Pulled Low Time When Fault Event still Exists. The Period is 1ms	-	10	-	μs
f_{SCL}	SCL Clock Frequency		-	-	400	kHz
PGOOD DEFINITION (Relative with all DC/DC Converters, Load Switch and LDOs)						
	PGOOD Delay Time	Default, All VRs are Regulated	-	12.8	-	ms
	WAKEUP0 Hard Reset Detect Time	RSTTMR_EN=1	-	16	-	sec
	VSYS POR OKAY to Wakupx Enable Delay Time		-	150	-	μs
	Wakeupx Triggered to VR Starts to Rise Up Delay Time	VSYS=5V, Wakeupx Has Enabled to Strobe1 Starts to Rise Up Period	-	2.5	-	ms
	WAKEUP0/1/2/3/4 Deglitch Time		500	-	-	μs

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC1=5V and T_A=25°C.

- **BUCK1**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
$I_{Q\_NSW\_DC1}$	Consumption Current (No Switching Current)	VIN_DC1=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC1}$	Switching Current	VIN_DC1=5V, In Switching	-	5	-	mA
I_{SHUN_DC1}	Shutdown IQ	VIN_DC1=5V, In Shutdown	-	-	1	μA
V_{REF_DC1}	FB_DC1 Voltage	Selectable In I^2C	0.555	-	0.66	V
		Feedback Voltage Step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC1}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC1}=1.1V, I_{OUT_DC1}=0.75A ~ 2.5A	-	0.3	-	%/A
		V_{OUT_DC1}=1.1V, I_{OUT_DC1}=0.1A ~ 2.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC1=2.7V to 5.5V, V_{OUT_DC1}=1.1V, I_{OUT_DC1}=2.5A	-	0.4	-	%/V
I_{CL_DC1}	Current Limit		3.6	4	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC1}	Switching Frequency	I_{OUT_DC1}=0A, Force PWM	1350	1500	1650	kHz
		I_{OUT_DC1}=2.5A	1275	1500	1725	kHz
D_{MAX_DC1}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC1}$	Minimum On Time		-	60	-	ns
T_{SS_DC1}	Soft Start	V_{OUT_DC1}=1.1V, 0 to 95% of V_{OUT_DC1}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC1}$	High Side Ron	I_{OUT_DC1}=100mA	-	100	-	mΩ
$R_{DS(ON)\_L\_DC1}$	Low Side Ron	I_{OUT_DC1}=100mA	-	35	-	mΩ
R_{DIS_DC1}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	Persentage of Regulation Voltage	60	70	80	%
	Output Voltage OVP	Persentage of Regulation Voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC2=5V and T_A=25°C.

- **BUCK2**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
$I_{Q\_NSW\_DC2}$	Consumption Current (No Switching Current)	VIN_DC2=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC2}$	Switching Current	VIN_DC2=5V, In Switching	-	5	-	mA
I_{SHUN_DC2}	Shutdown IQ	VIN_DC2=5V, In Shutdown	-	-	1	μA
V_{REF_DC2}	FB_DC2 Voltage	Selectable In I^2C	0.555	-	0.66	V
		Feedback Voltage Step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC2}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC2}=0.6V, I_{OUT_DC2}=0.5A ~ 1.5A	-	0.3	-	%/A
		V_{OUT_DC2}=0.6V, I_{OUT_DC2}=0.1A ~ 1.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC2=2.7V to 5.5V, V_{OUT_DC2}=0.6V, I_{OUT_DC2}=1.5A	-	0.4	-	%/V
I_{CL_DC2}	Current Limit		2.1	3	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC2}	Switching Frequency	I_{OUT_DC2}=0A, Force PWM	1350	1500	1650	kHz
		I_{OUT_DC2}=1.5A	1275	1500	1725	kHz
D_{MAX_DC2}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC2}$	Minimum On Time		-	60	-	ns
T_{SS_DC2}	Soft Start	V_{OUT_DC2}=0.6V, 0 to 95% of V_{OUT_DC2}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC2}$	High Side Ron	I_{OUT_DC2}=100mA	-	130	-	mΩ
$R_{DS(ON)\_L\_DC2}$	Low Side Ron	I_{OUT_DC2}=100mA	-	65	-	mΩ
R_{DIS_DC2}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	Persentage of Regulation Voltage	60	70	80	%
	Output Voltage OVP	Persentage of Regulation Voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC3=5V and T_A=25°C.

- **BUCK3**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
$I_{Q\_NSW\_DC3}$	Consumption Current (No Switching Current)	VIN_DC3=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC3}$	Switching Current	VIN_DC3=5V, In Switching	-	5	-	mA
I_{SHUN_DC3}	Shutdown IQ	VIN_DC3=5V, In Shutdown	-	-	1	μA
V_{REF_DC3}	FB_DC3 Voltage	Selectable In I^2C	0.555	-	0.66	V
		Feedback Voltage Step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC3}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC3}=1.8V, I_{OUT_DC3}=0.25A ~ 1A	-	0.3	-	%/A
		V_{OUT_DC3}=1.8V, I_{OUT_DC3}=10mA ~ 1A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC3=2.7V to 5.5V, V_{OUT_DC3}=1.8V, I_{OUT_DC3}=1A	-	0.4	-	%/V
I_{CL_DC3}	Current Limit		1.6	2	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC3}	Switching Frequency	I_{OUT_DC3}=0A, Force PWM	1350	1500	1650	kHz
		I_{OUT_DC3}=1A	1275	1500	1725	kHz
D_{MAX_DC3}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC3}$	Minimum On Time		-	60	-	ns
T_{SS_DC3}	Soft Start	V_{OUT_DC3}=1.8V, 0 to 95% of V_{OUT_DC3}, No Load	-	750	-	μs
$R_{DS(ON)\_H\_DC3}$	High Side Ron	I_{OUT_DC3}=100mA	-	210	-	mΩ
$R_{DS(ON)\_L\_DC3}$	Low Side Ron	I_{OUT_DC3}=100mA	-	105	-	mΩ
R_{DIS_DC3}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	Persentage of Regulation Voltage	60	70	80	%
	Output Voltage OVP	Persentage of Regulation Voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC4=5V and T_A=25°C.

- **BUCK4**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
$I_{Q\_NSW\_DC4}$	Consumption Current (No Switching Current)	VIN_DC4=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC4}$	Switching Current	VIN_DC4=5V, In Switching	-	5	-	mA
I_{SHUN_DC4}	Shutdown IQ	VIN_DC4=5V, In Shutdown	-	-	1	μA
V_{REF_DC4}	FB_DC4 Voltage	Selectable In I^2C	0.555	-	0.66	V
		Feedback Voltage Step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC4}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC4}=3.3V, I_{OUT_DC4}=0.65A ~ 2A	-	0.3	-	%/A
		V_{OUT_DC4}=3.3V, I_{OUT_DC4}=0.1A ~ 2A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC4=4V to 5.5V, V_{OUT_DC4}=3.3V, I_{OUT_DC4}=2A	-	0.4	-	%/V
I_{CL_DC4}	Current Limit		3.6	4	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC4}	Switching Frequency	I_{OUT_DC4}=0A, Force PWM	1350	1500	1650	kHz
		I_{OUT_DC4}=2A	1275	1500	1725	kHz
D_{MAX_DC4}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC4}$	Minimum On Time		-	60	-	ns
T_{SS_DC4}	Soft Start	V_{OUT_DC4}=3.3V, 0 to 95% of V_{OUT_DC4}, No Load	-	750	-	μs
$R_{DS(ON)\_H\_DC4}$	High Side Ron	I_{OUT_DC4}=100mA	-	130	-	mΩ
$R_{DS(ON)\_L\_DC4}$	Low Side Ron	I_{OUT_DC4}=100mA	-	65	-	mΩ
R_{DIS_DC4}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	Persentage of Regulation Voltage	60	70	80	%
	Output Voltage OVP	Persentage of Regulation Voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{VSYS}=5V and T_A=25°C.

- **RTCLDO**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
	RTCLDO Output Voltage	Adjustable by I²C	1.5	-	3.05	V
I_{RTCLDO_Max}	RTCLDO Source Capability	V_{VIN_RTCLDO}=3.7V, V_{OUT_RTCLDO}=1.95V	-	-	10	mA
	DC Output Voltage Accuracy	I_{OUT_RTCLDO}=10mA, V_{VIN_RTCLDO} > V_{OUT_RTCLDO}+650mV, V_{OUT_RTCLDO}=1.95V	-3	-	3	%
	Load Regulation	I_{OUT_RTCLDO}=0mA ~ 10mA, V_{VIN_RTCLDO}=3.7V, V_{OUT_RTCLDO}=1.95V	-3	-	3	%
	Line Regulation	V_{VIN_RTCLDO}=3.7V ~ 5V, I_{OUT_RTCLDO}=10mA, V_{OUT_RTCLDO}=1.95V	-3	-	3	%
$V_{DROPOUT\_RTC}$	VSYS - VOUT_RTCLDO Dropout Voltage	I_{OUT_RTCLDO}=10mA, V_{OUT_RTCLDO}=1.95V, T_A=25°C	-	450	650	mV
		T_J= -40 ~ 85°C	-	650	865	mV
I_{CL_RTC}	Short Circuit Current Limit	$V_{OUT\_RTCLOD1}$ Short to GND, V_{VIN_RTCLDO}=5V	-	150	-	mA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VINLDO1=5V and T_A=25°C.

- **LDO1**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
	LDO1 Output Voltage Range	Output Adjustable, V_{FB_LDO1}=0.6V	0.6	-	3.3	V
	DC Output Voltage Accuracy	I_{LDO1}=10mA, $V_{VINLDO1}$ > V_{LDO1}+30mV	-2	-	2	%
	Load Regulation	I_{LDO1}=0mA to 150mA, $V_{VINLDO1}$=1.8V, V_{LDO1}=0.8V	-1.5	-	1.5	%
	Line Regulation	$V_{VINLDO1}$=1.8V to 5V, I_{LDO1}=150mA, V_{LDO1}=0.8V	-1.5	-	1.5	%
	VINLDO1 POR Voltage Threshold	VINLDO1 Rising	0.9	1	1.1	V
	VINLDO1 POR Voltage Hysteresis	VINLDO1 Falling	-	0.2	-	V
$V_{DROPOUT\_LDO1}$	VINLDO1 - VLDO1 Dropout Voltage	I_{LDO1}=150mA, $V_{VINLDO1}$=1.8V, T_A=25°C	-	-	650	mV
I_{CL_LDO1}	Short Circuit Current Limit	V_{LDO1} Short to GND, $V_{VINLDO1}$=5V	180	300	-	mA
	Output Voltage UVP	Persentage of Regulation Voltage	40	50	60	%
T_{SS_LDO1}	Soft Start Time	Time to Ramp V_{LDO1} from 5% to 95%, No Load	-	150	-	μs
R_{DIS_LDO1}	Discharge Resistor	Internal Discharge Resistor when Shutdown Occur	100	375	500	Ω
	PSRR	Frequency=1kHz, $V_{VINLDO1}$=1.8V, V_{LDO1}=0.8V, Loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VINLDO2=5V and T_A=25°C.

- **LDO2**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
	LDO2 Output Voltage Range	Output Adjustable by I^2C	1.5	-	3.05	V
	DC Output Voltage Accuracy	I_{LDO2}=10mA, $V_{VINLDO2}$ > V_{LDO2}+20mV	-2	-	2	%
	Load Regulation	I_{LDO2}=0mA to 200mA, $V_{VINLDO2}$=3.3V, V_{LDO2}=1.5V	-1.5	-	1.5	%
	Line Regulation	$V_{VINLDO2}$=3.3V to 5.5V, I_{LDO2}=200mA, V_{LDO2}=1.5V	-1	-	1	%
$V_{DROPOUT\_LDO2}$	VINLDO2 - VLDO2 Dropout Voltage	I_{LDO2}=200mA, $V_{VINLDO2}$=3.3V, T_A=25°C	-	-	900	mV
I_{CL_LDO2}	Short Circuit Current Limit	V_{LOD2} Short to GND, $V_{VINLDO2}$=5V	350	450	-	mA
	Output Voltage UVP	Persentage of Regulation Voltage	40	50	60	%
T_{SS_LDO2}	Soft Start Time	Time to Ramp V_{LDO2} from 5% to 95%, V_{LDO2}=1.5V, No Load	-	125	-	μs
R_{DIS_LDO2}	Discharge Resistor	Internal Discharge Resistor when Shutdown Occur	100	375	500	Ω
	PSRR	Frequency=1kHz, $V_{VINLDO2}$=3.3V, V_{LDO2}=1.5V, Loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over T_A=25°C.
External Load Switch, use LS1/2_EN to be an enable trigger signal.

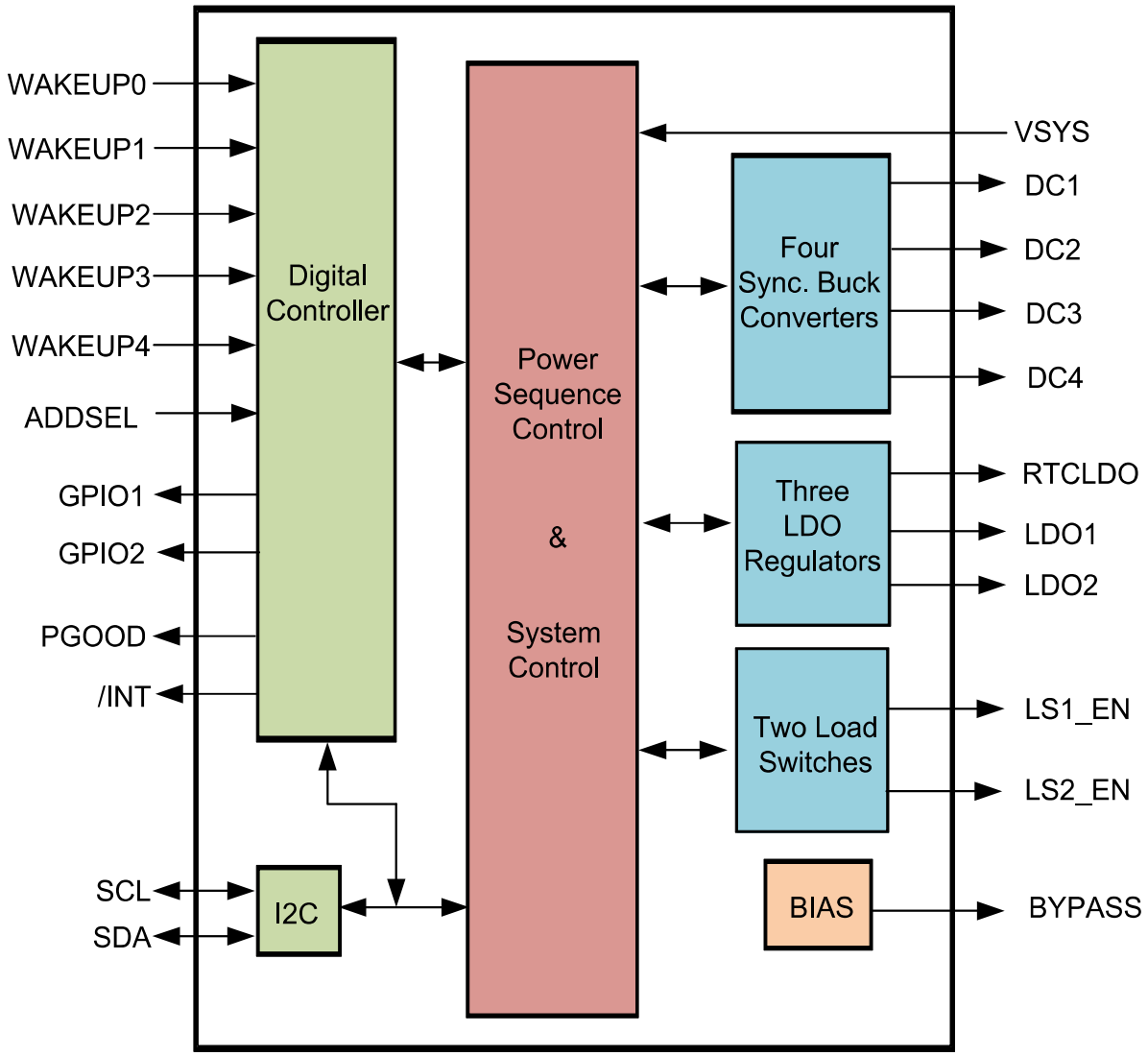
- **LS1/2**

Symbol	Parameter	Test Conditions	APW7704C			Unit
			Min.	Typ.	Max.	
V_{LDO_LS}	Internal LDO Voltage	Supply Source From V_{SYS}, No Load	2.5	3	3.5	V
V_{OH}	Output High Voltage	LS_ENx Voltage High Range, ILS_ENx=0mA, Supply Source is the Internal LDO Output V_{LDO_LS}	2.5	3	3.5	V
V_{OL}	Output Low Voltage	LS_ENx Voltage Low Range	-	0	-	V
	V_{LDO_LS} - V_{LS_ENx} Dropout Voltage	I_{LS_ENx}=5mA, V_{SYS}=3.6V, T_A=25°C	-	150	300	mV
		T_J= -40 ~125°C	-	225	400	mV
R_{LDO_LS}	VSYS to V_{LDO_LS} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Source}	V_{LDO_LS} to V_{LS_ENx} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Sink}	Output Sink Capability		-	6	-	Ω
	Short Circuit Current Limit	V_{LS_ENx} Short to GND, V_{SYS}=3.6V	-	30	-	mA
	LS_ENx Pin Pulled Low Resistor		-	10	-	kΩ

Pin Description

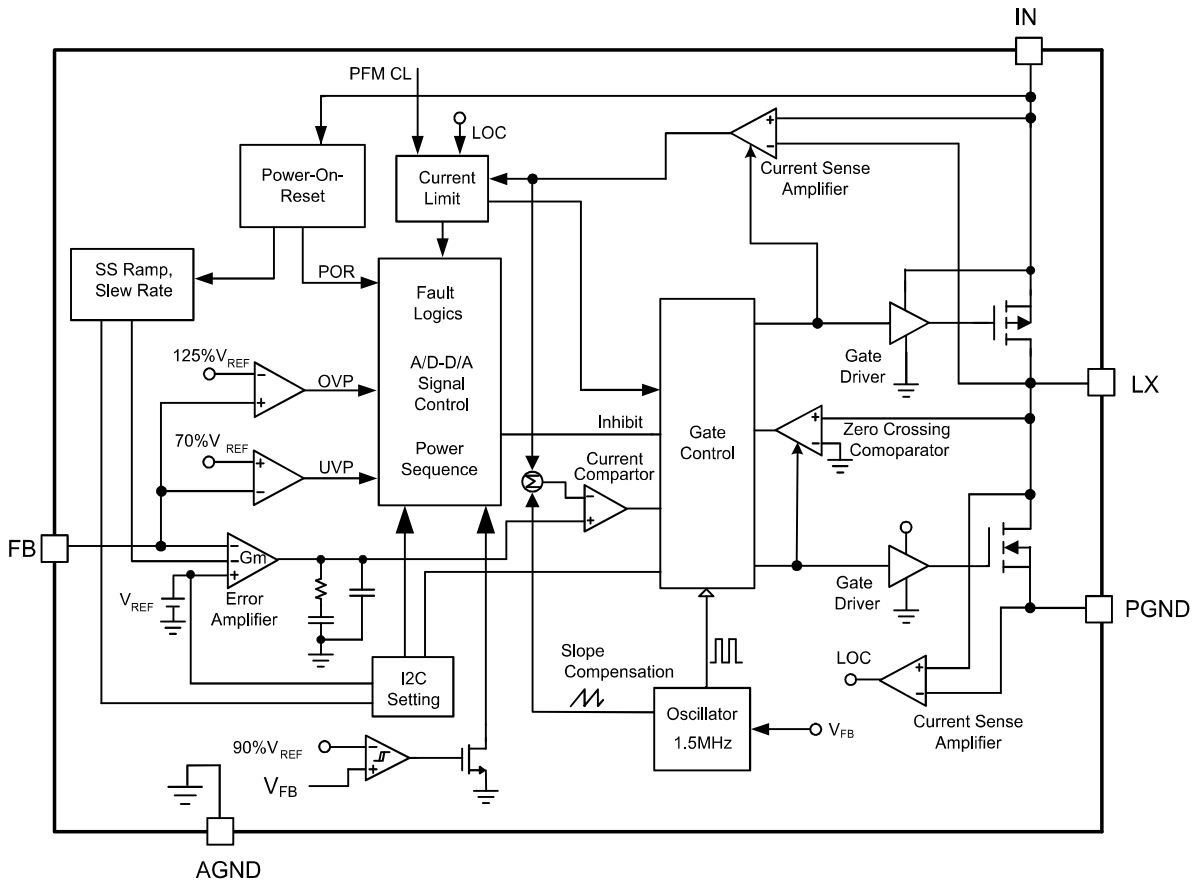
PIN		FUNCTION
NO.	NAME	
1	GPIO1	Indicated the PMIC VRs status and report to GPIO1 pin. Connect the GPIO1 to the pull up rail via 10kΩ resistor.
2	GPIO2	I^2C Select High-Low status and output to GPIO2 pin. Connect the GPIO2 to the pull up rail via 10kΩ resistor.
3	WAKEUP4	Input wake up pin to startup the PMIC with a power on event (pulse high).
4	WAKEUP3	Input wake up pin to startup the PMIC with a power on event (pulse high).
5	WAKEUP2	Input wake up pin to startup the PMIC with a power on event (pulse high).
6	WAKEUP1	Input wake up pin to startup the PMIC with a power on event (pulse high).
7	WAKEUP0	Push-Button input pin. When the pin signal is triggered from low to high, the device starts to power up.
8, 11, 12	NC	No Used.
9, 10	VSYS	System connection point.
13	LS2_EN	Load Switch 2 Output Enable Pin.
14	LX_DC4	DC4 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
15	VIN_DC4	DC4 PWM Converter Input Pin.
16	FB_DC4	DC4 Output Feedback Voltage Pin.
17	FB_DC2	DC2 Output Feedback Voltage Pin.
18	VIN_DC2	DC2 PWM Converter Input Pin.
19	LX_DC2	DC2 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
20	LS1_EN	Load Switch 1 Output Enable Pin.
21	VINLDO2	LDO2 Input Voltage Pin.
22	LDO2	LDO2 Output Voltage Pin.
23	VINLDO1	LDO1 Input Voltage Pin.
24	LDO1	LDO1 Output Voltage Pin.
25	FB_LDO1	LDO1 Output Feedback Voltage Pin. The LDO1 internal reference is 0.6V.
26	FB_DC1	DC1 Output Feedback Voltage Pin.
27	VIN_DC1	DC1 PWM Converter Input Pin.
28	LX_DC1	DC1 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
29	PGND	Power ground connection for high-current power converter node. Internally, PGND is connected to the anode of the low side diode. A single point connection is recommended between power PGND and the analog AGND near the IC PGND pin.
30	LX_DC3	DC3 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
31	VIN_DC3	DC3 PWM Converter Input Pin.
32	FB_DC3	DC3 Output Feedback Voltage Pin.
33	RTCLDO	RTCLDO Output Voltage Pin. The pin voltage is adjustable by I^2C.
34	BYPASS	Internal Bias Voltage. Connecting the BYPASS pin to the VSYS pin insures the IC operation. It is not recommended to connect any load to this pin.
35	AGND	IC Analog Ground.
36	ADDSEL	ADDSEL pin for I^2C slave address select, which an external resistor pull-high/low can select the slave address. If ADDSEL=L, the 7 bit slave ID is Hex 24h; if ADDSEL=H, the 7 bit slave ID is Hex 25h.
37	PGOOD	Power Good Indicator. Pulled low when either buck converter output is out of regulation.
38	/INT	Open Interrupt Output. Connect the /INT to the pull up rail via 10kΩ resistor. The /INT pin sends active low, 10us pulse to host to report charger device status and fault.
39	SDA	I^2C Interface Data.
40	SCL	I^2C Interface Clock.

Block Diagram



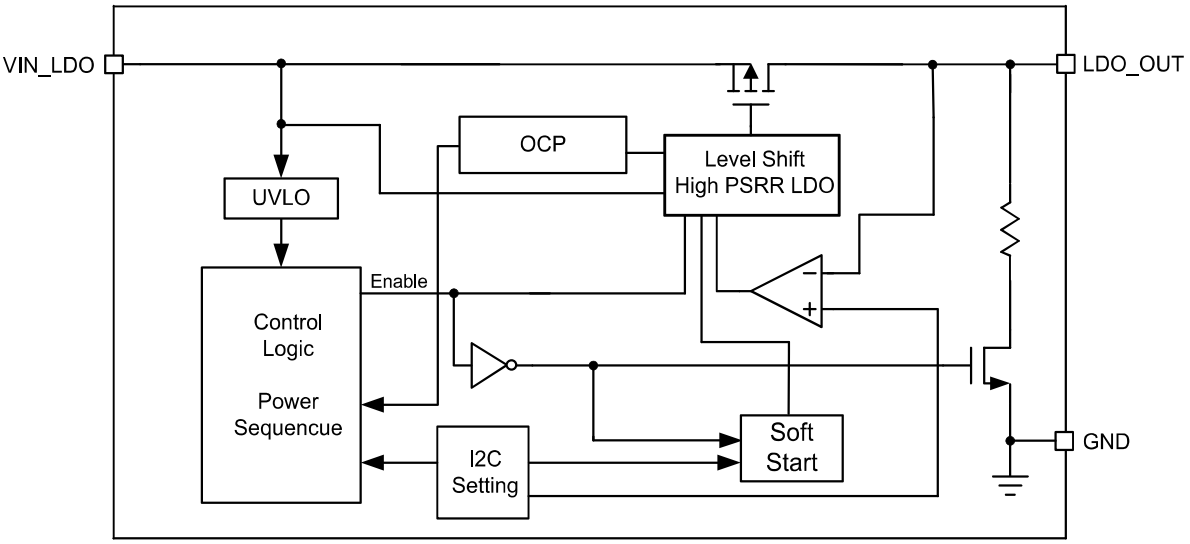
Block Diagram (Cont.)

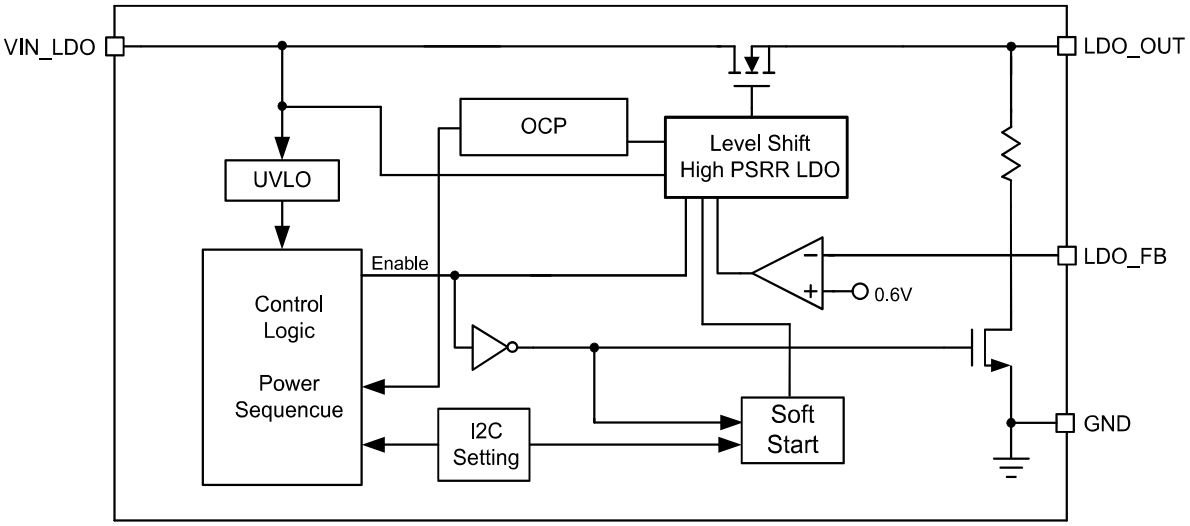
Buck Converter



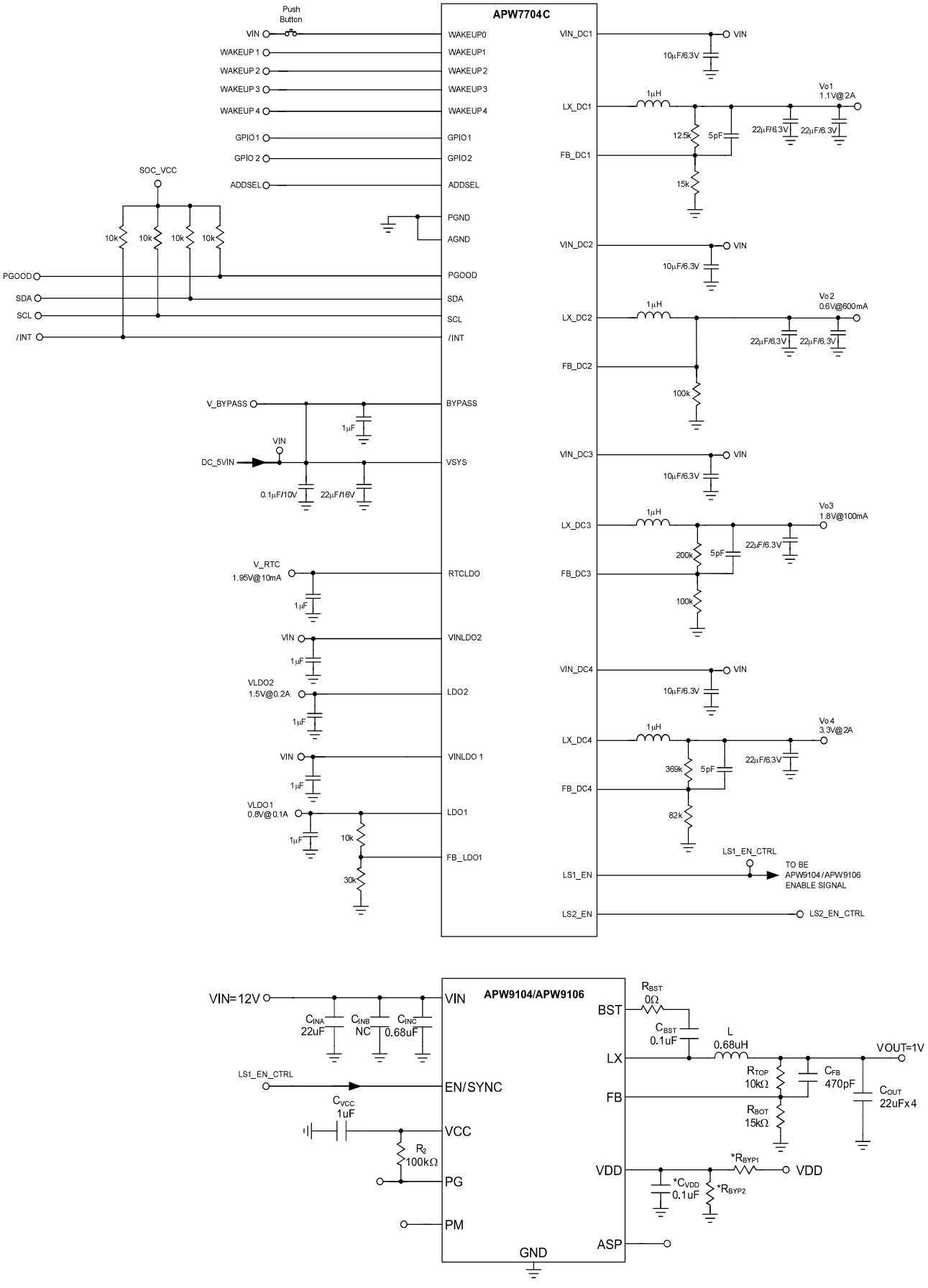
Block Diagram (Cont.)

LDO



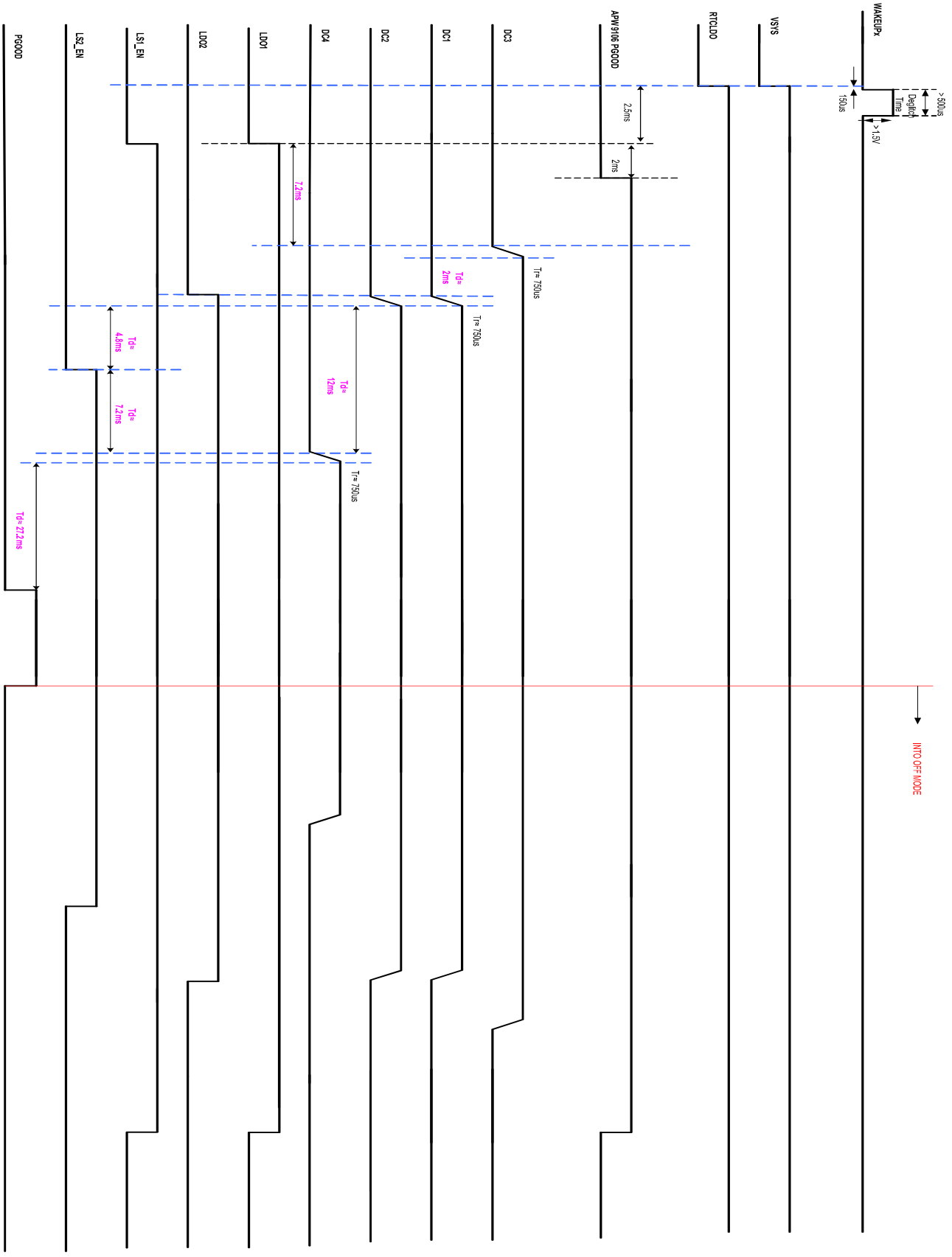


Typical Application Circuit



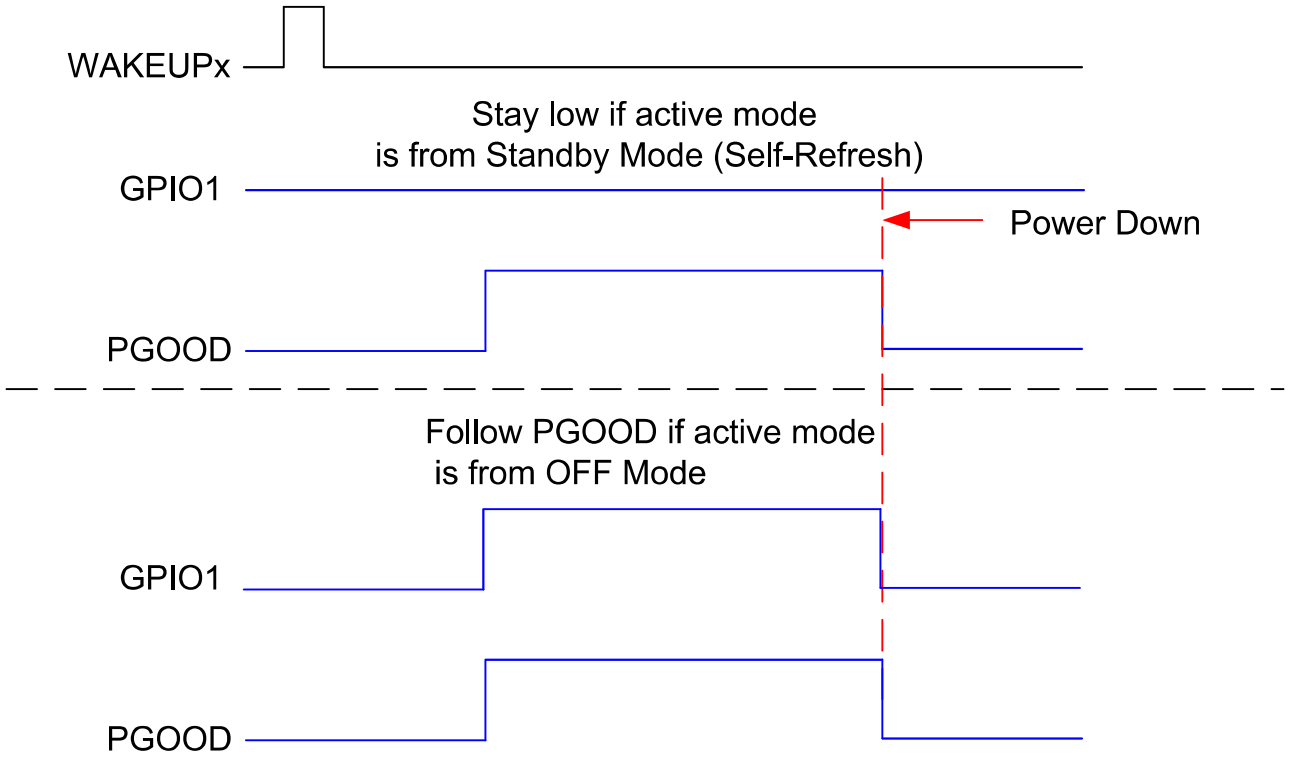
Power Sequence

- **DC_5V IN Supplied to VSYS Terminal**



GPIO Behavior

GPIO1 indicates APW7704C ACTIVE status comes from OFF or Self-Refresh mode (Has "OFF bit "write" setting. If OFF bit is written to 1 and one of VRs is still alive, the status is in “self-refresh” mode. If all of VRs are shutoff when OFF bit is written to 1, the status is in “OFF” mode). If ACTIVE status is from self-refresh mode, GPIO1 keeps in low; else if ACTIVE status is from OFF Mode, GPIO1 goes high with PGOOD timing.
GPIO2 output high-low status can be set from I^2C register. When the bit is written to “1”, GPIO2 keeps in high; else if the bit is written to “0”, GPIO2 keeps in low.



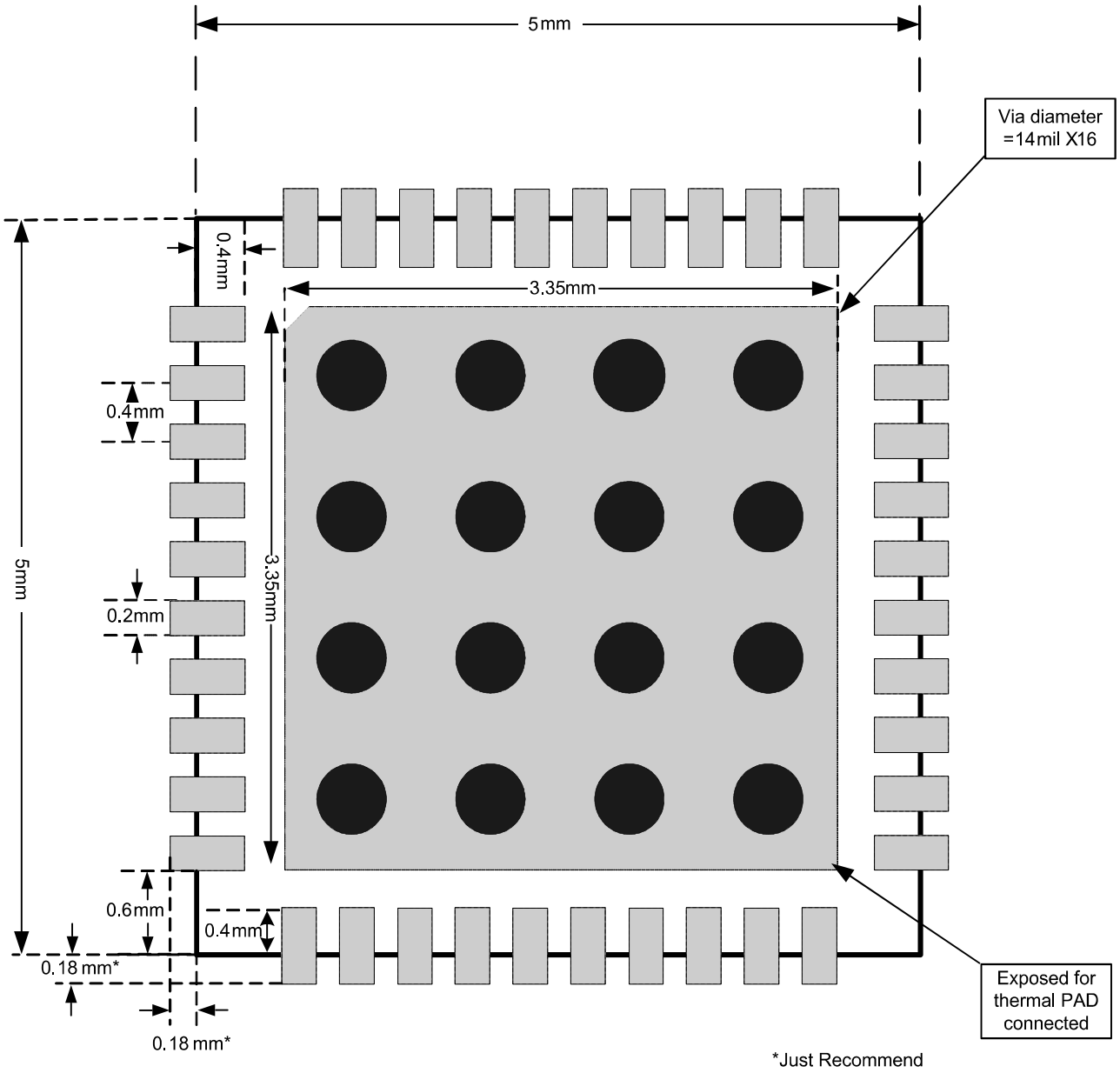
Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. Below are Layout consideration checklist and demoboard layout for your reference:

Signal Name	Pinouts Definition	Layout
Input Pins (VSYS, VIN_DC1, VIN_DC2, VIN_DC3, VIN_DC4, VINLDO1, VINLDO2)	Charger and All VR's Power Source Input Pins	Place the input capacitors on each power source input pins with low impedance to GND and low impedance to the each input pins. Noted that, because VSYS is the all VR's input power source, the VSYS terminal bulk capacitor is recommended to 22uF/16V and connects to VSYS terminal as close as possible.
LX Pins (LX_DC1, LX_DC2, LX_DC3, LX_DC4)	ALL VR's LX Pins	Keep the switching nodes away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes to inductors as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer. Ideally, route the LX pins to inductors on the top layer is recommended to avoid the switching nodes interference.
Feedback Pins (FB_DC1, FB_DC2, FB_DC3, FB_DC4, FB_LDO1)	ALL VR's Output Feedback Voltage Pin	The pins are high impedance and sensible to noise from the switch node. Coupling from fast switching signals must be avoided. For the better stability, the forward capacitor 5pF from output to feedback is recommended and the feedback divider resistance is recommended as the application circuit.
Bypass Pin	Internal Bias Voltage	Connect the decoupling capacitor to bypass pin as close as possible. The small control signals should be routed away from the high current paths.
Ground (Thermal Pad, PGND, AGND)	IC's Analog and Power Ground	Connect the IC's AGND and PGND pad to thermal pad directly. The thermal pad connects to other layer's ground plane through several vias.

Layout Consideration (Cont.)

Recommended Minimum Footprint



I²C Programming

I²C Serial Control Interface

The APW7704C DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status. The DAP supports the standard-mode I²C bus operation (100kHz maximum), the fast I²C bus operation (400kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the R/$\overline{W}$ bit a zero indicates a transmission (WRITE), a “one” indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7704C holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

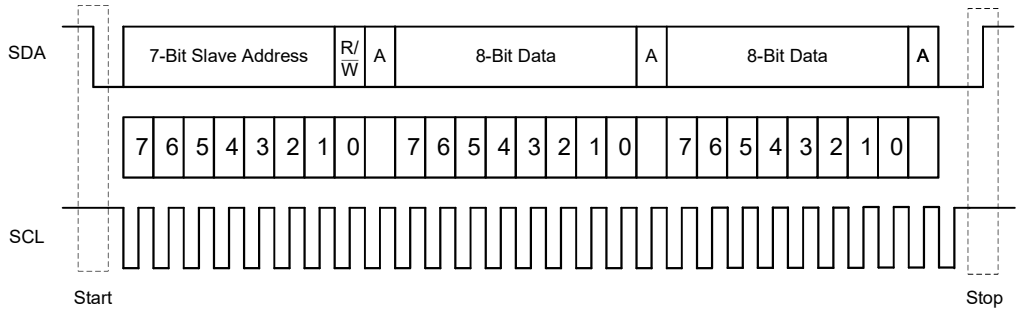


Figure 1. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. Pin ADDSEL defines the I²C device address. The device 7-bit address is defined as “0100100” (24H) for ADDSEL=LOW and “0100101” (25H) for ADDSEL=HIGH.

I²C Programming (Cont.)

Single-Byte Transfer

The serial control interface supports single-byte R/$\overline{W}$ operations for sub-addresses 0x00 to 0xFF.
Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7704C also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7704C. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 2., a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit determines the direction of the data transfer. For a write data transfer, the R/$\overline{W}$ bit will be a 0. After receiving the correct I²C device address and the R/$\overline{W}$ bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7704C internal memory address being accessed. After receiving the address byte, the APW7704C again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7704C again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

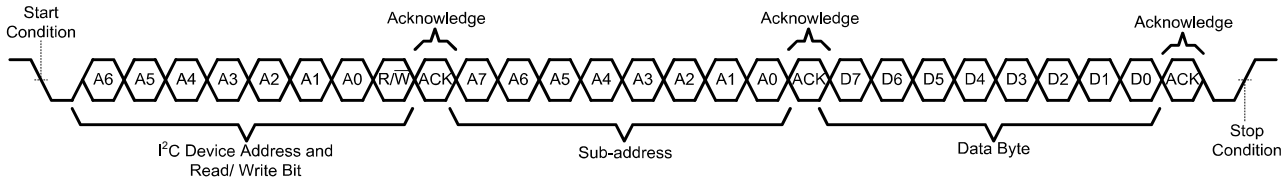


Figure 2. Single-Byte Write Transfer

I²C Programming (Cont.)

Single-Byte Read

As shown in Figure 3., a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/$\overline{W}$ bit becomes a 0. After receiving the APW7704C address and the R/$\overline{W}$ bit, APW7704C responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7704C address and the R/$\overline{W}$ bit again. This time the R/$\overline{W}$ bit becomes a 1, indicating a read transfer. After receiving the address and the R/$\overline{W}$ bit, the APW7704C again responds with an acknowledge bit. Next, the APW7704C transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

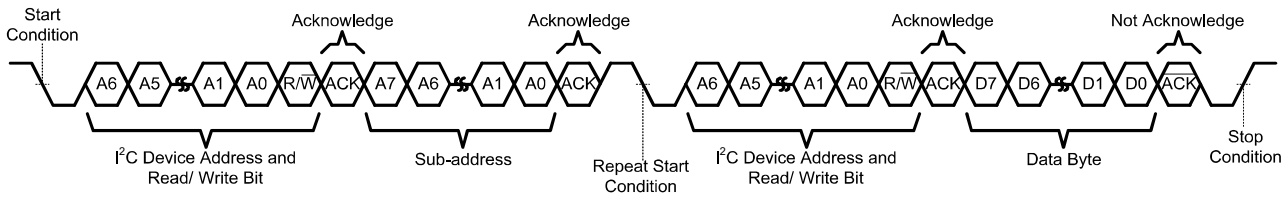


Figure 3. Single-Byte Read Transfer

I²C Programming (Cont.)

I²C Control Timing			Min.	Typ.	Max.	Unit
	SDA and SCL Leakage Current		-	0.01	1	μA
F_{I2C}	I²C Operating Frequency		-	-	100 400	kHz
T_{BUF}	I²C Free Time Between Stop and Start Condition	SCL=100kHz SCL=400kHz	4.7 1.3	- -	- -	μs
$T_{\_HD\_STA}$	Hold Time After Start Condition	After this period, the first clock is generated SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
$T_{\_SU\_STA}$	Repeated Start Condition Setup Time	SCL=100kHz SCL=400kHz	4.7 0.6	- -	- -	μs
$T_{\_SU\_STO}$	Stop Condition Setup Time	SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
$T_{\_HD\_DAT}$	Data Hold Time	SCL=100kHz SCL=400kHz	0 0	- -	- -	ns
$T_{\_SU\_DAT}$	Data Setup Time	SCL=100kHz SCL=400kHz	250 100	- -	- -	ns
$T_{\_LOW}$	Clock Low Period	SCL=100kHz SCL=400kHz	4.7 1.3	- -	- -	μs
$T_{\_HIGH}$	Clock High Period	SCL=100kHz SCL=400kHz	4 0.6	- -	- -	μs
T_F	Fall Time of I²C SDA	SCL=100kHz SCL=400kHz	0 0	- -	300 300	ns
T_F	Fall Time of I²C SCL	SCL=100kHz SCL=400kHz	0 0	- -	300 300	ns
T_R	Rise Time of I²C SDA	SCL=100kHz SCL=400kHz	- 20+0.1 C_b	- -	1000 300	ns
T_R	Rise Time of I²C SCL	SCL=100kHz SCL=400kHz	- 20+0.1 C_b	- -	300 300	ns
C_b	Capacitive Load for Each Bus Line	SCL=100kHz SCL=400kHz	- -	- -	400 400	pF

I²C Programming (Cont.)

Timing Diagram

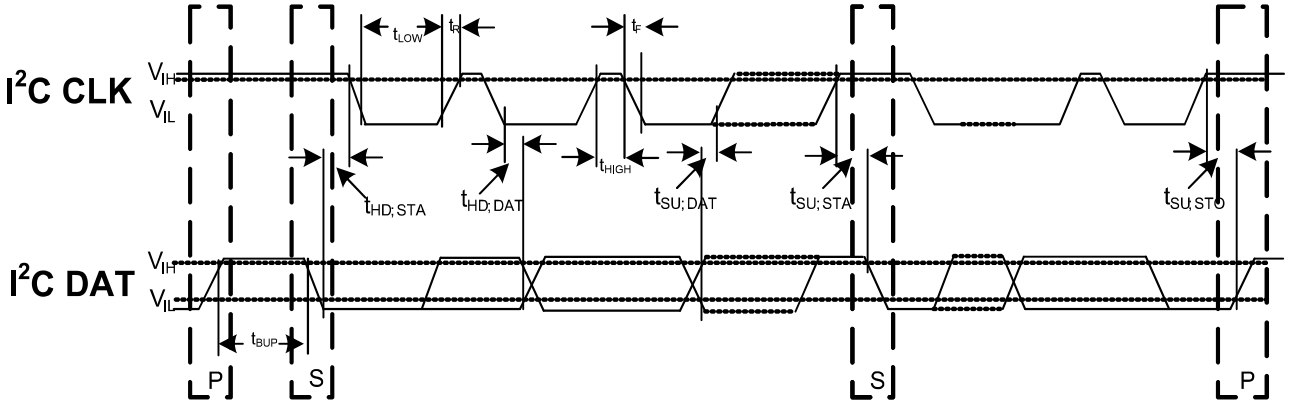


Figure 4: I²C Common AC Specification

I²C Programming (Cont.)

Register Map

Register Address	Register Name	Read/Write/Read Only State	Bits								Default Value
			D7	D6	D5	D4	D3	D2	D1	D0	
00	CONTROL0	Read/Write	0	0	0	1	1	0	1	1	1B
01	CONTROL1	Read/Write	0	1	0	1	0	1	0	0	54
02	CONTROL2	Read/Write	0	1	0	1	1	0	0	1	59
07	BUCKCONFIG0	Read/Write	0	0	1	1	0	0	1	1	33
08	BUCKCONFIG1	Read/Write	0	0	1	1	0	0	1	1	33
09	LDOCONFIG0	Read/Write	0	0	0	0	1	0	0	1	09
0A	LDOCONFIG1	Read/Write	0	0	0	0	0	0	0	0	00
0B	TIME LAPSE2	Read/Write	0	0	0	0	0	0	0	0	00
0C	TIME LAPSE1	Read/Write	0	0	0	0	0	0	0	0	00
0D	TIME LAPSE0	Read/Write	0	0	0	0	0	0	0	0	00
0E	SEQ0	Read/Write	0	0	1	1	0	0	1	1	33
0F	SEQ1	Read/Write	0	0	1	0	0	1	0	1	25
10	SEQ2	Read/Write	0	0	0	1	0	1	0	0	14
11	SEQ3	Read/Write	0	0	0	1	0	0	1	1	13
12	DLY0	Read/Write	0	0	0	0	1	1	1	1	0F
13	DLY1	Read/Write	0	0	1	0	1	0	0	1	29
14	DLY2	Read/Write	1	1	1	1	1	1	1	1	FF
15	DLY3	Read/Write	1	1	1	1	1	1	1	1	FF
16	INT MASK	Read/Write	1	0	0	0	0	0	0	0	80
17	CHIPID	ReadOnly	0	1	1	0	0	x	x	x	6x
19	INT FLAG	Read Only	0	0	0	0	0	0	0	0	00
1A	WAKEUP	Read Only	0	0	0	0	0	0	0	0	00

I²C Programming (Cont.)

REG00

Bit	7	6	5	4	3	2	1	0
Name	WDT_RST	RESERVED	OFF	RSTTMR_EN	RESERVED			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	1	0	1	1

Name	Description
WDT_RST	Watchdog timer reset bit. Write “1” to reset the watchdog timer when WDT_EN bit is enabled. **0 – Read 0 as usual, write 1 no effect** 1 – Write 1 to reset the watchdog timer. (auto clear)
OFF	**0 – Normal status** 1 – Trigger a power-down sequence. Note: When set this bit to 1 to trigger a power-down sequence. Bit is automatically reset to 0. During power down sequence, if the STBYON bit set to “1”, the channel will still on.
RSTTMR_EN	Push-button (Wakeup0) reset function enable-disable bit. 0 – Disabled **1 – Enabled**
RESERVED	No Used.

I²C Programming (Cont.)

REG01

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	RESERVED	TL_EN	RSTTMR	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	0	1	0	1	0	0
Name	**Description**							
TL_EN	Time lapse function enabled bit. **0 – time lapse function disable** 1 – time lapse function enable							
RSTTMR	Push-button (Wakeup0) reset time constant. 0 – 8s **1 – 16s** NOTE: Device enters RESET if wakeup0 is held high pulse width for >8s or >16s (default), depending on RSTTMR bit.							
RESERVED	No Used.							

I²C Programming (Cont.)

REG02

Bit	7	6	5	4	3	2	1	0
Name	WDT_EN	WDTMR			RESERVED	RESERVED	RESERVED	GPIO2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	0	1	1	0	0	1

Name	Description
WDT_EN	Watchdog timer function enabled bit. **0 – watchdog timer function disable** 1 – watchdog timer function enable Note: When WDT_EN is enabled, write “1” to reset WDT_RST bit to reset watchdog timer, if watchdog timer is timeout, the PMIC will reset all registers and auto reboot.
WDTMR	Watchdog timer setting bit. 000 – 1s 001 – 2s 010 – 4s 011 – 8s 110 – 16s **101 – 32s** 110 – 64s 111 – 128s
GPIO2	GPIO2 status bit; This bit determines the output signal of GPIO2 pin. 0 – GPIO2 pin is output low **1 – GPIO2 pin is output high**
RESERVED	No Used.

I²C Programming (Cont.)

REG07

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC1	VFB_DC1			STBYON_DC2	VFB_DC2		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1
Name	**Description**							
STBYON_DC1	Off mode DC1 regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
VFB_DC1	VFB_DC1 voltage setting. 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							
STBYON_DC2	Off mode DC2 regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
VFB_DC2	VFB_DC2 voltage setting. 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							

I²C Programming (Cont.)

REG08

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC3	VFB_DC3			STBYON_DC4	VFB_DC4		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1
Name	**Description**							
STBYON_DC3	Off mode DC3 regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
VFB_DC3	VFB_DC3 voltage setting. 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							
STBYON_DC4	Off mode DC4 regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
VFB_DC4	VFB_DC4 voltage setting. 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V							

I²C Programming (Cont.)

REG09

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	RTCLDO				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	1	0	0	1
Name	Description							
RTCLDO	RTCLDO output voltage setting. 00000 – 1.5V 00001 – 1.55V 00010 – 1.6V 00011 – 1.65V 00100 – 1.7V 00101 – 1.75V 00110 – 1.8V 00111 – 1.85V 01000 – 1.9V **01001 – 1.95V** 01010 – 2.0V 01011 – 2.05V 01100 – 2.1V 01101 – 2.15V 01110 – 2.2V 01111 – 2.25V 10000 – 2.3V 10001 – 2.35V 10010 – 2.4V 10011 – 2.45V 10100 – 2.5V 10101 – 2.55V 10110 – 2.6V 10111 – 2.65V 11000 – 2.7V 11001 – 2.75V 11010 – 2.8V 11011 – 2.85V 11100 – 2.9V 11101 – 2.95V 11110 – 3.0V 11111 – 3.05V							
RESERVED	No Used.							

REG0A

Bit	7	6	5	4	3	2	1	0
Name	STBYON_LDO1	STBYON_LDO2	RESERVED	LDO2				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
STBY_ON_LDO1	Standby mode regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
STBY_ON_LDO2	Standby mode regulator enabled bit. **0 – power off as sequence** 1 – still enable in OFF mode							
LDO2	LDO2 output voltage setting. **0 0000 – 1.50V** 0 0001 – 1.55V 0 0010 – 1.60V 0 0011 – 1.65V 0 0100 – 1.70V 0 0101 – 1.75V 0 0110 – 1.80V 0 0111 – 1.85V 0 1000 – 1.90V 0 1001 – 1.95V 0 1010 – 2.00V 0 1011 – 2.05V 0 1100 – 2.10V 0 1101 – 2.15V 0 1110 – 2.20V 0 1111 – 2.25V 1 0000 – 2.30V 1 0001 – 2.35V 1 0010 – 2.40V 1 0011 – 2.45V 1 0100 – 2.50V 1 0101 – 2.55V 1 0110 – 2.60V 1 0111 – 2.65V 1 1000 – 2.70V 1 1001 – 2.75V 1 1010 – 2.80V 1 1011 – 2.85V 1 1100 – 2.90V 1 1101 – 2.95V 1 1110 – 3.00V 1 1111 – 3.05V							
RESERVED	No Used.							

I²C Programming (Cont.)

REG0B

Bit	7	6	5	4	3	2	1	0
Name	T23	T22	T21	T20	T19	T18	T17	T16
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second. **00000000 00000000 00000000 - 1sec** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

REG0C

Bit	7	6	5	4	3	2	1	0
Name	T15	T14	T13	T12	T11	T10	T09	T08
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second. **00000000 00000000 00000000 - 1sec** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

REG0D

Bit	7	6	5	4	3	2	1	0
Name	T07	T06	T05	T04	T03	T02	T01	T00
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0
Name	Description							
T23~T0	Time lapse length setting in second. **00000000 00000000 00000000 - 1sec** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

I²C Programming (Cont.)

REG0E

Bit	7	6	5	4	3	2	1	0
Name	DC1_SEQ				DC2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1

Name	Description
DC1_SEQ	DC1 enable STROBE. 0000 – No Used 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC2_SEQ	DC2 enable STROBE. 0000 – No Used 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG0F

Bit	7	6	5	4	3	2	1	0
Name	DC3_SEQ				DC4_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	0	0	1	0	1

Name	Description
DC3_SEQ	DC3 enable STROBE. 0000 – No Used 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC4_SEQ	DC4 enable STROBE. 0000 – No Used 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 **0101 – enable at STROBE5** 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG10

Bit	7	6	5	4	3	2	1	0
Name	LS1_EN_SEQ				LS2_EN_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	1	0	0
Name	Description							
LS1_EN_SEQ	LS1_EN enable STROBE. 0000 – No Used **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
LS2_EN_SEQ	LS2_EN enable STROBE. 0000 – No Used 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 **0100 – enable at STROBE4** 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

I²C Programming (Cont.)

REG11

Bit	7	6	5	4	3	2	1	0
Name	LDO1_SEQ				LDO2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	1	1
Name	Description							
LDO1_SEQ	LDO1 enable STROBE. 0000 – No Used **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							
LDO2_SEQ	LDO2 enable STROBE. 0000 – No Used 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7							

I²C Programming (Cont.)

REG12

Bit	7	6	5	4	3	2	1	0
Name	RESERVED				DLY2			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	1	1	1	1
Name	Description							
RESERVED	No Used.							
DLY2	Delay 2 time (Between STROBE1 and STROBLE2) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms 1001 – 4.8ms 1101 – 6.4ms 0010 – 2ms 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms **1111 – 7.2ms**							

REG13

Bit	7	6	5	4	3	2	1	0
Name	DLY3				DLY4			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	0	1	0	0	1
Name	Description							
DLY3	Delay 3 time (Between STROBE2 and STROBLE3) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms 1001 – 4.8ms 1101 – 6.4ms **0010 – 2ms** 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms 1111 – 7.2ms							
DLY4	Delay 4 time (Between STROBE3 and STROBLE4) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms **1001 – 4.8ms** 1101 – 6.4ms 0010 – 2ms 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms 1111 – 7.2ms							

I²C Programming (Cont.)

REG14

Bit	7	6	5	4	3	2	1	0
Name	DLY5				DLY6			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	1	1	1	1	1	1
Name	Description							
DLY5	Delay 5 time (Between STROBE4 and STROBLE5) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms 1001 – 4.8ms 1101 – 6.4ms 0010 – 2ms 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms **1111 – 7.2ms**							
DLY6	Delay 6 time (Between STROBE5 and STROBLE6) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms 1001 – 4.8ms 1101 – 6.4ms 0010 – 2ms 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms **1111 – 7.2ms**							

REG15

Bit	7	6	5	4	3	2	1	0
Name	DLY7				PGDLY			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	1	1	1	1	1	1
Name	Description							
DLY7	Delay 7 time (Between STROBE6 and STROBLE7) 0000 – 1.2ms 0100 – 2.8ms 1000 – 4.4ms 1100 – 6ms 0001 – 1.6ms 0101 – 3.2ms 1001 – 4.8ms 1101 – 6.4ms 0010 – 2ms 0110 – 3.6ms 1010 – 5.2ms 1110 – 6.8ms 0011 – 2.4ms 0111 – 4ms 1011 – 5.6ms **1111 – 7.2ms**							
PGDLY	Power Good Delay time. 0000 – 1ms 0100 – 4ms 1000 – 7.2ms 1100 – 10.4ms 0001 – 1.6ms 0101 – 4.8ms 1001 – 8ms 1101 – 11.2ms 0010 – 2.4ms 0110 – 5.6ms 1010 – 8.8ms 1110 – 12ms 0011 – 3.2ms 0111 – 6.4ms 1011 – 9.6ms **1111 – 12.8ms** Note PGDLY applies to PGOOD pin.							

I²C Programming (Cont.)

REG16

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	WKUPxM	RESERVED	TEMPM	RESERVED	RESERVED	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	0	0	0	0	0	0
Name	**Description**							
WKUPxM	Wakeupx status change interrupt mask. **0 – interrupt is issued when wakeupx status changes (WAKEUPx changed low to high)** 1 – no interrupt is issued when wakeupx status changes							
TEMPM	Chip temperature alarm status change interrupt mask. **0 – interrupt is issued when chip temperature is over 130°C** 1 – no interrupt is issued when chip temperature is over 130°C							
RESERVED	No Used.							

I²C Programming (Cont.)

REG17

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	CHIPID			RESERVED	REV		
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	1	1	0	0	x	x	x

Name	Description
CHIP ID	Chip ID.
REV	Revision. 000 – revision 1.0 001 – revision 1.1 010 – revision 1.2 011 – revision 1.3 … 111 – Future Use
RESERVED	No Used.

I²C Programming (Cont.)

REG19

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	WKUPxI	RESERVED	TEMPI	RESERVED	
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Name	Description
WKUPxI	Wakeupx status changed flag. **0 – no change in status** 1 – wakeupx status change (WAKEUPx changed low to high) NOTE: Detail information is available in 0x1A register
TEMPI	Chip temperature alarm status changed flag. **0 – no change in status** 1 – Chip temperature is over 130°C
RESERVED	No Used.

I²C Programming (Cont.)

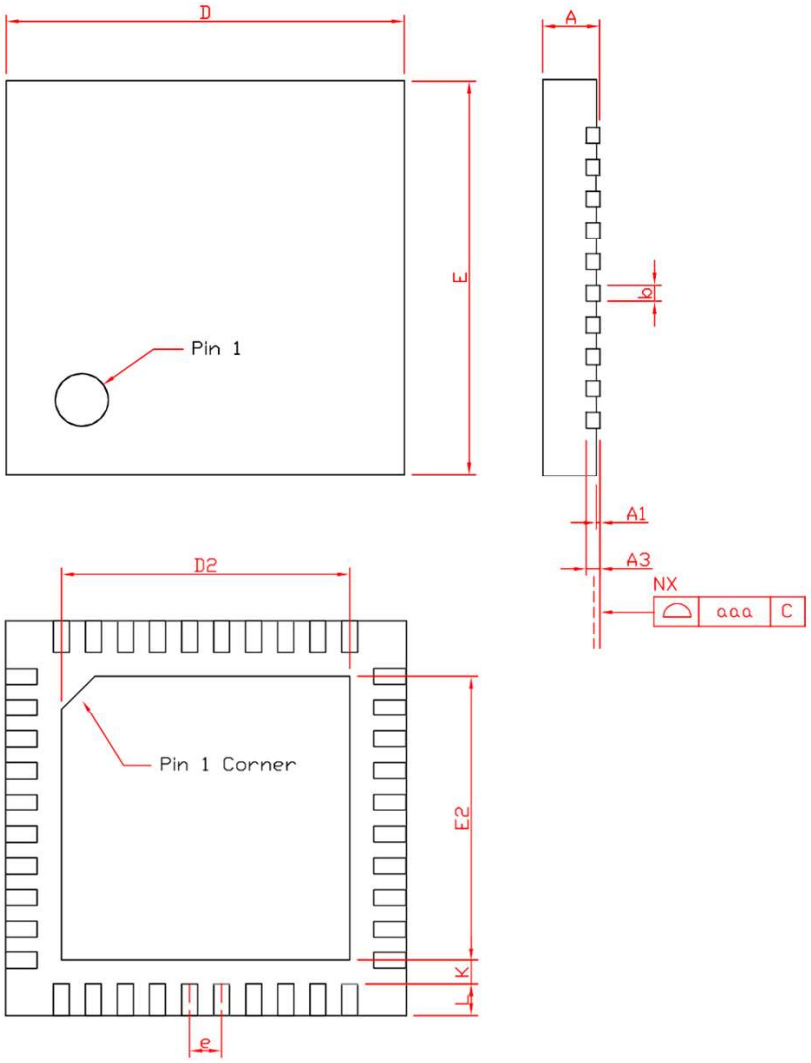
REG1A

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	WKUP0	WKUP1	WKUP2	WKUP3	WKUP4
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Name	Description
WKUP0	WAKEUP0 status changed bit. (Alto clear when readout) **0 – no change in WAKEUP0 status** 1 – WAKEUP0 status change
WKUP1	WAKEUP1 status changed bit. (Alto clear when readout) **0 – no change in WAKEUP1status** 1 – WAKEUP1 status change
WKUP2	WAKEUP2 status changed bit. (Alto clear when readout) **0 – no change in WAKEUP2 status** 1 – WAKEUP2 status change
WKUP3	WAKEUP3 status changed bit. (Alto clear when readout) **0 – no change in WAKEUP3status** 1 – WAKEUP3 status change
WKUP4	WAKEUP4 status changed bit. (Alto clear when readout) **0 – no change in WAKEUP4 status** 1 – WAKEUP4 status change
RESERVED	No Used.

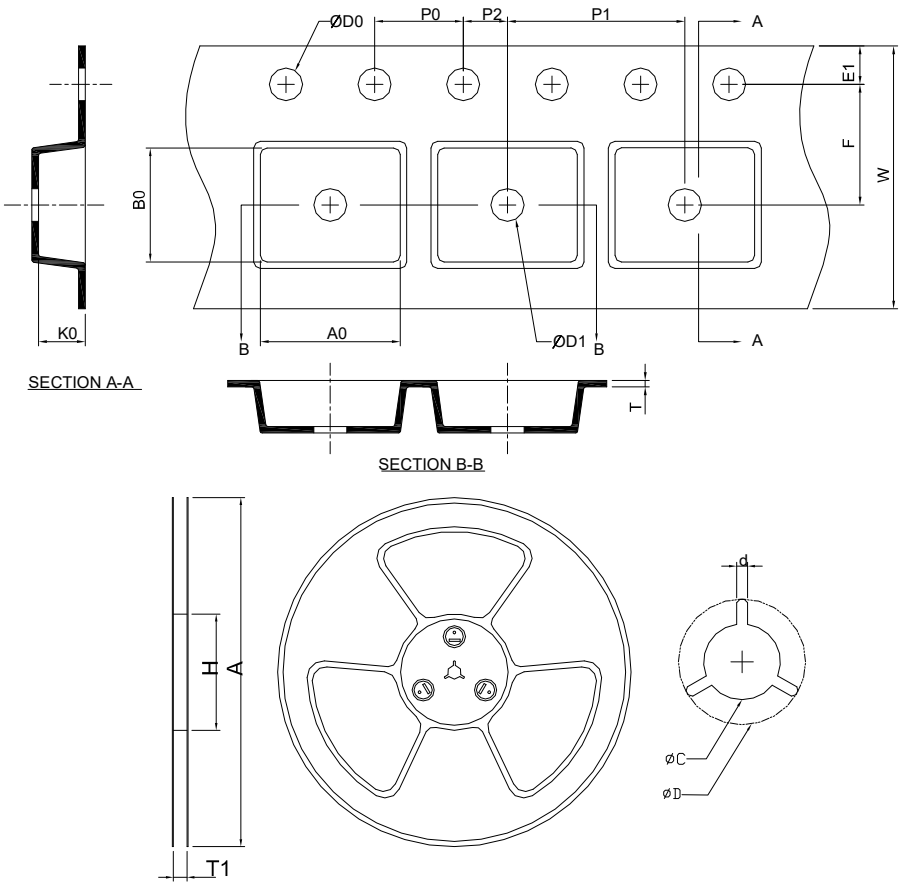
Package Information

TQFN5x5-40B



SYMBOL	TQFN5*5-40B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.50	3.70	0.138	0.146
E	4.90	5.10	0.193	0.201
E2	3.50	3.70	0.138	0.146
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

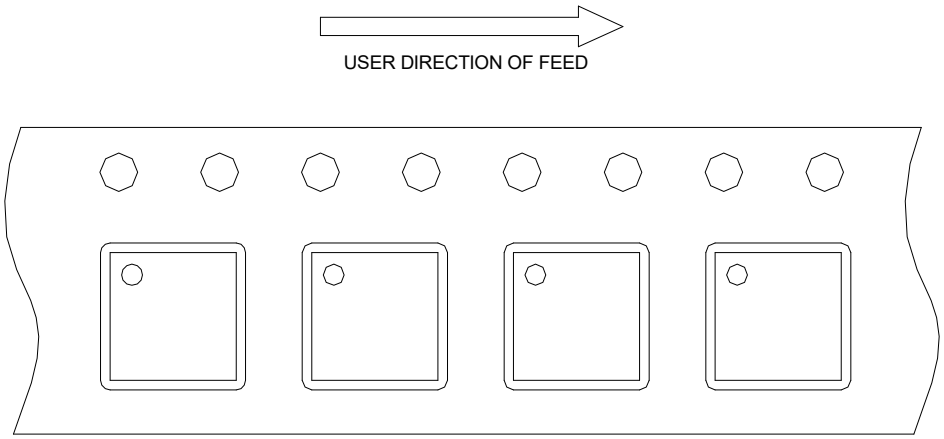
(mm)

Devices Per Unit

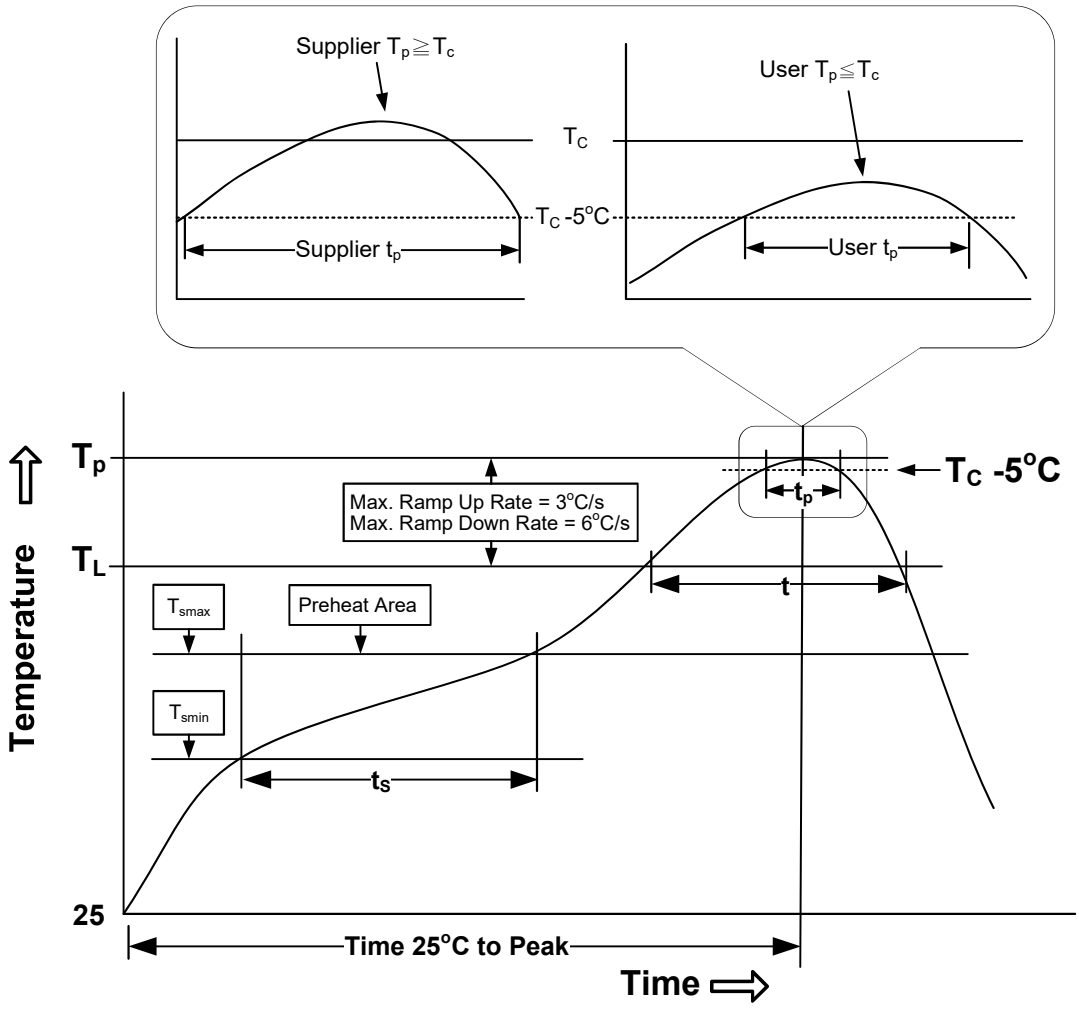
Package Type	Packing	Quantity
TQFN 5x5	Tape & Reel	2500

Taping Direction Information

TQFN5x5-40B



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test Item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD-78	10ms, 1_{tr} ≧ 100mA

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