

Features

- Input Voltage Range: 5V to 60V
- 5A Output Current
- Power-On-Reset Monitoring on VCC
- 0.6V±1% Internal Reference Voltage
- 95% Efficiency at 500kHz (12Vin, 5Vout, 1.5A)
- Selectable FPWM or Automatic Operation
- Adjustable Frequency Range: 300kHz to 2.2MHz
- Adjustable Soft-Start
- Protections
 - Programmable Current Limit
 - Under Voltage Protection with Hiccup Mode
 - Over Temperature Protection
- Power Good Indicator
- Available in TQFN5x5-24 Package

Applications

- Doorbell
- Automotive DVR
- General DC/DC Converter Applications

General Description

The APW7710 is a wide input voltage range synchronous step-down DC-DC converter that can deliver up to 5A output current with a 5V to 60V input supply. The exceptional efficiency and output accuracy provided in a smaller solution size make APW7710 easier to use.

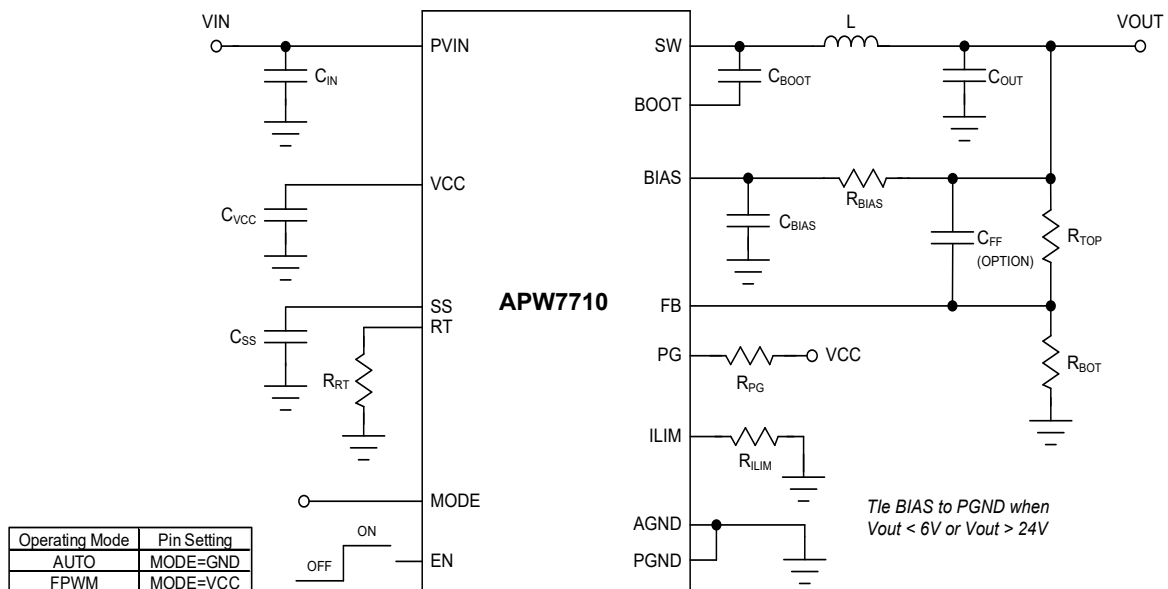
The APW7710 uses a peak current mode control scheme to regulate the output voltage. Auto mode selection is provided to improve the efficiency when the device operates in light load.

BIAS bypass pin allows for connecting VOUT to power the internal control circuitry under the output voltage range of 6V~24V application, thereby reducing overall system power consumption for better efficiency.

Under-voltage protection with hiccup mode provides cycle-by-cycle current limit protection against shorted output and soft-start eliminates inrush current during start-up.

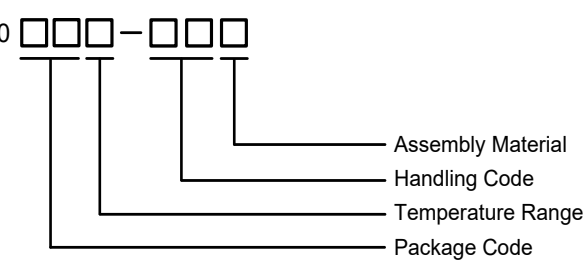

Adjustable switching frequency, soft start, current limit, FPWM option provide flexible application. Additional features such as input under-voltage lock-out, output over-voltage protection, over-temperature protection offer completely safe and smooth operation in applied conditions.

Simplified Application Circuit



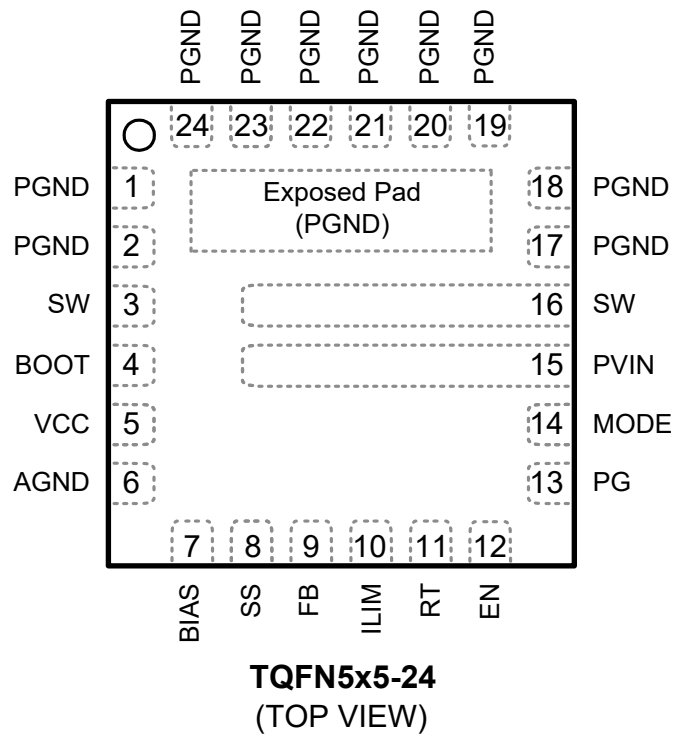
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APW7710 <input type="checkbox"/><input type="checkbox"/><input type="checkbox"/>-<input type="checkbox"/><input type="checkbox"/><input type="checkbox"/></p>  <p>Assembly Material Handling Code Temperature Range Package Code</p>	<p>Package Code QB : TQFN5x5-24 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Green part</p>
<p>APW7710 QB:  XXXXX : Date Code</p>	

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PVIN}	PVIN to GND Voltage	-0.3 ~ 65	V
V_{BIAS}	BIAS to GND Voltage	-0.3 ~ Lower of ($V_{IN}+0.3$) or 30V	V
V_{EN}	EN to GND Voltage	-0.3 ~ 65	V
V_{BOOT}	BOOT to GND Voltage	-0.3 ~ 70	V
V_{SW}	SW to GND Voltage	-0.3 ~ 65	V
Other Pins	VCC, FB, SS, ILIM, RT, PG, MODE	-0.3 ~ 6	V
T_J	Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	20	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 2)	12	°C/W

Note 2: θ_{JA} and θ_{JC} is measured with the component mounted on a high effective thermal conductivity test board in free air.

ESD Ratings

Symbol	Parameter	Range	Unit
$V_{(ESD)}$	Min. Charged-Device Model	750	V
	Min. Machine Model ESD Rating	200	V
	Min. Human Body Model ESD Rating	2	kV

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{PVIN}	PVIN to GND Voltage	5 ~ 60	V
V_{CC}	VCC to GND Voltage	4.5 ~ 5.5	V
V_{BIAS}	BIAS to GND Voltage	6 ~ Lower of ($V_{IN}+0.3$) or 24V	V
V_{EN}	EN to GND Voltage	0 ~ 60	V
V_{OUT}	Adjustable Output Voltage Range	3.3 ~ 95%VIN	V
I_{OUT}	Converter Output Current	5	A
R_{ILIM}	Resistor Setting Range of ILIM	39k ~ 150k	Ω
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}=34V$, $T_A=25^{\circ}C$.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY						
$V_{IN_POR_R}$	VIN POR Rising Threshold Voltage	V_{IN} Rising	4.6	4.7	4.8	V
$V_{IN_POR_F}$	VIN POR Falling Threshold Voltage	V_{IN} Falling	4.2	4.3	4.4	V
I_Q	VIN Supply Current	$V_{IN}=60V$, $V_{FB}=1V$, No Load, Auto Mode	-	170	-	μA
I_{SW}	Switching Current	$V_{IN}=60V$, $F_{SW}=500kHz$, No Load	-	10	-	mA
I_{SD}	VIN Shutdown Current	$V_{IN}=60V$, $V_{EN}=0V$	-	5.5	-	μA
INTERNAL LDO						
V_{CC}	VCC Output Voltage	$6V \leq V_{IN} \leq 60V$, $I_{VCC}=0A$	4.75	5	5.25	V
		$6V \leq V_{IN} \leq 60V$, $I_{VCC}=30mA$	4.75	5	5.25	V
I_{VCC}	VCC Supply Current	$V_{IN}=V_{EN}=60V$, $V_{CC}=5V$, $F_{SW}=500kHz$	-	10	-	mA
$V_{CC_POR_R}$	VCC POR Rising Threshold Voltage	V_{CC} Rising	3.7	4	4.3	V
$V_{CC_POR_F}$	VCC POR Falling Threshold Voltage	V_{CC} Falling	3.4	3.6	3.8	V
T_{SS_VCC}	Internal VCC Soft Start Time	Time to Ramp V_{CC} from 0% to 90%, No Load	-	1	-	ms
V_{CC_UVP}	VCC UVP Threshold	V_{CC} Falling	-	55	-	%
$V_{CC_UVP_HYS}$	VCC UVP Threshold Hysteresis	V_{CC} Rising	-	5	-	%
T_{HICCUP_VCC}	VCC Hiccup Count Times		-	8	-	t_{SS_VCC}
I_{LEAK_BIAS}	BIAS Leakage Current	$V_{IN}=V_{EN}=GND$, $V_{BIAS}=24V$	-	-	1	μA
V_{BIAS_ON}	VBIAS Turn On Threshold Voltage	V_{BIAS} Rising	4.5	4.7	5	V
V_{BIAS_OFF}	VBIAS Turn Off Threshold Voltage	V_{BIAS} Falling	4.2	4.4	4.7	V
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage		-	0.6	-	V
	Voltage Accuracy	$T_A=25^{\circ}C$	1	-	1	%
		$T_A=-40^{\circ}C \sim 85^{\circ}C$	1.5	-	1.5	%
I_{LEAK_FB}	FB Leakage Current	V_{FB} to GND=5V	-	-	0.1	μA
OSCILLATOR						
F_{SW}	PWM Mode Setting Range		300	-	2200	kHz
	Frequency Accuracy	FPWM Mode	-15	-	15	%
T_{ON_MIN}	Minimum On Time		-	115	-	ns
T_{OFF_MIN}	Minimum Off Time		-	53	-	ns
SOFT-START, ENABLE AND MODE						
T_{SS}	Internal Soft-Start Time	SS Pin=Floating, From V_{OUT} 5% to 95%	-	4	-	ms
I_{SSC}	Soft-Start Charging Current		-	1.37	-	μA
V_{EN_H}	EN Threshold High Voltage		0.8	1	1.2	V
V_{EN_HYS}	EN Hysteresis		-	0.25	-	V
I_{EN}	Enable Input Current	$V_{IN}=V_{EN}=34V$	-	120	-	μA
I_{LEAK_EN}	Enable Leakage Current	$V_{IN}=0V$, $V_{EN}=60V$	-	-	46	μA
EN_ON_DB	Enable Turn On Delay Time	SS Pin=Floating	-	1.8	-	ms
V_{MODE_H}	Into PWM Mode High Threshold		1.1	1.4	1.6	V
V_{MODE_HYS}	PWM Mode Hysteresis		-	0.7	-	V
I_{MODE}	Mode Input Current	$V_{IN}=V_{CC}=V_{MODE}=5.5V$	-	1	-	μA

Electrical Characteristics (Cont.)

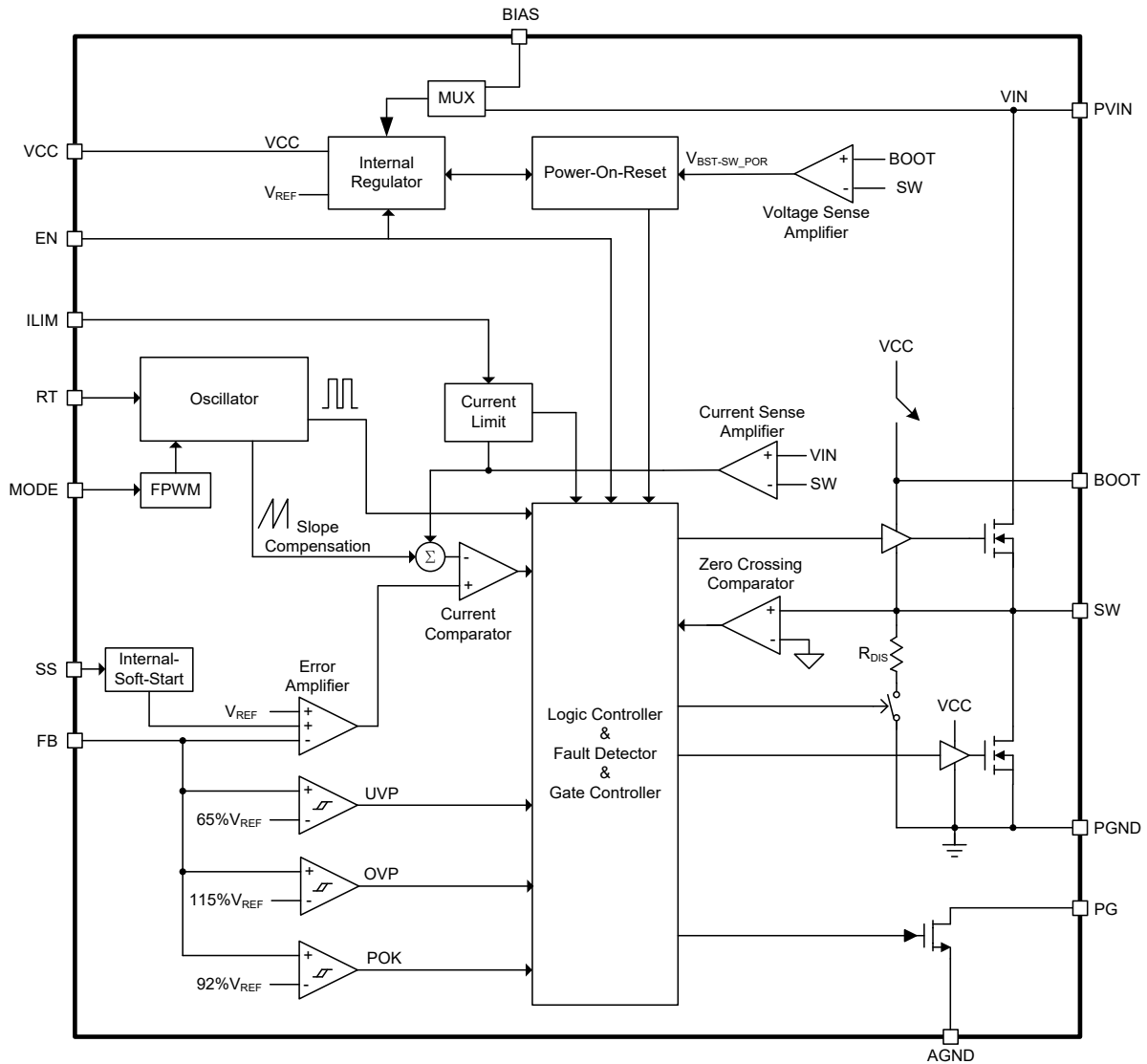
Unless otherwise specified, these specifications apply over $V_{IN}=34V$, $T_A=25^{\circ}C$.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
POWER MOSFET AND BOOTSTRAP POWER						
$R_{DS(ON)_H}$	High-Side MOSFET Resistance	$V_{IN}=34V$, $I_{SW}=0.5A$	-	85	-	m Ω
I_{LEAK_H}	High Side MOSFET Leakage Current	$V_{IN}=60V$, $V_{SW}=GND$	-	-	20	μA
$R_{DS(ON)_L}$	Low-Side MOSFET Resistance	$V_{IN}=34V$, $I_{SW}=0.5A$	-	40	-	m Ω
I_{LEAK_L}	Low Side MOSFET Leakage Current	$V_{SW}=V_{IN}=60V$, No Switching	-	-	40	μA
V_{BOOT}	BOOT to SW Output POR Voltage	$V_{IN}=34V$, $V_{BOOT} - V_{SW}$	-	3.3	-	V
R_{BOOT}	BOOT Switch On Resistance	$V_{IN}=34V$, $I_{BOOT}=10mA$	-	10	-	Ω
I_{LEAK_BST}	BOOT Leakage Current	$V_{BOOT} - V_{SW}=5.5V$, $V_{BOOT-GND}=65.5V$, $V_{SW}=60V$	-	-	0.6	μA
PROTECTIONS						
I_{LIMIT_H}	High-Side Current Limit	$R_{ILIM}=39k$	6.3	7	-	A
I_{LIMIT_L}	Low-Side Current Limit	$R_{ILIM}=39k$	3.86	4.55	-	A
T_{HICCUP}	Hiccup Count Times		-	8	-	t_{SS}
UVP	Output Under Voltage Threshold	V_{OUT} Falling	-	65	-	%
	Under Voltage Threshold Hysteresis	V_{OUT} Rising	-	5	-	%
OVP	Output Over Voltage Threshold	V_{OUT} Rising	-	115	-	%
	Over Voltage Threshold Hysteresis	V_{OUT} Falling	-	5	-	%
R_{DIS}	Output Discharge Resistor	$V_{EN}=0V$, $V_{OUT}=20V$	-	710	-	Ω
OTP	Over Temperature Protection		-	160	-	$^{\circ}C$
OTP _{HYS}	Over Temperature Hysteresis		-	30	-	$^{\circ}C$
PGOOD INDICATOR						
V_{PG}	PG Threshold	PG In (PG go High), Output Voltage Rising	87	91	95	% V_{REF}
		PG Out (PG go Low), Output Voltage Falling	83	88	93	% V_{REF}
		PG Out (PG go Low), Output Voltage Rising	108	115	122	% V_{REF}
		PG In (PG go High), Output Voltage Falling	103	110	117	% V_{REF}
		PG Hysteresis	-	2	-	% V_{REF}
I_{PG}	PG Leakage Current	$V_{PG}=5V$	-	-	0.1	μA
I_{SINK_PG}	PG Sink Capability	$V_{PG}=0.4V$	-	85	-	mA
$T_{DB_PG_R}$	PG Low to High Debounce Time		-	115	-	us

Pin Description

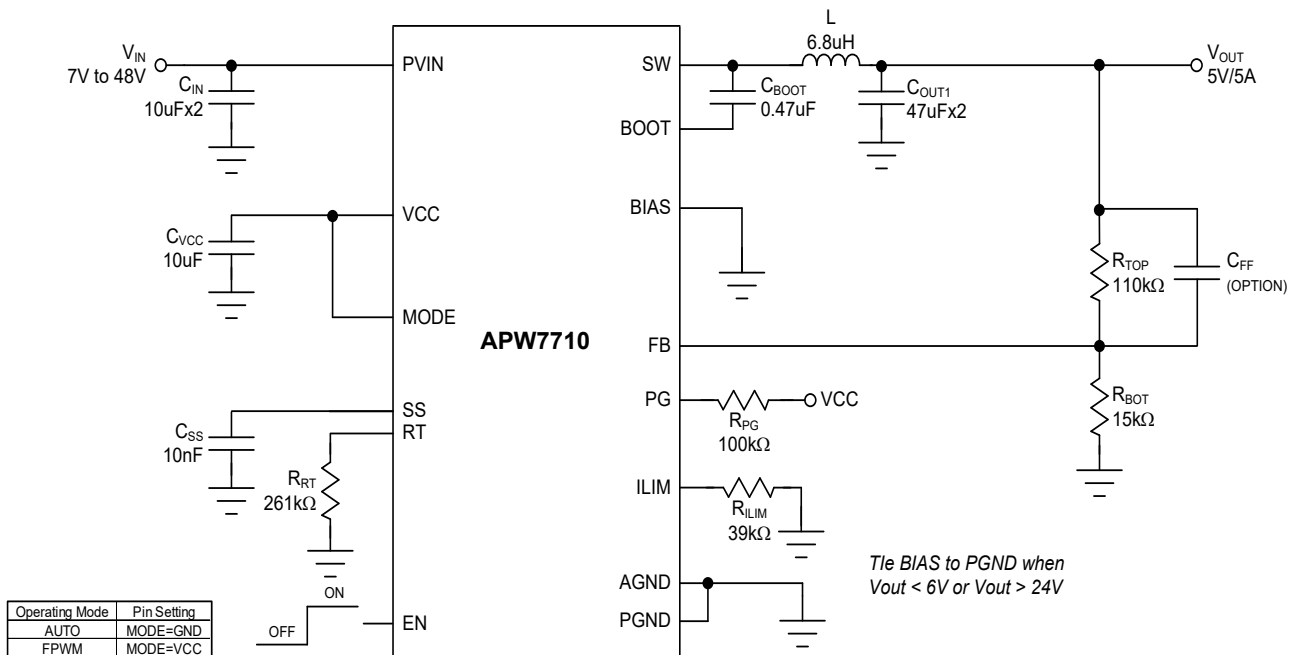
PIN		FUNCTION
NO.	NAME	
1, 2, 17 ~ 25	PGND	Power ground, connected to system ground and GND plane on the PCB.
3, 16	SW	Switching output of the regulator. Internally connected to source of the HS MOSFET and drain of the LS MOSFET. Connect to the output inductor and boot-strap capacitor.
4	BOOT	Boot-strap capacitor connection for High-Side Gate Driver. Place a 0.47 μ F capacitor to connect SW pin and BOOT pin to provide a bootstrap voltage to drive the HS MOSFET.
5	VCC	Output of internal bias supply. The internal regulator provides an 5V-VCC for the internal control circuitry. It is recommended to connect a 2.2 μ F capacitor from this pin to ground and do not apply loading by external circuitry.
6	AGND	Analog ground. Ground reference for internal references and logic. Connect to system ground on PCB.
7	BIAS	It is recommended to tie this pin to VOUT through a series resistor in the range of 10 Ω to 20 Ω when the voltage is between 6V and 24V, or to an external power rail within the recommended voltage range, in order to improve efficiency. When this pin is used, place a 1 μ F capacitor from the pin to ground. If not used, tie the pin directly to ground.
8	SS	Soft-start-control pin. Connect a capacitor to GND to set the soft start interval. Leave this pin floating to use the shortest internal soft-start time.
9	FB	Feedback input for output voltage regulation. Senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.
10	ILIM	Current limit threshold setting pin. Connect a setting resistor to GND. ILIM is a constant voltage pin through a resistor to ground that generate current to be internal current limit threshold reference.
11	RT	Switching frequency setting pin. Place a resistor from this pin to ground to set the switching frequency.
12	EN	Enable pin. When EN goes high, the device is enabled. Contrarily, IC shuts down when EN is low. Do not float this pin.
13	PG	Power good output. PG is an open drain output used to indicate the status of the output voltage. Connect the PG to VCC or external supply rail through a resistor.
14	MODE	FPWM setting pin. Pull this pin logic low: operation in automatic mode, improved light loads efficiency; tie to logic high: operation in FPWM mode with constant switching frequency. Never leave this pin floating.
15	PVIN	Supply input to internal LDO and power stage. Connect capacitors C _{IN} to this pin that stable the input power of regulator. C _{IN} must be placed close to PVIN and PGND in a short path.

Block Diagram



Typical Application Circuit

400kHz, 5V, 5A Step-Down Converter



Designator	Value	Case size	Part Number
L	6.8uH	7.6mmX7.8mm	TUP0707W-6R8M
C _{IN}	10uF/63V	1210(inch)	GRM32ER71J106KA12L
C _{OUT1}	47uF/10V	1210(inch)	GRM32ER71A476KE15L

Function Descriptions

Operation

The APW7710 is a wide input voltage range step-down converter using current mode control to regulate the output voltage. The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier. The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage. The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Power-On-Reset / VCC Power-On-Reset

The VCC POR function is used to prevent the IC from operating erroneously when the VCC voltage is insufficient. When the chip is powered by a VIN above the $V_{IN_POR_R}$ threshold and the EN signal is above the V_{EN_H} level, the VCC voltage begins to ramp up. During this process, the IC continuously monitors the voltage at the VCC pin. The VOUT soft-start is triggered once the VCC voltage exceeds its respective threshold.

Soft-Start and EN Delay Time

The APW7710 provides a programmed soft-start function that controls a predictable slew rate of the output voltage during ramp-up to reduce input current surges and prevent output overshooting.

The soft-start and EN delay times can be programmed by connecting an external capacitor between SS and GND.

The corresponding typical values can be found in Table 1:

Table 1. C_{SS} Corresponding Timetable

C _{SS} (nF)	EN-Delay (ms)	Soft-Start (ms)	EN High to PG High (ms)
NC	1.8	4	6
10	5.4	7.6	13
22	6	10	16
47	9	25	34
100	14	49	63

The soft-start function will be enabled when any condition can initiate an output start-up, such as VIN power to the IC or toggling the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Over-Temperature Protection (OTP)

The IC includes an over-temperature protection (OTP) circuitry by monitoring the chip's junction temperature to prevent damage due to operating at extremely high temperatures. The OTP will shut down switching operation when the junction temperature exceeds the OTP threshold value. Once the junction temperature cools down and lower than the hysteresis threshold, the IC will restart a new soft-start cycle and regulate the output voltage again.

Enable and Shutdown

The enable input (EN) controls the ON/OFF functionality. Drive EN pin voltage higher than V_{EN_H} to turn on the converter and apply a voltage less than V_{EN_H} minus the V_{EN_HYS} to shut down the APW7710.

Current Limit

The APW7710 uses the internal High-side and Low-side MOSFET's $R_{DS(ON)}$ as a current-sensing element to monitors the current through the high-side MOSFET. The current limit function has both valley current limit and peak current limit algorithm (See Figure 1).

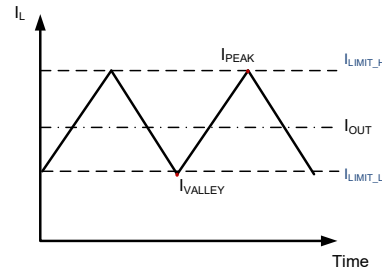


Figure 1.

The high-side switch current (peak current) is compared to the current point that set (I_{LIMIT_H}). If the magnitude of the current-sense signal at SW pin is above the current limit threshold the PWM is not allowed to initiate a new cycle. Similarly, if the low-side switch current (Valley current) is exceeding I_{LIMIT_L} , the Low-side MOSFET remains on, and the High-side switch is turned off. Therefore, the inductor current continues decrease until the inductor current drops below I_{LIMIT_L} . Once the Low-side current falls below the I_{LIMIT_L} , the High-side switch is turned on again after a dead time.

The high-side current-limit threshold is set by the RILIM resistor between the ILIM pin and GND. Choose a current limit resistor according to the following equation:

$$RILIM(\Omega) = \frac{75k}{0.3 \times I_{LIMIT_H}(A) - 0.15}$$

The $I_{LIMIT_L} = I_{LIMIT_H} * 0.65$ typically.

The combination of high/low side current protection is more effective in preventing IC from being damaged in the event of an overload or short circuit. When the current limit protection is activated, the output current is limited. And the output voltage will drop down if the output load continues to increase.

Over-Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage condition. If the output voltage exceeds 115% of regulate voltage, the over-voltage protection is triggered, both high-side and low-side gate drivers are pull low until the output voltage downward to below 110% of regulate voltage, and the IC converter's MOSFETs return to its switching state.

Under-Voltage Protection and Hiccup

The IC detects under-voltage conditions by monitoring the feedback voltage on FB pin after internal soft start signal is okay. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the APW7710 enters hiccup mode to periodically restart the part (wait for $8 \times T_{SS}$ typical). The cycle-by-cycle current limit protection is especially useful to shortened outputs. The average short-circuit current is greatly alleviate the chip from thermal issues and protect the regulator. Once the output voltage is higher than UVP Hysteresis threshold, the regulator exits the hiccup mode and resumes normal operation again.

Function Descriptions (Cont.)

FPWM and Auto Mode

The APW7710 is allowed to either operate in fixed frequency PWM mode or in an automatic PSM/PWM mode by the MODE pin setting. If this pin is pull high and above the MODE's threshold voltage, the regulator will be always in a fixed frequency mode of user setting regardless any vary of the output load current. Contrary, the regulator operates in an automatic PSM/PWM mode when MODE pin is connected to ground.

About switching frequency of FPWM, setting range at 300kHz to 2.2MHz. It should be noted that the setting frequency would be affected if duty on time less than minimum on time of APW7710. To operate the regulator at different frequencies, use equation as below to calculate the required resistor value for RT.

$$R_T = \left(\frac{1}{\text{Frequency (Hz)} - 200n} \right) \div 8.8p$$

The unit for the R_T is Ω .

Fast Discharge

When EN signal goes low, Over-Temperature Protection occurred or the VCC voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered.

An internal discharge path between the SW and the ground of the converter turns on when the discharge function is triggered to allow the output energy to quickly discharged through this path.

Power Good (PG)

PG is an open-drain output that indicates the output regulation state. In normal operation, the PG window is from 91% to 115% typically of the converter's reference voltage. When the output voltage stays within this window, PG signal will become high. When the output voltage outruns the target of window range, PG signal will be pulled low. Since PG is an open-drain output device, it requires an external pull-up resistor. However, if the pin is not used, no resistor is needed.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, two pieces of 22uF capacitor are sufficient.

Since the input capacitor (C_{IN}) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. Using a small, high-quality ceramic capacitor should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient. Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended due to their better temperature and voltage characteristics. The output voltage ripple caused by the capacitance can be estimated by:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times F_{OSC} \times C_{OUT}}$$

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage. The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result. A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductor value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current. To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency.

Output Voltage Setting

The output voltage can be adjusted by setting the resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing and the output voltage can be calculated as below:

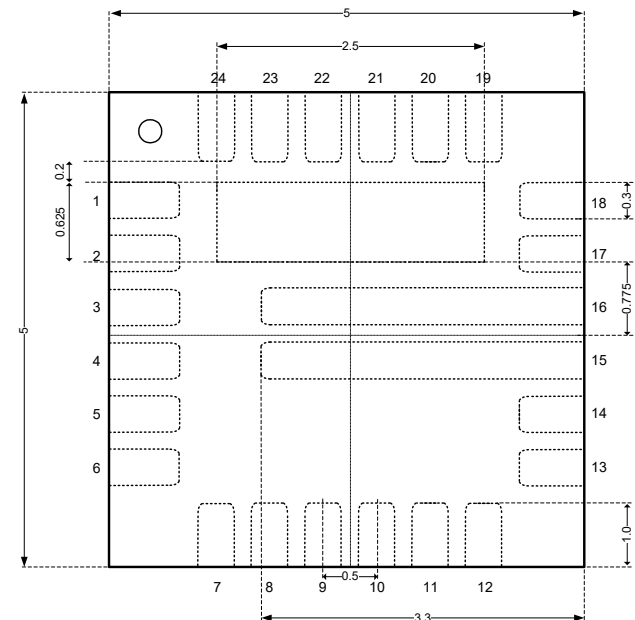
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN and VOUT capacitor should be placed close to the IC and PGND pins with short and wide trace.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible.
3. Place the inductor as close as possible to the SW pin to minimize noise coupling into other circuits.
4. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
5. For better heat dissipation, it is recommended to place a large ground plane under the thermal pad of all PCB layers and place as many vias as possible on the thermal pad from the top layer to the bottom layer.

Recommended Minimum Footprint

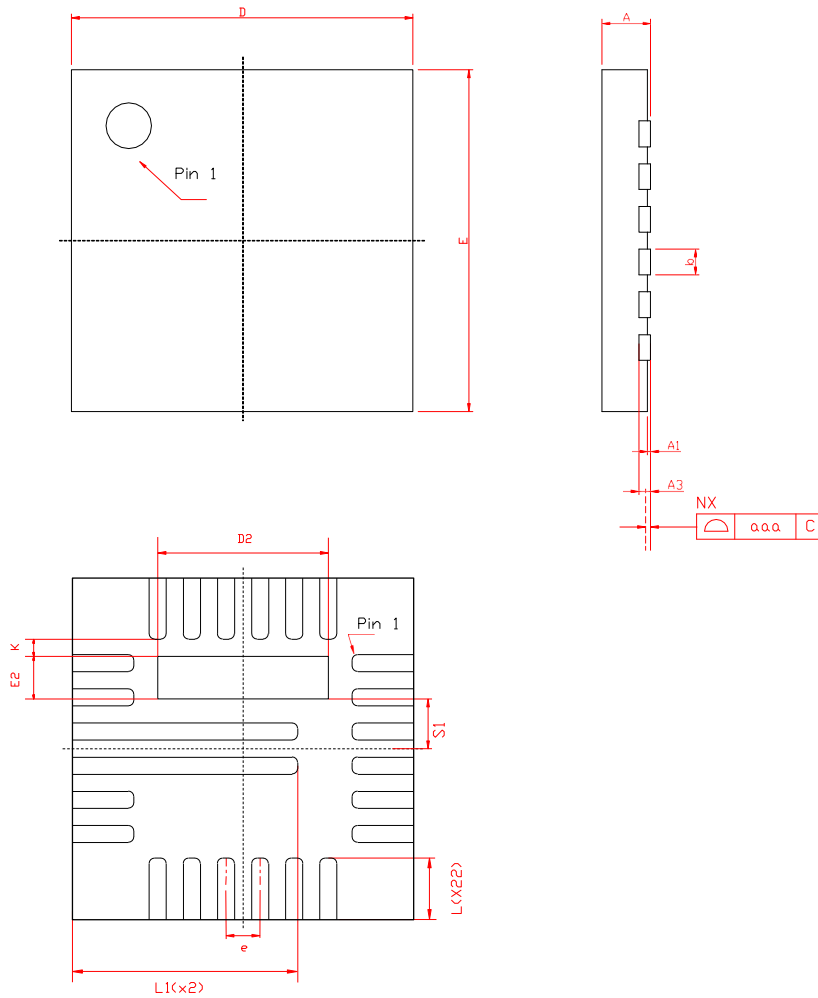


Unit: mm

* Just Recommend

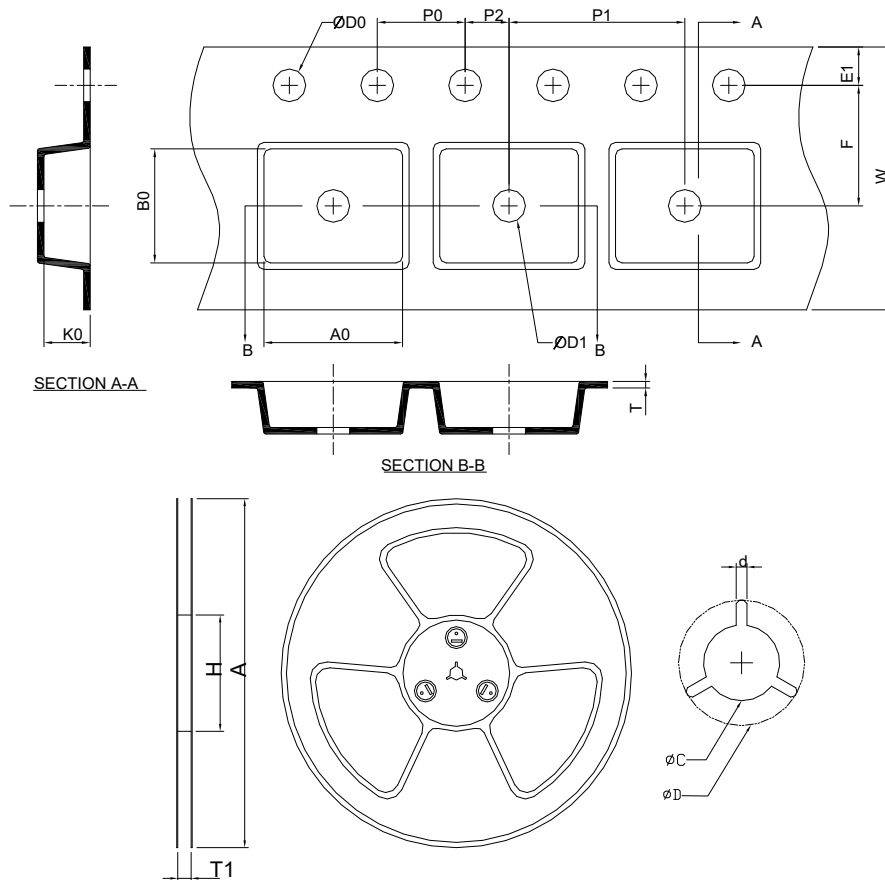
Package Information

TQFN5x5-24



SYMBOL	TQFN5x5-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	4.90	5.10	0.193	0.201
D2	2.40	2.60	0.094	0.102
E	4.90	5.10	0.193	0.201
E2	0.575	0.675	0.023	0.027
e	0.50 BSC		0.020 BSC	
L	0.80	1.00	0.031	0.039
L1	3.20	3.40	0.126	0.134
K	0.20		0.008	
S1	0.775 REF		0.031 REF	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

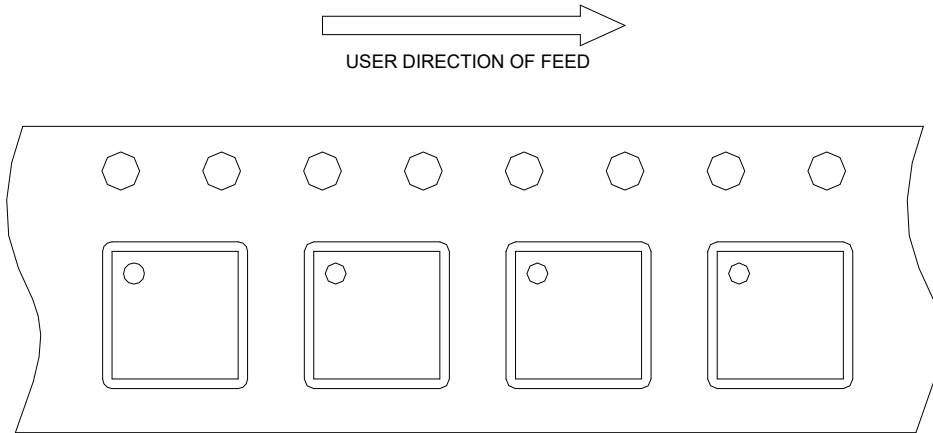
(mm)

Devices Per Unit

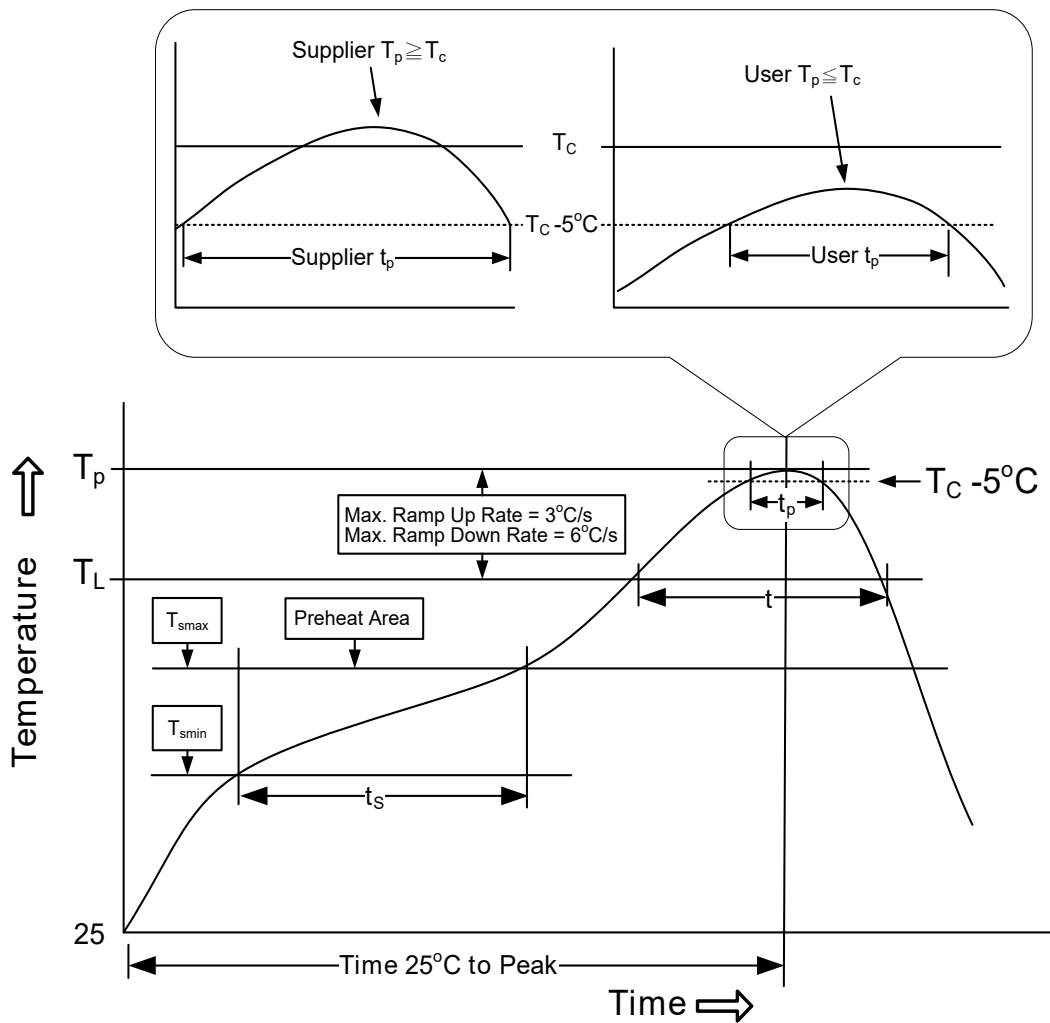
Package Type	Packing	Quantity
TQFN 5x5	Tape & Reel	2500

Taping Direction Information

TQFN5x5-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100°C	150°C
Temperature max (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test Item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD-78	10ms, $1_{tr} \geq 100\text{mA}$

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