APW7720

The PMIC Features 7 Buck Converters, 6 LDOs, 2 LSs, and Flexible System Settings via I²C and MTP

Features

- **3.5V to 5.5V Operating Input Range**
- **Built-in UVLO, OVP for Main Input Voltage**
- **Built-in 7 High-Efficiency Step-Down Converters**
  - **BUCK1: 0.45V ~ 1.275V, 3.75mV Step, 6A**
  - **BUCK2: 1V ~ 3.4V, 10mV Step, 2A**
  - **BUCK3: 0.45V ~ 1.275V, 3.75mV Step, 6A**
  - **BUCK4: 0.6V ~ 1.54V, 5mV Step, 3A**
  - **BUCK5: 0.45V ~ 1.275V, 3.75mV Step, 3A**
  - **BUCK6: 1V ~ 3.4V, 10mV Step, 2A**
  - **BUCK7: 1V ~ 3.4V, 10mV Step, 2A**
- **Configurable Dual Phase or Single Phase Regulator for BUCK1/BUCK3**
- **Configurable PWM Switching Frequency from 400kHz to 2.5MHz**
- **Programmable Automatic PFM/PWM Mode, Forced PWM Mode**
- **Adjustable Ramp-Up Time and Ramp-Down Time for BUCK1 ~ BUCK7**
- **Built-in RTC Dedicated LDO and 5 Low-Noise LDOs**
  - **RTCLDO: 1.8V, 2.5V, 3.3V, 10mA**
  - **LDO2: 1V ~ 3.4V, 50mV Step, 300mA**
  - **LDO3: 1V ~ 3.4V, 50mV Step, 300mA**
  - **LDO4: 0.6V ~ 1.23V, 10mV Step, 200mA**
  - **LDO5: 1V ~ 3.4V, 50mV Step, 150mA**
  - **LDO6: 0.6V ~ 1.23V, 10mV Step, 300mA**
- **Configurable LDO2/3 output 1.8V/3.3V by LDO2/3_SEL Pin**
- **Built-in Dual Sets of Logic Control Signal Outputs, Selectable at 1.8V or 3.3V**
- **Built-in Double Thermal Protection with Temperature Alarm and Thermal Shutdown**
- **Built-in Output Over Voltage Protection (OVP), Output Under Voltage Protection (UVP), Current Limit**
- **Built-in Interrupt Control and Reporting by /INT Pin**
- **Built-in PGOOD to Indicate the Power Status of All VRs**
- **I²C Bus and User Programmable MTP**
- **Programmable Power Sequence Control for All Channels via I²C**
- **Built-in Watchdog Timer, Programmable via I²C**
- **Supports Self-Refresh Mode via Off Mode Function**
- **Available in TQFN6x6-52B Package**

General Description

The APW7720 is a Power Management IC (PMIC) designed to provide complete power management solution for Surveillance Cam, IP Cam and Video Conference-Call applications. It integrates a PWM power stage and well-designed control circuitry to minimize the need for external components, thereby simplifying layout in constrained PCB areas.

This device features 7 adjustable output voltage buck converters, 6 adjustable output voltage low-noise LDOs, and 2 sets of built-in logic control signal outputs selectable at 1.8V or 3.3V, all of which can be configured via I²C.

The APW7720 features protection functions against over current, output over/under voltage, VSYS over voltage and over temperature to prevent catastrophic failure. Fault events also cause a state change on the PGOOD and /INT output pins, which is helpful for interrupt control or debugging. Additionally, it integrates two Under-Voltage Lockout (UVLO) features to monitor the voltages of VSYS and VINLDO1, thereby preventing improper operation during power-up and power-down.

An I²C interface is provided in this device for the system designer to customize settings or presets using Multi-Time Programmable (MTP) features, including power-up/down sequence, output voltage, ramp-up/down time, power-good delay time, watchdog timer, PWM switching frequency, forced PWM mode or automatic PFM/PWM mode, output discharge mode or ramp-down mode, and latch off mode or auto-reboot mode. These customizable MTP settings give system designers the flexibility to optimize performance for various use cases, ensuring efficient and reliable operation.

The APW7720 is a halogen-free and lead-free device, compliant with RoHS, and available in a TQFN6x6-52B package.

Applications

- **IP-Cam**
- **Security**
- **Drone**
- **Video Conferencing System**

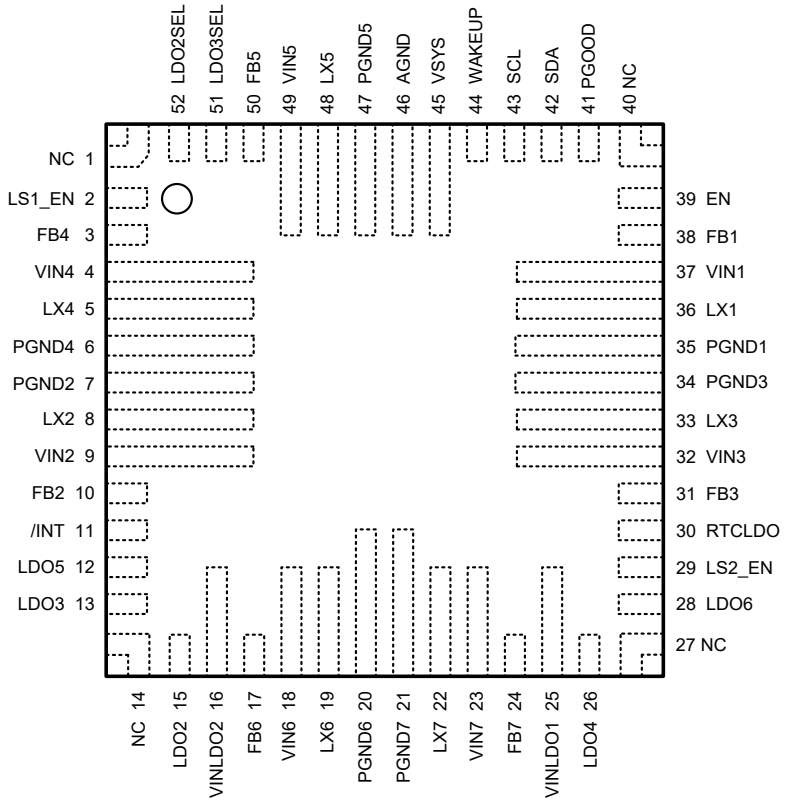
Ordering and Marking Information

APW7720 – □□ □□□-□□□ Assembly Material Handling Code Temperature Range Package Code Product Code	Product Code 00, 01, 02··· Package Code QB : TQFN6x6-52B Operating Ambient Temperature Range I : -40 to 105°C Handling Code TR : Tape & Reel Assembly Material G : Green Part

APW7720-00 QB:	00 APW7720 XXXXX ●	X - Date Code	APW7720-01 QB:	01 APW7720 XXXXX ●	X - Date Code
APW7720-02 QB:	02 APW7720 XXXXX ●	X - Date Code	APW7720-03 QB:	03 APW7720 XXXXX ●	X - Date Code
APW7720-04 QB:	04 APW7720 XXXXX ●	X - Date Code	APW7720-05 QB:	05 APW7720 XXXXX ●	X - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



TQFN6x6-52B
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{SYS}	VSYS to AGND Voltage	-0.3 to 6.5	V
V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}, V_{IN5}, V_{IN6}, V_{IN7}	VIN1 ~ VIN7 to PGND Voltage	-0.3 to 6.5	V
V_{LX1}, V_{LX2}, V_{LX3}, V_{LX4}, V_{LX5}, V_{LX6}, V_{LX7}	LX1 ~ LX7 to PGND Voltage	-0.3 to 6.5	V
V_{FB1}, V_{FB2}, V_{FB3}, V_{FB4}, V_{FB5}, V_{FB6}, V_{FB7}	FB1 ~ FB7 to AGND Voltage	-0.3 to 6.5	V
$V_{VINLDO1}$, $V_{VINLDO2}$	VINLDO1, VINLDO2 to AGND Voltage	-0.3 to 6.5	V
	EN, WAKEUP, LDO2SEL, LDO3SEL, SDA, SCL, /INT, PGOOD to AGND	-0.3 to 6.5	V
	PGND to AGND	-0.3 to 0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	15	°C/W
θ_{JC}	Junction-to-Case Resistance in free air	4	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{SYS}	Main Input Voltage	3.5 to 5.5	V
V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}, V_{IN5}, V_{IN6}, V_{IN7}	BUCK1 ~ BUCK7 Input Voltage	3.5 to 5.5	V
V_{INLDO1}	LDO4, LDO6 Input Voltage	$V_{LDO4,\ 6}$ + V_{DROP} to 5.5	V
V_{INLDO2}	LDO2, LDO3, LDO5 Input Voltage	V_{SYS} to 5.5	V
V_{LS1_EN}, V_{LS2_EN}	LS1_EN, LS2_EN Output Voltage Range	0 ~ 1.8 or 3.3	V
V_{DC1}	BUCK1 Output Voltage Range (3.75mV/Step)	0.45 ~ 1.275	V
I_{DC1}	BUCK1 Output Current Range	~ 6	A
V_{DC3}	BUCK3 Output Voltage Range (3.75mV/Step)	0.45 ~ 1.275	V
I_{DC3}	BUCK3 Output Current Range	~ 6	A
V_{DC2}	BUCK2 Output Voltage Range (10mV/Step)	1 ~ 3.4	V
I_{DC2}	BUCK2 Output Current Range	~ 2	A
V_{DC4}	BUCK4 Output Voltage Range (5mV/Step)	0.6 ~ 1.54	V
I_{DC4}	BUCK4 Output Current Range	~ 3	A
V_{DC5}	BUCK5 Output Voltage Range (3.75mV/Step)	0.45 ~ 1.275	V
I_{DC5}	BUCK5 Output Current Range	~ 3	A
V_{DC6}	BUCK6 Output Voltage Range (10mV/Step)	1 ~ 3.4	V
I_{DC6}	BUCK6 Output Current Range	~ 2	A
V_{DC7}	BUCK7 Output Voltage Range (5mV/Step)	1 ~ 3.4	V
I_{DC7}	BUCK7 Output Current Range	~ 2	A
fsw	Switching Frequency Setting Range	400 ~ 2500	kHz
V_{RTC}	RTCLDO Output Voltage Range	1.8, 2.5, 3.3	V
I_{RTC}	RTCLDO Output Current Range	~ 10	mA
V_{LDO2}	LDO2 Output Voltage Range (50mV/Step)	1 ~ 3.4	V
I_{LDO2}	LDO2 Output Current Range	~ 300	mA
V_{LDO3}	LDO3 Output Voltage Range (50mV/Step)	1 ~ 3.4	V
I_{LDO3}	LDO3 Output Current Range	~ 300	mA
V_{LDO4}	LDO4 Output Voltage Range (10mV/Step)	0.6 ~ 1.23	V
I_{LDO4}	LDO4 Output Current Range	~ 200	mA
V_{LDO5}	LDO5 Output Voltage Range (50mV/Step)	1 ~ 3.4	V
I_{LDO5}	LDO5 Output Current Range	~ 150	mA
V_{LDO6}	LDO6 Output Voltage Range (10mV/Step)	0.6 ~ 1.23	V
I_{LDO6}	LDO6 Output Current Range	~ 300	mA
T_A	Ambient Temperature	-40 ~ 105	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
VSYS SUPPLY CURRENT						
I_{VSYS}	VSYS Supply Current in Dual-phase	All VRs are enabled in PFM mode and all LX will not switch (VDC1 and VDC3 operate in dual-phase mode)	-	1.0	1.5	mA
I_{VSYS}	VSYS Supply Current in Single-phase	All VRs are enabled in PFM mode and all LX will not switch (VDC1 and VDC3 respectively operate in single-phase mode)	-	0.75	1.3	mA
$I_{VINLDO1}$	VINLDO1 Supply Current	Both LDO4 and LDO6 are enabled	-	15	25	μA
$I_{VINLDO2}$	VINLDO2 Supply Current	LDO2, LDO3 and LDO5 are all enabled. LDO2SEL=LDO3SEL=L	-	100	160	μA
I_{VSYS_SR}	VSYS Supply Current in Self-Refresh Mode	In Off Mode, only BUCK4 and LDO5 are in PFM mode, and other VRs are disabled	-	120	170	μA
$I_{VINLDO2\_SR}$	VINLDO2 Supply Current in Self-Refresh		-	26	40	μA
I_{VSYS_SD}	VSYS Shutdown Current	T_J=25°C, all VRs are disabled	-	17	25	μA
MAIN INPUT UVLO						
$V_{SYS\_UVLO\_R}$	VSYS UVLO Rising Threshold		2.9	3.0	3.1	V
$V_{SYS\_UVLO\_F}$	VSYS UVLO Falling Threshold		2.7	2.8	2.9	V
	VSYS UVLO Hysteresis		-	0.2	-	V
	VSYS UVLO Falling Debounce Time	(Note 4)	-	20	-	μs
$V_{SYS\_OVP\_R}$	VSYS OVP Rising Threshold		5.8	6	6.2	V
$V_{SYS\_OVP\_F}$	VSYS OVP Falling Threshold		5.4	5.6	5.8	V
	VSYS OVP Rising Delay Time	(Note 4)	-	8	-	μs
LDO INPUT UVLO						
$V_{INLDO1\_UVLO\_R}$	VINLDO1 Rising UVLO Threshold	LDO4, 6 Rising UVLO	0.85	1	1.15	V
$V_{INLDO1\_UVLO\_F}$	VINLDO1 Falling UVLO Threshold	LDO4, 6 Falling UVLO	0.65	0.8	0.95	V
	VINLDO1 UVLO Hysteresis		-	0.2	-	V

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER ON TIME SLOT0 ~ 13 IDLE TIME						
td0_on ~ td13_on	Power On Time Slot 0 ~ 13 Idle Time Range	Selectable via MTP setting. tdx_on=0.2ms, 2ms, 4ms, ...10ms, 12ms, 14ms (Typ.)	0.2	-	14	ms
	Power On Time Slot 0 ~ 13 Idle Time	PON_TSLOTx_IDLE[2:0]=000	-	0.2	-	ms
	Power On Time Slot 0 ~ 13 Idle Time	PON_TSLOTx_IDLE[2:0]=001	-	2	-	ms
	Power On Time Slot 0 ~ 13 Idle Time	PON_TSLOTx_IDLE[2:0]=111	-	14	-	ms
	Automatic Reboot Wait Time	LATCH_OFF[0]=0	-	1	-	ms
POWER OFF TIME SLOT0 ~ 13 IDLE TIME						
td0_off ~ td13_off	Power Off Time Slot 0 ~ 13 Idle Time Range	Selectable via MTP setting. tdx_on=0.2ms, 2ms, 4ms, ...10ms, 12ms, 14ms (Typ.)	0.2	-	14	ms
	Power Off Time Slot 0 ~ 13 Idle Time	POFF_TSLOTx_IDLE[2:0]=000	-	0.2	-	ms
	Power Off Time Slot 0 ~ 13 Idle Time	POFF_TSLOTx_IDLE[2:0]=001	-	2	-	ms
	Power Off Time Slot 0 ~ 13 Idle Time	POFF_TSLOTx_IDLE[2:0]=111	-	14	-	ms
POWER GOOD INDICATOR						
	PGOOD Delay Time Range	Selectable via MTP setting. t_{PG}=1ms, 2ms, 5ms, 10ms, ...70ms (Typ.)	1	-	70	ms
t_{PG}	PGOOD Delay Time	PGDELAY[7:4]=0011. All VRs are regulated	0.8xt_{PG}	10	1.2xt_{PG}	ms
	PGOOD Debounce Interval	(Note 4)	-	20	-	µs
	PGOOD Output Low Voltage	V_{EN}=0V, I_{PGOOD_SINK}=5mA	-	-	0.4	V
	PGOOD Leakage Current	V_{PGOOD}=5.5V	-	-	1	µA
/INT						
	Output Low Voltage	If any VR fault is detected, the /INT signal keeps low. Sink current 5mA	-	-	0.4	V
	Leakage Current	Force 5.5V	-	-	1	µA
	Pull Low Minimum Duration	For non-latching mode	-	100	-	µs
EN						
V_{IH}	Input Logic High Voltage	Execute the power-up sequence	1.5	-	-	V
V_{IL}	Input Logic Low Voltage	Executes power-down sequence, then clear the non-MTP registers to their default values and reload the MTP registers	-	-	0.4	V
	Enable Debounce Time	(Note 4)	-	1	-	µs
	Input Resistance		-	100	-	kΩ
	Re-enable Delay Duration	Power cycle the EN (Note 4)	-	3	-	ms
LDO2SEL, LDO3SEL						
V_{IH}	Input Logic High Voltage	MLDOSEL[0]=0, LDO2 or LDO3 Output is 1.8V	1.5	-	-	V
V_{IL}	Input Logic Low Voltage	MLDOSEL[0]=0, LDO2 or LDO3 Output is 3.3V	-	-	0.4	V
	Input Resistance		-	100	-	kΩ
SCL, SDA						
V_{IH}	Input Logic High Voltage		1.5	-	-	V
V_{IL}	Input Logic Low Voltage		-	-	0.4	V
V_{SDA_L}	SDA Output Low Voltage	(Note 4)	-	-	0.3	V
V_{SCL_L}	SCL Output Low Voltage	(Note 4)	-	-	0.3	V
	Leakage Current	Force 5.5V	-	-	1	µA

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
WAKEUP						
V_{IH}	Input Logic High Voltage	V_{WAKEUP} rising	1.5	-	-	V
V_{IL}	Input Logic Low Voltage		-	-	0.4	V
t_{WAKUP_H}	WAKEUP Rising Deglitch Time	Rising	500	-	-	μs
t_{WAKUP_L}	WAKEUP Falling Deglitch Time	Falling	500	-	-	μs
	Input Resistance		-	100	-	kΩ
TEMPERATURE ALARM						
	Temperature Alarm Threshold	(Note 4)	-	125	-	°C
	Temperature Alarm Hysteresis	(Note 4)	-	15	-	°C
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold	(Note 4)	-	155	-	°C
	Thermal Shutdown Hysteresis	(Note 4)	-	20	-	°C

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **RTCLDO**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
RTCLDO						
	Supply Current	(Note 4)	-	2.5	-	μA
V_{RTCLDO}	RTCLDO Output Voltage	Default voltage	-	1.8	-	V
			-	2.5	-	V
			-	3.3	-	V
I_{RTCLDO_Max}	RTCLDO Source Capability		-	-	10	mA
V_{RTCLDO}	RTCLDO Output Voltage Accuracy (V_{RTCLDO}=1.8V)	I_{OUT_RTCLDO}=0mA, T_J=25°C	1.782	1.8	1.818	V
		I_{OUT_RTCLDO}=0mA, T_J= -40 ~ 125°C	1.764	1.8	1.836	V
	RTCLDO Output Voltage Accuracy (V_{RTCLDO}=2.5V)	I_{OUT_RTCLDO}=0mA, T_J=25°C	2.475	2.5	2.525	V
		I_{OUT_RTCLDO}=0mA, T_J= -40 ~ 125°C	2.45	2.5	2.55	V
	RTCLDO Output Voltage Accuracy (V_{RTCLDO}=3.3V)	I_{OUT_RTCLDO}=0mA, T_J=25°C	3.267	3.3	3.333	V
		I_{OUT_RTCLDO}=0mA, T_J= -40 ~ 125°C	3.234	3.3	3.366	V
	Line Regulation	V_{SYS}=3.5V ~ 5.5V, I_{OUT_RTCLDO}=0mA, T_J=25°C	-0.2	-	0.2	%
	Load Regulation	V_{SYS}=5V, I_{OUT_RTCLDO}=0mA ~ 10mA	-3	-	3	%
V_{DROP_RTC}	VSYS to RTCLDO Dropout Voltage (V_{RTCLDO}=3.3V)	V_{SYS}=3V, I_{OUT_RTCLDO}=10mA, T_J=25°C	-	105	120	mV
		V_{SYS}=3V, I_{OUT_RTCLDO}=10mA, T_J= -40 ~ 125°C	-	-	150	mV
I_{RTC_CL}	Short-Circuit Current Limit	V_{SYS}=2.5V ~ 5.5V, RTCLDO Short to GND	-	100	-	mA

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LS1_EN, LS2_EN**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
	VSYS Consumption Current		-	115	170	μA
LS1_EN						
V_{LDO_LS1}	Internal LDO Voltage	Selectable by VLS1/2_EN_SET[0] in PMIC_CFG_0 register, VLS1/2_EN_SET[0]=1, Supply source from VSYS, No Load	3.234	3.3	3.366	V
V_{LDO_LS1}	Internal LDO Voltage	Default voltage by MTP setting, VLS1/2_EN_SET[0]=0, Supply source from VSYS, No Load	1.764	1.8	1.836	V
R_{LDO_LS1}	Internal LDO ON Resistor	VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, Source 5mA	-	35	-	Ω
	Short Circuit Current Limit	VLS1/2_EN_SET[0]=1, VLS1_EN Short to GND	-	50	-	mA
V_{LS1_H}	LS1_EN Pull High Voltage	VLS1/2_EN_SET[0]=1, Source 5mA, Supply source is the internal LDO output VLDO_LS1	2.97	3.3	3.63	V
	LS1_EN Pull High Voltage	VLS1/2_EN_SET[0]=0, Source 3mA, Supply source is the internal LDO output VLDO_LS1	1.62	1.8	1.818	V
R_{LS1_SOURCE}	LS1_EN Output Source Capability	VLS1_EN=3.3V, Source 5mA	-	15	-	Ω
		VLS1_EN=1.8V, Source 5mA	-	30	-	Ω
	VSYS to LS1_EN Dropout Voltage	VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, I_{LS1_EN}=5mA, T_J=25°C	-	250	275	mV
		VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, I_{LS1_EN}=5mA, T_J= -40 ~ 125°C	-	-	360	mV
	Input Resistance	VSYS < VSYS Falling POR Threshold	-	10	-	kΩ
LS2_EN						
V_{LDO_LS2}	Internal LDO Voltage	Selectable by VLS1/2_EN_SET[0] in PMIC_CFG_0 register, VLS1/2_EN_SET[0]=1, Supply source from VSYS, No Load	3.234	3.3	3.366	V
V_{LDO_LS2}	Internal LDO Voltage	Default voltage by MTP setting, VLS1/2_EN_SET[0]=0, Supply source from VSYS, No Load	1.764	1.8	1.836	V
R_{LDO_LS2}	Internal LDO ON Resistor	VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, Source 5mA	-	27	-	Ω
	Short Circuit Current Limit	VLS1/2_EN_SET[0]=1, VLS2_EN Short to GND	-	60	-	mA
V_{LS2_H}	LS2_EN Pull High Voltage	VLS1/2_EN_SET[0]=1, Source 5mA, Supply source is the internal LDO output VLDO_LS2	2.97	3.3	3.63	V
	LS2_EN Pull High Voltage	VLS1/2_EN_SET[0]=0, Source 3mA, Supply source is the internal LDO output VLDO_LS2	1.62	1.8	1.818	V
R_{LS2_SOURCE}	LS2_EN Output Source Capability	VLS2_EN=3.3V, Source 5mA	-	15	-	Ω
		VLS2_EN=1.8V, Source 5mA	-	30	-	Ω
	VSYS to LS2_EN Dropout Voltage	VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, I_{LS2_EN}=5mA, T_J=25°C	-	210	230	mV
		VLS1/2_EN_SET[0]=1, V_{SYS}=3.2V, I_{LS2_EN}=5mA, T_J= -40 ~ 125°C	-	-	300	mV
	Input Resistance	VSYS < VSYS Falling POR Threshold	-	10	-	kΩ

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO2**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VSYS Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, No Load	-	40	65	μA
	VINLDO2 Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, V_{LDO2}=3.3V, No Load	-	35	55	μA
	VINLDO2 Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, V_{LDO2}=1.8V, No Load	-	30	50	μA
	VSYS Shutdown Current	In Shutdown Mode	-	-	1	μA
	VINLDO2 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
V_{LDO2}	Output Voltage	Default voltage by MTP setting	-	3.3	-	V
		LDO2 voltage set by LDO2SEL pin, VLDO2SEL=L	-	3.3	-	V
		LDO2 voltage set by LDO2SEL pin, VLDO2SEL=H	-	1.8	-	V
	Output Voltage Change Step		-	50	-	mV
	Output Voltage Change Rising Slew Rate	C_{LDO2}=2.2μF	-	1	-	mV/μs
	Output Discharge Resistor	In Shutdown Mode	-	100	-	Ω
	Output Voltage Accuracy	I_{LDO2}=0mA, T_J=25°C	-0.8	-	0.8	%
		I_{LDO2}=0mA, T_J= -40 ~ 125°C	-2	-	2	%
	Line Regulation	V_{SYS}=V_{INLDO2}=3.5V ~ 5.5V, I_{LDO2}=0mA, T_J=25°C	-0.2	-	0.2	%
	Load Regulation	V_{SYS}=V_{INLDO2}=5V, I_{LDO2}=0mA ~ 0.3A, T_J=25°C	-0.25	-	0.25	%
DROPOUT VOLTAGE						
V_{DROP}	VINLDO2 to VLDO2 Dropout Voltage	V_{LDO2}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO2}=0.3A, T_J=25°C	-	390	435	mV
		V_{LDO2}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO2}=0.3A, T_J= -40 ~ 125°C	-	-	565	mV
LDO2 ENABLE DELAY TIME						
	Enable Delay Time		-	360	-	μs
SOFT-START						
	Soft-Start Slew Rate		-	8	-	mV/μs
INTERNAL POWER GOOD INDICATOR						
	Internal PG_LDO2 in	Output Voltage Rising	85	90	95	%V_{REF}
	Internal PG_LDO2 Hysteresis		-	130	-	mV
	Internal PG_LDO2 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO2**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
PROTECTION						
	Current Limit Level	T_J=25°C	410	550	690	mA
		T_J= -40 ~ 125°C	350	-	-	mA
	Output Voltage UVP		45	50	55	%V_{REF}
	UVP Debounce Time	V_{LDO2} Falling (Note 4)	-	20	-	μs
	Output Voltgae OVP		118	123	128	%V_{REF}
	OVP Debounce Time	V_{LDO2} Rising (Note 4)	-	2	-	μs
PSRR						
	PSRR	Frequency=1kHz, I_{LDO2}=10mA (Note 4)	-	-60	-	dB

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO3**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VSYS Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, No Load	-	40	65	μA
	VINLDO2 Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, V_{LDO3}=3.3V, No Load	-	35	55	μA
	VINLDO2 Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, V_{LDO3}=1.8V, No Load	-	30	50	μA
	VSYS Shutdown Current	In Shutdown Mode	-	-	1	μA
	VINLDO2 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
V_{LDO3}	Output Voltage	Default voltage by MTP setting	-	3.3	-	V
		LDO3 voltage set by LDO3SEL pin, VLDO3SEL=L	-	3.3	-	V
		LDO3 voltage set by LDO3SEL pin, VLDO3SEL=H	-	1.8	-	V
	Output Voltage Change Step		-	50	-	mV
	Output Voltage Change Rising Slew Rate	C_{LDO3}=2.2μF	-	1	-	mV/μs
	Output Discharge Resistor	In Shutdown Mode	-	100	-	Ω
	Output Voltage Accuracy	I_{LDO3}=0mA, T_J=25°C	-0.8	-	0.8	%
		I_{LDO3}=0mA, T_J= -40 ~ 125°C	-2	-	2	%
	Line Regulation	V_{SYS}=V_{INLDO2}=3.5V ~ 5.5V, I_{LDO3}=0mA, T_J=25°C	-0.2	-	0.2	%
	Load Regulation	V_{SYS}=V_{INLDO2}=5V, I_{LDO3}=0 ~ 0.3A, T_J=25°C	-0.25	-	0.25	%
DROPOUT VOLTAGE						
V_{DROP}	VINLDO2 to VLDO3 Dropout Voltage	V_{LDO3}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO3}=0.3A, T_J=25°C	-	390	435	mV
		V_{LDO3}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO3}=0.3A, T_J= -40 ~ 125°C	-	-	565	mV
LDO3 ENABLE DELAY TIME						
	Enable Delay Time		-	360	-	μs
SOFT-START						
	Soft-Start Slew Rate		-	8	-	mV/μs
INTERNAL POWER GOOD INDICATOR						
	Internal PG_LDO3 in	Output Voltage Rising	85	90	95	%V_{REF}
	Internal PG_LDO3 Hysteresis		-	130	-	mV
	Internal PG_LDO3 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO3**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
PROTECTION						
	Current Limit Level	T_J=25°C	410	550	690	mA
		T_J= -40 ~ 125°C	350	-	-	mA
	Output Voltage UVP		45	50	55	%V_{REF}
	UVP Debounce Time	V_{LDO3} Falling (Note 4)	-	20	-	μs
	Output Voltgae OVP		118	123	128	%V_{REF}
	OVP Debounce Time	V_{LDO3} Rising (Note 4)	-	2	-	μs
PSRR						
	PSRR	Frequency=1kHz, I_{LDO3}=10mA (Note 4)	-	-60	-	dB

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO4**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VSYS Consumption Current	V_{SYS}=5V, V_{INLDO1}=1.8V, No Load	-	100	160	μA
	VINLDO1 Consumption Current	V_{SYS}=5V, V_{INLDO1}=1.8V, V_{LDO4}=1.2V, No Load	-	10	20	μA
	VSYS Shutdown Current	In Shutdown Mode	-	-	1	μA
	VINLDO1 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
V_{LDO4}	Output Voltage	Default voltage by MTP setting	-	1.2	-	V
	Output Voltage Change Step		-	10	-	mV
	Output Voltage Change Rising Slew Rate	C_{LDO4}=2.2μF	-	1	-	mV/μs
	Output Discharge Resistor	In Shutdown Mode	-	100	-	Ω
	Output Voltage Accuracy	I_{LDO4}=0mA, T_J=25°C	-0.8	-	0.8	%
		I_{LDO4}=0mA, T_J= -40 ~ 125°C	-2	-	2	%
	VINLDO1 Line Regulation	V_{INLDO1}=1.25V ~ 5.5V, I_{LDO4}=0mA, T_J=25°C	-0.15	-	0.15	%
	VSYS Line Regulation	V_{SYS}=3.5V ~ 5.5V, I_{LDO4}=0mA, T_J=25°C	-0.2	-	0.4	%
	Load Regulation	V_{SYS}=5V, V_{INLDO1}=1.8V, I_{LDO4}=0 ~ 200mA, T_J=25°C	-0.3	-	0.3	%
DROPOUT VOLTAGE						
V_{DROP}	VINLDO1 to VLDO4 Dropout Voltage	V_{SYS}=3.2V, V_{INLDO1}=1.2V, V_{LDO4}=1.2V, I_{LDO4}=200mA, T_J=25°C	-	330	360	mV
		V_{SYS}=3.2V, V_{INLDO1}=1.2V, V_{LDO4}=1.2V, I_{LDO4}=200mA, T_J= -40 ~ 125°C	-	-	470	mV
		V_{SYS}=5V, V_{INLDO1}=1.2V, V_{LDO4}=1.2V, I_{LDO4}=200mA, T_J=25°C	-	285	315	mV
		V_{SYS}=5V, V_{INLDO1}=1.2V, V_{LDO4}=1.2V, I_{LDO4}=200mA, T_J= -40 ~ 125°C	-	-	410	mV
LDO4 ENABLE DELAY TIME						
	Enable Delay Time		-	360	-	μs
SOFT-START						
	Soft-Start Slew Rate		-	8	-	mV/μs
INTERNAL POWER GOOD INDICATOR						
	Internal PG_LDO4 in	Output Voltage Rising	85	90	95	%V_{REF}
	Internal PG_LDO4 Hysteresis		-	50	-	mV
	Internal PG_LDO4 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO4**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
PROTECTION						
	Current Limit Level	T_J=25°C	350	475	600	mA
		T_J= -40 ~ 125°C	300	-	-	mA
	Output Voltage UVP		45	50	55	%V_{REF}
	UVP Debounce Time	V_{LDO4} Falling (Note 4)	-	20	-	μs
	Output Voltgae OVP		120	125	130	%V_{REF}
	OVP Debounce Time	V_{LDO4} Rising (Note 4)	-	2	-	μs
PSRR						
	PSRR	Frequency=1kHz, I_{LDO4}=10mA (Note 4)	-	-50	-	dB

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO5**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VSYS Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, No Load	-	40	65	μA
	VINLDO2 Consumption Current	V_{SYS}=5V, V_{INLDO2}=5V, V_{LDO5}=1.8V, No Load	-	30	50	μA
	VSYS Shutdown Current	In Shutdown Mode	-	-	1	μA
	VINLDO2 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
V_{LDO5}	Output Voltage	Default voltage by MTP setting	-	1.8	-	V
	Output Voltage Change Step		-	50	-	mV
	Output Voltage Change Rising Slew Rate	C_{LDO5}=2.2μF	-	1	-	mV/μs
	Output Discharge Resistor	In Shutdown Mode	-	100	-	Ω
	Output Voltage Accuracy	I_{LDO5}=0mA, T_J=25°C	-0.8	-	0.8	%
		I_{LDO5}=0mA, T_J= -40 ~ 125°C	-2	-	2	%
	Line Regulation	V_{SYS}=V_{INLDO2}=3.5V ~ 5.5V, I_{LDO5}=0mA, T_J=25°C	-0.2	-	0.2	%
	Load Regulation	V_{SYS}=V_{INLDO2}=5V, I_{LDO5}=0 ~ 150mA, T_J=25°C	-0.2	-	0.2	%
DROPOUT VOLTAGE						
V_{DROP}	VINLDO2 to VLDO5 Dropout Voltage	V_{LDO5}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO5}=150mA, T_J=25°C	-	195	215	mV
		V_{LDO5}=3.3V, V_{SYS}=3.2V, V_{INLDO2}=3.2V, I_{LDO5}=150mA, T_J= -40 ~ 125°C	-	-	280	mV
LDO5 ENABLE DELAY TIME						
	Enable Delay Time		-	360	-	μs
SOFT-START						
	Soft-Start Slew Rate		-	8	-	mV/μs
INTERNAL POWER GOOD INDICATOR						
	Internal PG_LDO5 in	Output Voltage Rising	85	90	95	%V_{REF}
	Internal PG_LDO5 Hysteresis		-	130	-	mV
	Internal PG_LDO5 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO5**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
PROTECTION						
	Current Limit Level	T_J=25°C	210	280	350	mA
		T_J= -40 ~ 125°C	175	-	-	mA
	Output Voltage UVP		45	50	55	%V_{REF}
	UVP Debounce Time	V_{LDO5} Falling (Note 4)	-	20	-	μs
	Output Voltgae OVP		118	123	128	%V_{REF}
	OVP Debounce Time	V_{LDO5} Rising (Note 4)	-	2	-	μs
PSRR						
	PSRR	Frequency=1kHz, I_{LDO5}=10mA (Note 4)	-	-60	-	dB

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO6**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VSYS Consumption Current	V_{SYS}=5V, V_{INLDO1}=1.8V, No Load	-	100	160	μA
	VINLDO1 Consumption Current	V_{SYS}=5V, V_{INLDO1}=1.8V, V_{LDO6}=0.8V, No Load	-	5	20	μA
	VSYS Shutdown Current	In Shutdown Mode	-	-	1	μA
	VINLDO1 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
V_{LDO6}	Output Voltage	Default voltage by MTP setting	-	0.8	-	V
	Output Voltage Change Step		-	10	-	mV
	Output Voltage Change Rising Slew Rate	C_{LDO6}=2.2μF	-	1	-	mV/μs
	Output Discharge Resistor	In Shutdown Mode	-	100	-	Ω
	Output Voltage Accuracy	I_{LDO6}=0mA, T_J=25°C	-0.8	-	0.8	%
		I_{LDO6}=0mA, T_J= -40 ~ 125°C	-2	-	2	%
	VINLDO1 Line Regulation	V_{INLDO1}=1.25V ~ 5.5V, I_{LDO6}=0mA, T_J=25°C	-0.15	-	0.15	%
	VSYS Line Regulation	V_{SYS}=3.5V ~ 5.5V, I_{LDO6}=0mA, T_J=25°C	-0.2	-	0.4	%
	Load Regulation	V_{SYS}=5V, V_{INLDO1}=1.8V, I_{LDO6}=0 ~ 300mA, T_J=25°C	-0.3	-	0.3	%
DROPOUT VOLTAGE						
V_{DROP}	VINLDO1 to VLDO6 Dropout Voltage	V_{SYS}=3.2V, V_{INLDO1}=1.2V, V_{LDO6}=1V, I_{LDO6}=300mA, T_J=25°C	-	500	550	mV
		V_{SYS}=3.2V, V_{INLDO1}=1.2V, V_{LDO6}=1V, I_{LDO6}=300mA, T_J= -40 ~ 125°C	-	-	715	mV
		V_{SYS}=5V, V_{INLDO1}=1.2V, V_{LDO6}=1V, I_{LDO6}=300mA, T_J=25°C	-	440	485	mV
		V_{SYS}=5V, V_{INLDO1}=1.2V, V_{LDO6}=1V, I_{LDO6}=300mA, T_J= -40 ~ 125°C	-	-	630	mV
LDO6 ENABLE DELAY TIME						
	Enable Delay Time		-	360	-	μs
SOFT-START						
	Soft-Start Slew Rate		-	8	-	mV/μs
INTERNAL POWER GOOD INDICATOR						
	Internal PG_LDO6 in	Output Voltage Rising	85	90	95	%V_{REF}
	Internal PG_LDO6 Hysteresis		-	50	-	mV
	Internal PG_LDO6 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **LDO6**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
PROTECTION						
	Current Limit Level	T_J=25°C	600	750	900	mA
		T_J= -40 ~ 125°C	500	-	-	mA
	Output Voltage UVP		45	50	55	%V_{REF}
	UVP Debounce Time	V_{LDO6} Falling (Note 4)	-	20	-	μs
	Output Voltgae OVP		120	125	130	%V_{REF}
	OVP Debounce Time	V_{LDO6} Rising (Note 4)	-	2	-	μs
PSRR						
	PSRR	Frequency=1kHz, I_{LDO6}=10mA (Note 4)	-	-50	-	dB

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK1, 3**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current in Single-Phase Mode	BUCK1 and BUCK3 are enabled in single-phase PFM mode and all LX will not switch	-	45	80	μA
	Consumption Current in Dual-Phase Mode	BUCK1 and BUCK3 are enabled in dual-phase PFM mode and all LX will not switch	-	300	470	μA
	VIN1, 3 Shutdown Current	In Shutdown Mode	-	-	1	μA
OUTPUT VOLTAGE						
$V_{DC1,3}$	Output Voltage	Default voltage (Selectable by MTP setting)	-	0.75	-	V
	Output Voltage Change Step		-	3.75	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation (Single-Phase)	In CCM, $I_{DC1,3}$=0A ~ 6A (Note 4)	-0.3	-	0.3	%
	Load Regulation (Dual-Phase)	In CCM, I_{DC1}=0A ~ 12A (Note 4)	-0.5	-	0.5	%
	FB1 Input Resistance		-	150	-	kΩ
	FB3 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	750	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	120	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK1, 3**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
BUCK1 POWER MOSFET						
$R_{DS(ON)\_HS1}$	High-Side MOSFET ON Resistance	I_{DC1}=1A, T_J=25°C	-	15.5	17	mΩ
		I_{DC1}=1A, T_J= -40 ~ 125°C	-	-	22	mΩ
$R_{DS(ON)\_LS1}$	Low-Side MOSFET ON Resistance	I_{DC1}=1A, T_J=25°C	-	9.5	10.5	mΩ
		I_{DC1}=1A, T_J= -40 ~ 125°C	-	-	14	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN1}=5.5V, V_{LX1}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX1}=5.5V, V_{SYS}=V_{IN1}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	V_{SYS}=V_{IN1}=5V, I_{DC1}=6A, V_{LX1} rising (Note 4)	-	10	-	ns
	Dead Time	V_{SYS}=V_{IN1}=5V, I_{DC1}=6A, V_{LX1} falling (Note 4)	-	10	-	ns
BUCK3 POWER MOSFET						
$R_{DS(ON)\_HS3}$	High-Side MOSFET ON Resistance	I_{DC3}=1A, T_J=25°C	-	15.5	17	mΩ
		I_{DC3}=1A, T_J= -40 ~ 125°C	-	-	22	mΩ
$R_{DS(ON)\_LS3}$	Low-Side MOSFET ON Resistance	I_{DC3}=1A, T_J=25°C	-	9.5	10.5	mΩ
		I_{DC3}=1A, T_J= -40 ~ 125°C	-	-	14	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN3}=5.5V, V_{LX3}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX3}=5.5V, V_{SYS}=V_{IN3}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	V_{SYS}=V_{IN3}=5V, I_{DC3}=6A, V_{LX3} rising (Note 4)	-	10	-	ns
	Dead Time	V_{SYS}=V_{IN3}=5V, I_{DC3}=6A, V_{LX3} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC1}	Zero Cross Comparator Offset	V_{GND} - V_{LX1}	-5	0	5	mV
V_{ZC3}	Zero Cross Comparator Offset	V_{GND} - V_{LX3}	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC1, 3	Output Voltage Rising	82.5	87.5	92.5	%V_{REF}
	Internal PG_DC1, 3 Hysteresis		-	30	-	mV
	Internal PG_DC1, 3 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	LS OCP Level	T_J=25°C	6.38	7.5	8.62	A
		T_J= -40 ~ 125°C	5.75	-	-	A
	Output Voltage UVP		70	75	80	%V_{REF}
	UVP Debounce Time	$V_{FB1,3}$ Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		115	120	125	%V_{REF}
	OVP Debounce Time	$V_{FB1,3}$ Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK2**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current	In PFM mode, only BUCK2 is enabled, and LX2 does not switch	-	45	80	μA
	VIN2 Shutdown Current	In Shutdown Mode, V_{SYS}=V_{IN2}=5V	-	-	1	μA
OUTPUT VOLTAGE						
V_{DC2}	Output Voltage	Default voltage (Selectable by MTP setting)	-	1.8	-	V
	Output Voltage Change Step		-	10	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation	In CCM, V_{DC2}=1.8V, I_{DC2}=0A ~ 2A (Note 4)	-0.3	-	0.3	%
	FB2 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	1000	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	85	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK2**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
$R_{DS(ON)\_HS2}$	High-Side MOSFET ON Resistance	I_{DC2}=1A, T_J=25°C	-	28.5	31.5	mΩ
		I_{DC2}=1A, T_J= -40 ~ 125°C	-	-	41	mΩ
$R_{DS(ON)\_LS2}$	Low-Side MOSFET ON Resistance	I_{DC2}=1A, T_J=25°C	-	17.5	19.5	mΩ
		I_{DC2}=1A, T_J= -40 ~ 125°C	-	-	25.5	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN2}=5.5V, V_{LX2}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX2}=5.5V, V_{SYS}=V_{IN2}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	I_{DC2}=2A, V_{LX2} rising (Note 4)	-	10	-	ns
	Dead Time	I_{DC2}=2A, V_{LX2} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC2}	Zero Cross Comparator Offset	V_{GND} - V_{LX2} Voltage	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC2	Output Voltage Rising	87.5	92.5	97.5	%V_{REF}
	Internal PG_DC2 Hysteresis		-	60	-	mV
	Internal PG_DC2 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	HS OCP Level	T_J=25°C	3.4	4	4.6	A
		T_J= -40 ~ 125°C	3.1	-	-	A
	LS OCP Level	T_J=25°C	2.55	3	3.45	A
		T_J= -40 ~ 125°C	2.3	-	-	A
	Output Voltage UVP		60	65	70	%V_{REF}
	UVP Debounce Time	V_{FB2} Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		107.5	112.5	117.5	%V_{REF}
	OVP Debounce Time	V_{FB2} Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK4**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current	In PFM mode, only BUCK4 is enabled, and LX4 does not switch	-	45	80	μA
	VIN4 Shutdown Current	In Shutdown Mode, V_{SYS}=V_{IN4}=5V	-	-	1	μA
OUTPUT VOLTAGE						
V_{DC4}	Output Voltage	Default voltage (Selectable by MTP setting)	-	1.05	-	V
	Output Voltage Change Step		-	5	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation	In CCM, V_{DC4}=1.05V, I_{DC4}=0A ~ 3A (Note 4)	-0.3	-	0.3	%
	FB4 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	1000	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	100	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK4**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
$R_{DS(ON)\_HS4}$	High-Side MOSFET ON Resistance	I_{DC4}=1A, T_J=25°C	-	28.5	31.5	mΩ
		I_{DC4}=1A, T_J= -40 ~ 125°C	-	-	41	mΩ
$R_{DS(ON)\_LS4}$	Low-Side MOSFET ON Resistance	I_{DC4}=1A, T_J=25°C	-	17.5	19.5	mΩ
		I_{DC4}=1A, T_J= -40 ~ 125°C	-	-	25.5	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN4}=5.5V, V_{LX4}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX4}=5.5V, V_{SYS}=V_{IN4}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	I_{DC4}=3A, V_{LX4} rising (Note 4)	-	10	-	ns
	Dead Time	I_{DC4}=3A, V_{LX4} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC4}	Zero Cross Comparator Offset	V_{GND} - V_{LX4} Voltage	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC4 in	Output Voltage Rising	87.5	92.5	97.5	%V_{REF}
	Internal PG_DC4 Hysteresis		-	30	-	mV
	Internal PG_DC4 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	LS OCP Level	T_J=25°C	3.4	4	4.6	A
		T_J= -40 ~ 125°C	3.1	-	-	A
	Output Voltage UVP		60	65	70	%V_{REF}
	UVP Debounce Time	V_{FB4} Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		107.5	112.5	117.5	%V_{REF}
	OVP Debounce Time	V_{FB4} Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK5**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current	In PFM mode, only BUCK5 is enabled, and LX5 does not switch	-	45	80	μA
	VIN5 Shutdown Current	In Shutdown Mode, V_{SYS}=V_{IN5}=5V	-	-	1	μA
OUTPUT VOLTAGE						
V_{DC5}	Output Voltage	Default voltage (Selectable by MTP setting)	-	0.55125	-	V
	Output Voltage Change Step		-	3.75	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, V_{DC5}< 0.5V, T_J=25°C	-3	-	3	mV
		Operate in PWM mode, V_{DC5}< 0.5V, T_J= -40 ~ 125°C	-8	-	8	mV
		Operate in PWM mode, V_{DC5} ≥ 0.5V, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, V_{DC5} ≥ 0.5V, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation	In CCM, V_{DC5}=1.05V, I_{DC5}=0A ~ 3A (Note 4)	-0.3	-	0.3	%
	FB5 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	1000	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	100	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK5**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
$R_{DS(ON)\_HS5}$	High-Side MOSFET ON Resistance	I_{DC5}=1A, T_J=25°C	-	26.5	29.5	mΩ
		I_{DC5}=1A, T_J= -40 ~ 125°C	-	-	38.5	mΩ
$R_{DS(ON)\_LS5}$	Low-Side MOSFET ON Resistance	I_{DC5}=1A, T_J=25°C	-	17.5	19.5	mΩ
		I_{DC5}=1A, T_J= -40 ~ 125°C	-	-	25.5	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN5}=5.5V, V_{LX5}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX5}=5.5V, V_{SYS}=V_{IN5}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	I_{DC5}=3A, V_{LX5} rising (Note 4)	-	10	-	ns
	Dead Time	I_{DC5}=3A, V_{LX5} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC5}	Zero Cross Comparator Offset	V_{GND} - V_{LX5} Voltage	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC5	Output Voltage Rising	82.5	87.5	92.5	%V_{REF}
	Internal PG_DC5 Hysteresis		-	30	-	mV
	Internal PG_DC5 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	LS OCP Level	T_J=25°C	3.4	4	4.6	A
		T_J= -40 ~ 125°C	3.1	-	-	A
	Output Voltage UVP		70	75	80	%V_{REF}
	UVP Debounce Time	V_{FB5} Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		115	120	125	%V_{REF}
	OVP Debounce Time	V_{FB5} Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK6**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current	In PFM mode, only BUCK6 is enabled, and LX6 does not switch	-	45	80	μA
	VIN6 Shutdown Current	In Shutdown Mode, V_{SYS}=V_{IN6}=5V	-	-	1	μA
OUTPUT VOLTAGE						
V_{DC6}	Output Voltage	Default voltage (Selectable by MTP setting)	-	3.3	-	V
	Output Voltage Change Step		-	10	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation	In CCM, V_{DC6}=3.3V, I_{DC6}=0A ~ 2A (Note 4)	-0.3	-	0.3	%
	FB6 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	1000	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	85	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK6**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
$R_{DS(ON)\_HS6}$	High-Side MOSFET ON Resistance	I_{DC6}=1A, T_J=25°C	-	27	30	mΩ
		I_{DC6}=1A, T_J= -40 ~ 125°C	-	-	39	mΩ
$R_{DS(ON)\_LS6}$	Low-Side MOSFET ON Resistance	I_{DC6}=1A, T_J=25°C	-	17.5	19.5	mΩ
		I_{DC6}=1A, T_J= -40 ~ 125°C	-	-	25.5	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN6}=5.5V, V_{LX6}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX6}=5.5V, V_{SYS}=V_{IN6}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	I_{DC6}=2A, V_{LX6} rising (Note 4)	-	10	-	ns
	Dead Time	I_{DC6}=2A, V_{LX6} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC6}	Zero Cross Comparator Offset	V_{GND} - V_{LX6} Voltage	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC6	Output Voltage Rising	87.5	92.5	97.5	%V_{REF}
	Internal PG_DC6 Hysteresis		-	60	-	mV
	Internal PG_DC6 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	HS OCP Level	T_J=25°C	3.4	4	4.6	A
		T_J= -40 ~ 125°C	3.1	-	-	A
	LS OCP Level	T_J=25°C	2.55	3	3.45	A
		T_J= -40 ~ 125°C	2.3	-	-	A
	Output Voltage UVP		60	65	70	%V_{REF}
	UVP Debounce Time	V_{FB6} Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		107.5	112.5	117.5	%V_{REF}
	OVP Debounce Time	V_{FB6} Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK7**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	Consumption Current	In PFM mode, only BUCK7 is enabled, and LX7 does not switch	-	45	80	μA
	VIN7 Shutdown Current	In Shutdown Mode, V_{SYS}=V_{IN7}=5V	-	-	1	μA
OUTPUT VOLTAGE						
V_{DC7}	Output Voltage	Default voltage (Selectable by MTP setting)	-	1.8	-	V
	Output Voltage Change Step		-	10	-	mV
	Output Voltage Change Slew Rate		-	1	-	mV/μs
	Output Voltage Accuracy	Operate in PWM mode, T_J=25°C	-0.6	-	0.6	%
		Operate in PWM mode, T_J= -40 ~ 125°C	-1.5	-	1.5	%
	Line Regulation	In CCM, V_{SYS}=3.5V ~ 5.5V	-0.5	-	0.5	%
	Load Regulation	In CCM, V_{DC7}=1.8V, I_{DC7}=0A ~ 2A (Note 4)	-0.3	-	0.3	%
	FB7 Input Resistance		-	150	-	kΩ
PWM FREQUENCY SETTING						
fsw	Switching Frequency	Default setting	-	1000	-	kHz
	Switching Frequency Tolerance		-10	-	10	%
t_{ON_MIN}	Minimum On Time	(Note 4)	-	50	-	ns
t_{OFF_MIN}	Minimum Off Time	(Note 4)	-	85	-	ns
ENABLE DELAY TIME						
	Enable Delay Time		-	250	-	μs
OUTPUT RAMP UP						
	Ramp Up Time Setting Range	Selectable by MTP setting: t_{RU}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RU}	Ramp Up Time	T_J=25°C	0.9xt_{RU}	-	1.1xt_{RU}	ms
	Ramp Up Time	T_J= -40 ~ 125°C	0.8xt_{RU}	-	1.2xt_{RU}	ms
OUTPUT RAMP DOWN or OUTPUT DISCHARGE (Selectable by MTP setting)						
	Ramp Down Time Setting Range	Selectable by MTP setting: t_{RD}=0.5ms, 1ms, 1.5ms, 2ms (Typical)	0.5	-	2	ms
t_{RD}	Ramp Down Time	T_J=25°C	0.9xt_{RD}	-	1.1xt_{RD}	ms
	Ramp Down Time	T_J= -40 ~ 125°C	0.8xt_{RD}	-	1.2xt_{RD}	ms
	Output Discharge Resistor (Optional)		-	100	-	Ω

Note 4: Guarantee by design, not production test.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{SYS}=5V=V_{INX}, V_{INLDO2}=5V, V_{INLDO1}=1.8V, V_{EN}=5V and T_A= -40 to 105°C. Typical values are at T_J=25°C.

- **BUCK7**

Symbol	Parameter	Test Condition	APW7720			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
$R_{DS(ON)\_HS7}$	High-Side MOSFET ON Resistance	I_{DC7}=1A, T_J=25°C	-	27	30	mΩ
		I_{DC7}=1A, T_J= -40 ~ 125°C	-	-	39	mΩ
$R_{DS(ON)\_LS7}$	Low-Side MOSFET ON Resistance	I_{DC7}=1A, T_J=25°C	-	17.5	19.5	mΩ
		I_{DC7}=1A, T_J= -40 ~ 125°C	-	-	25.5	mΩ
	High Side Mos Leakage Current	V_{SYS}=V_{IN7}=5.5V, V_{LX7}=0V, T_J=25°C	-	-	1	μA
	Low Side Mos Leakage Current	V_{LX7}=5.5V, V_{SYS}=V_{IN7}=5.5V, No Shutdown, No Switching, T_J=25°C	-	-	1	μA
	Dead Time	I_{DC7}=2A, V_{LX7} rising (Note 4)	-	10	-	ns
	Dead Time	I_{DC7}=2A, V_{LX7} falling (Note 4)	-	10	-	ns
ZERO CORSS DETECTION						
V_{ZC7}	Zero Cross Comparator Offset	V_{GND} - V_{LX7} Voltage	-5	0	5	mV
INTERNAL POWER GOOD INDICATOR						
	Internal PG_DC7	Output Voltage Rising	87.5	92.5	97.5	%V_{REF}
	Internal PG_DC7 Hysteresis		-	60	-	mV
	Internal PG_DC7 High to Low Debounce Time	95%V_{REF} to 80%V_{REF} (Note 4)	-	20	-	μs
PROTECTION						
	HS OCP Level	T_J=25°C	3.4	4	4.6	A
		T_J= -40 ~ 125°C	3.1	-	-	A
	LS OCP Level	T_J=25°C	2.55	3	3.45	A
		T_J= -40 ~ 125°C	2.3	-	-	A
	Output Voltage UVP		60	65	70	%V_{REF}
	UVP Debounce Time	V_{FB7} Falling (Note 4)	-	5	-	μs
	Output Voltgae OVP		107.5	112.5	117.5	%V_{REF}
	OVP Debounce Time	V_{FB7} Rising (Note 4)	-	3	-	μs

Note 4: Guarantee by design, not production test.

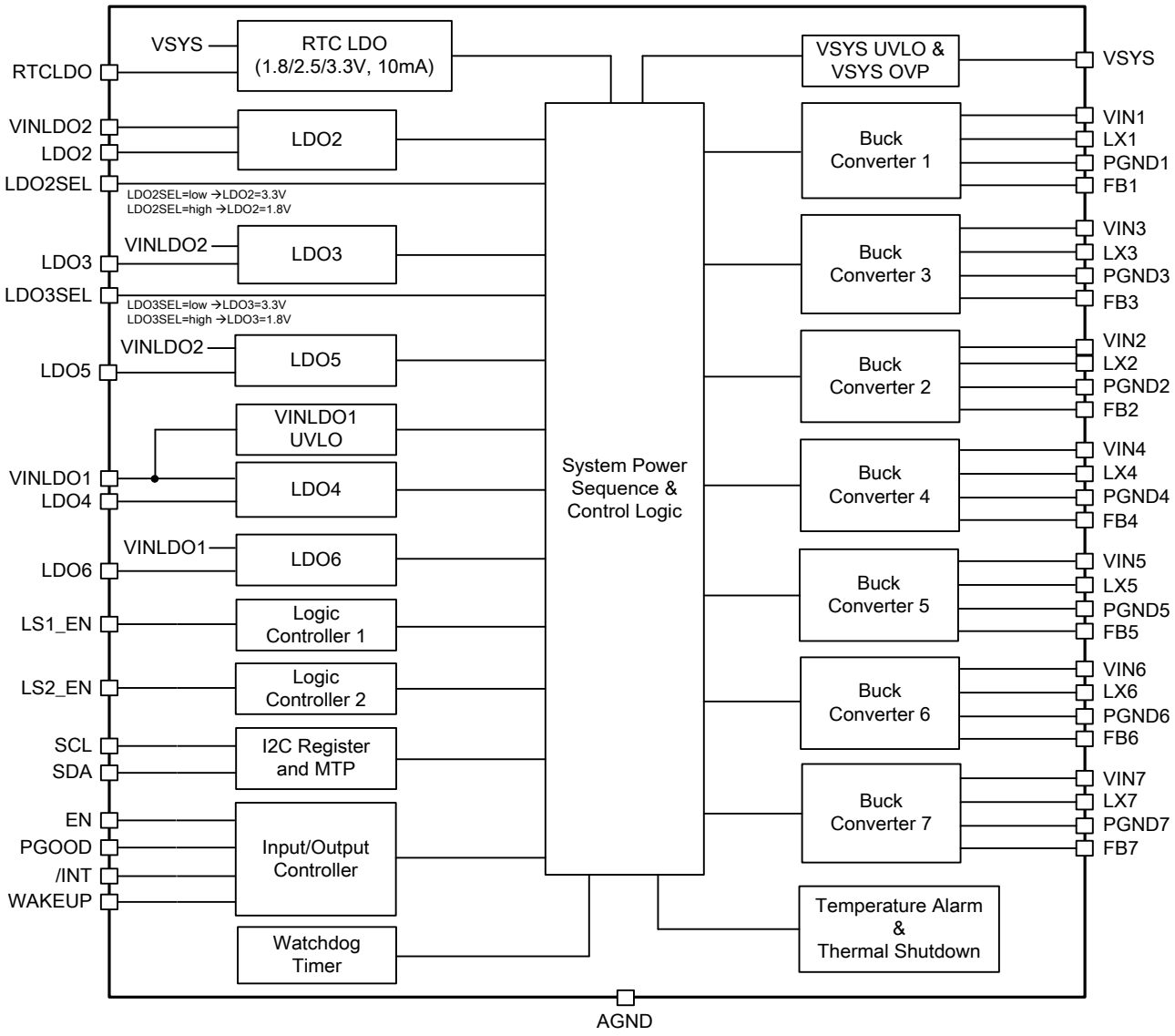
Pin Description

PIN		DESCRIPTION
NO.	NAME	
1, 14, 27, 40	NC	NC pins for improved solder joint reliability.
2	LS1_EN	Logic output pin for enable signal control.
3	FB4	BUCK4 output voltage feedback pin.
4	VIN4	BUCK4 PWM converter input pin. If BUCK4 is not used, VIN4 cannot be left floating and must be connected to the VSYS pin.
5	LX4	BUCK4 switch node. Connect to external inductor for output LC filter.
6	PGND4	Power ground for BUCK4.
7	PGND2	Power ground for BUCK2.
8	LX2	BUCK2 switch node. Connect to external inductor for output LC filter.
9	VIN2	BUCK2 PWM converter input pin. If BUCK2 is not used, VIN2 cannot be left floating and must be connected to the VSYS pin.
10	FB2	BUCK2 output voltage feedback pin.
11	/INT	The PMIC's active-low interrupt pin is an open-drain output and must be pulled up with a 10kΩ resistor.
12	LDO5	LDO5 output pin. The pin voltage is adjustable by I^2C.
13	LDO3	LDO3 output pin. The pin voltage can be adjusted via the LDO3SEL pin or I^2C.
15	LDO2	LDO2 output pin. The pin voltage can be adjusted via the LDO2SEL pin or I^2C.
16	VINLDO2	LDO2, 3, 5 input pin. If LDO2, LDO3, and LDO5 are not used, VINLDO2 cannot be left floating and must be connected to the VSYS pin.
17	FB6	BUCK6 output voltage feedback pin.
18	VIN6	BUCK6 PWM converter input pin. If BUCK6 is not used, VIN6 cannot be left floating and must be connected to the VSYS pin.
19	LX6	BUCK6 switch node. Connect to external inductor for output LC filter.
20	PGND6	Power ground for BUCK6.
21	PGND7	Power ground for BUCK7.
22	LX7	BUCK7 switch node. Connect to external inductor for output LC filter.
23	VIN7	BUCK7 PWM converter input pin. If BUCK7 is not used, VIN7 cannot be left floating and must be connected to the VSYS pin.
24	FB7	BUCK7 output voltage feedback pin.
25	VINLDO1	LDO4, 6 input pin.
26	LDO4	LDO4 output pin. The pin voltage is adjustable by I^2C.
28	LDO6	LDO6 output pin. The pin voltage is adjustable by I^2C.
29	LS2_EN	Logic output pin for enable signal control.
30	RTCLDO	RTCLDO output pin.
31	FB3	BUCK3 output voltage feedback pin.
32	VIN3	BUCK3 PWM converter input pin. If BUCK3 is not used, VIN3 cannot be left floating and must be connected to the VSYS pin.
33	LX3	BUCK3 switch node. Connect to external inductor for output LC filter.
34	PGND3	Power ground for BUCK3.
35	PGND1	Power ground for BUCK1.
36	LX1	BUCK1 switch node. Connect to external inductor for output LC filter.
37	VIN1	BUCK1 PWM converter input pin. If BUCK1 is not used, VIN1 cannot be left floating and must be connected to the VSYS pin.
38	FB1	BUCK1 output voltage feedback pin.
39	EN	PMIC enable pin.
41	PGOOD	Power Good Indicator. Pull low when either VR output is out of regulation.
42	SDA	I^2C interface data.
43	SCL	I^2C interface clock.
44	WAKEUP	When the device is in off mode (power-saving mode), sending a pulse signal to the WAKEUP pin for more than 500us will wake up the device and restart the power-up sequence.

Pin Description (Cont.)

PIN		DESCRIPTION
NO.	NAME	
45	VSYS	PMIC main power input pin.
46	AGND	Analog ground.
47	PGND5	Power ground for BUCK5.
48	LX5	BUCK5 switch node. Connect to external inductor for output LC filter.
49	VIN5	BUCK5 PWM converter input pin. If BUCK5 is not used, VIN5 cannot be left floating and must be connected to the VSYS pin.
50	FB5	BUCK5 output voltage feedback pin.
51	LDO3SEL	LDO3 output voltage 3.3V or 1.8V selection pin.
52	LDO2SEL	LDO2 output voltage 3.3V or 1.8V selection pin.

Block Diagram



Typical Application Circuit

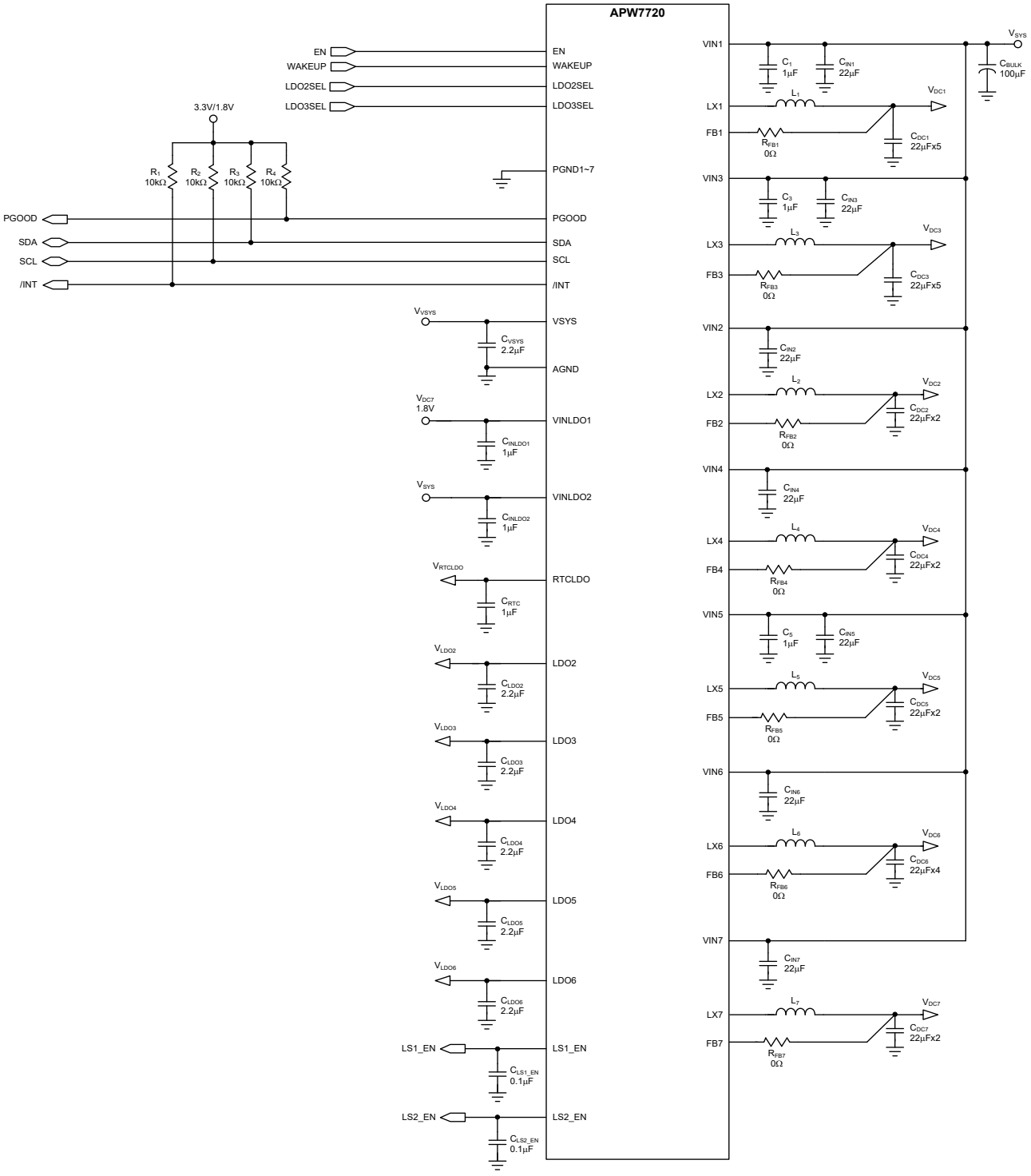


Figure 1. BUCK1, 3 for 1-Phase Active Configuration

Note 5: If any of BUCK1~7 is not used, any pin of VIN1~7 cannot be left floating and must be connected to the VSYS pin.

Typical Application Circuit (Cont.)

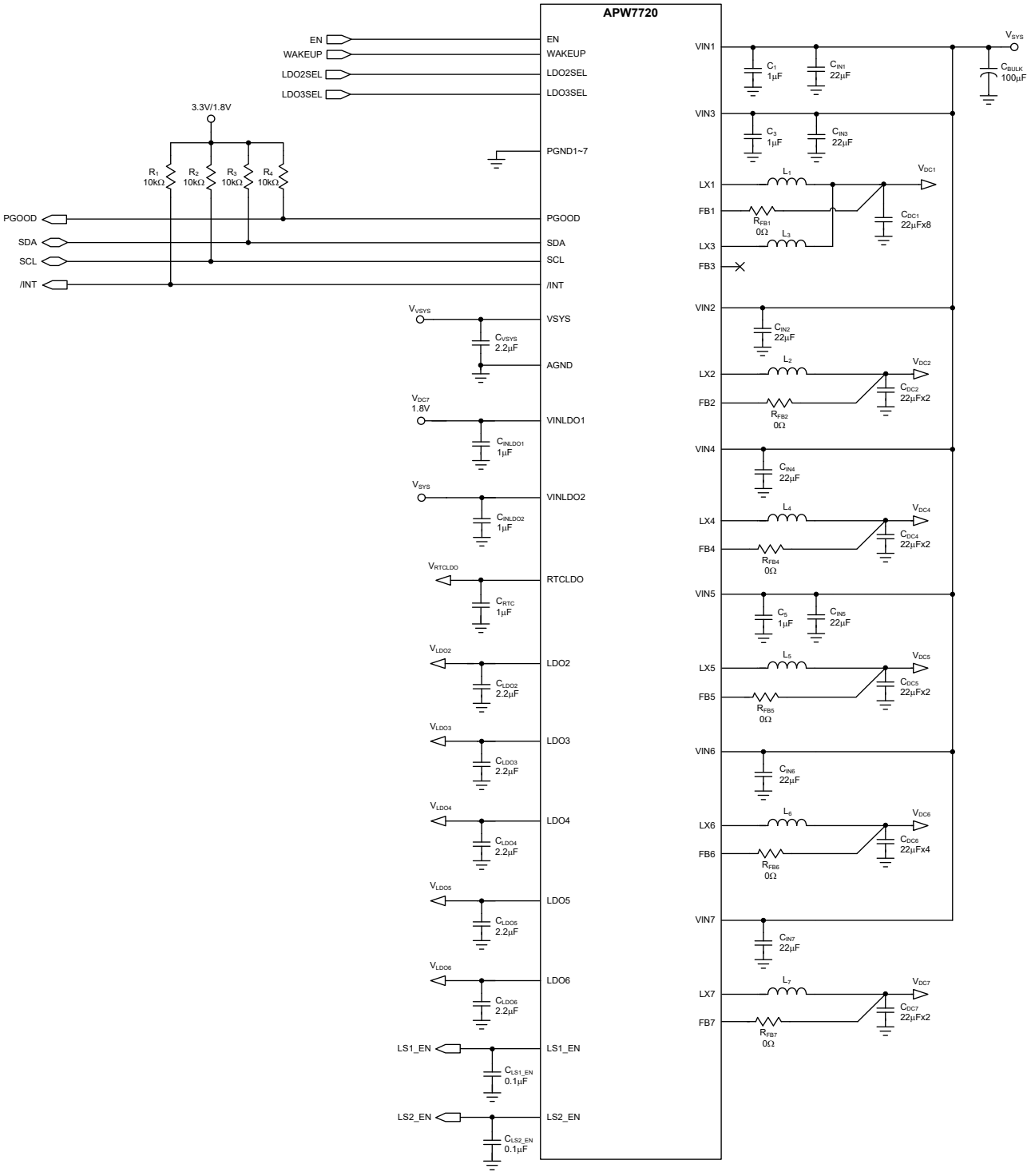


Figure 2. BUCK1, 3 for 2-Phase Active Configuration

Note 5: If any of BUCK1~7 is not used, any pin of VIN1~7 cannot be left floating and must be connected to the VSYS pin.

Typical Application Circuit (Cont.)

Table 1. APW7720-00/01/02/03/05 Operating Condition (V_{SYS}=5V)

Symbol	Parameter	BUCK1, 3	BUCK2	BUCK4	BUCK5	BUCK6	BUCK7
$V_{IN1~7}$	BUCKx Input Voltage	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}
$V_{DC1~7}$	BUCKx Output Voltage	0.75V	1.8V	1.05V	0.551V	3.3V	1.8V
f_{SW}	Switching Frequency	750kHz	1MHz	1MHz	1MHz	1MHz	1MHz
Symbol	**Parameter**	**RTCLDO**	**LDO2, 3**	**LDO4**	**LDO5**	**LDO6**	**LS1_EN, LS2_EN**
$V_{LDOIN1~2}$	LDOx Inputt Voltage	-	V_{SYS}	V_{DC7}	V_{SYS}	V_{DC7}	N/A
$V_{LDO2~6}$, V_{RTCLDO}	LDOx Output Voltage	1.8V	LDO2, 3_SEL=H, 1.8V LDO2, 3_SEL=L, 3.3V	1.2V	1.8V	0.8V	N/A
V_{LS1_EN}, V_{LS2_EN}	LSx_EN Pull High Voltage	N/A	N/A	N/A	N/A	N/A	1.8V

Table 2. APW7720-04 Operating Condition (V_{SYS}=5V)

Symbol	Parameter	BUCK1	BUCK3	BUCK2	BUCK4	BUCK5	BUCK6	BUCK7
$V_{IN1~7}$	BUCKx Input Voltage	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}
$V_{DC1~7}$	BUCKx Output Voltage	0.82V	0.82V	1.8V	1.1V	0.6V	3.3V	1.2V
f_{SW}	Switching Frequency	1MHz	1MHz	1MHz	1MHz	1MHz	1MHz	1MHz
Symbol	**Parameter**	**RTCLDO**	**LDO2**	**LDO3**	**LDO4**	**LDO5**	**LDO6**	**LS1_EN, LS2_EN**
$V_{LDOIN1~2}$	LDOx Inputt Voltage	-	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	V_{SYS}	N/A
$V_{LDO2~6}$, V_{RTCLDO}	LDOx Output Voltage	1.8V	1.8V	3.3V	1.2V	2.5V	0.6V	N/A
V_{LS1_EN}, V_{LS2_EN}	LSx_EN Pull High Voltage	N/A	N/A	N/A	N/A	N/A	N/A	1.8V

Table 3. APW7720-00/01/02/03/05 Reference BOM (V_{SYS}=5V)

Part	Value	Description	Part Number	Manufacturer
C_{SYS}, C_{LDO2}, C_{LDO3}, C_{LDO4}, C_{LDO5}, C_{LDO6}	2.2μF	Ceramic Cap., 10V, X7R	GRM188R71A225KE15J	Murata
$C_{IN1~7}$	22μF	Ceramic Cap., 10V, X7R	GRM21BZ71A226ME15L	Murata
C_1, C_3, C_5	1μF	Ceramic Cap., 10V, X6S	GRM033C81A105ME05D	Murata
$C_{DC1~7}$	22μF	Ceramic Cap., 6.3V, X6S	GRM21BC80J226ME51L	Murata
C_{INLDO1}, C_{INLDO2}, C_{RTC}	1μF	Ceramic Cap., 10V, X6S	GRM185C81A105KE36D	Murata
L_1, L_3	0.47μH	Inductor, Irms 18.4A (Typ.), Isat 26A (Typ.), DCR 4.13mΩ (Max.)	TUP0531W-R47M	3L Electronic
L_2, L_4, L_5, L_6, L_7	1μH	Inductor, Irms 4.5A (Typ.), Isat 7.6A (Typ.), DCR 24mΩ (Max.)	LHP322520-1R0M	3L Electronic
$R_{1~4}$	10kΩ	Film Res., 1%	-	-

Table 4. APW7720-00 Power-on Sequence (Supports self-refresh mode)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	Time Slot 3	Idle Time 3	Time Slot 4	Idle Time 4	Time Slot 5	Idle Time 5	Time Slot 6	Idle Time 6	Time Slot 7	Idle Time 7	PGOOD Delay Time
LDO5	10ms	BUCK4	10ms	BUCK5, BUCK7, LS1_EN	10ms	BUCK1+BUCK3 (2-phase), LS2_EN	10ms	LDO6	10ms	LDO4	10ms	BUCK2	10ms	BUCK6, LDO2, LDO3	0.2ms	10ms

Note 6: The power-off sequence is the reverse of the power-on sequence.

Typical Application Circuit (Cont.)

Table 5. APW7720-01 Power-on Sequence (No self-refresh mode supported) (Note 6)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	Time Slot 3	Idle Time 3	PGOOD Delay Time
BUCK1+ BUCK3 (2-Phase), LS2_EN	10ms	BUCK2, BUCK7, LDO5	10ms	BUCK4, BUCK5, LS1_EN, LDO4, LDO6	10ms	BUCK6, LDO2, LDO3	0.2ms	10ms

Table 6. APW7720-02 Power-on Sequence (No self-refresh mode supported) (Note 6)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	PGOOD Delay Time
BUCK1+ BUCK3 (2-Phase)	10ms	BUCK2, BUCK4, BUCK5, BUCK7, LDO4, LDO5, LDO6	10ms	BUCK6, LDO2, LDO3	0.2ms	10ms

Table 7. APW7720-03 Power-on Sequence (No self-refresh mode supported) (Note 6)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	Time Slot 3	Idle Time 3	Time Slot 4	Idle Time 4	PGOOD Delay Time
BUCK1+ BUCK3 (2-Phase)	10ms	BUCK2, BUCK7, LDO5	10ms	BUCK4	2ms	BUCK5, LDO4, LDO6	10ms	BUCK6, LDO2, LDO3	0.2ms	10ms

Table 8. APW7720-04 Power-on Sequence (Note 6)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	Time Slot 3	Idle Time 3	Time Slot 4	Idle Time 4	Time Slot 5	Idle Time 5	Time Slot 6	Idle Time 6	Time Slot 7	Idle Time 7	Time Slot 7	Idle Time 7	PGOOD Delay Time
BUCK1, BUCK3	0.2ms	BUCK2, LDO3, LDO4, LDO5	0.2ms	BUCK 7	0.2ms	LDO6	0.2ms	BUCK4, BUCK5	10ms	LS2_ EN	0.2ms	BUCK 6	0.2ms	LDO2	0.2ms	LS1_ EN	0.2ms	5ms

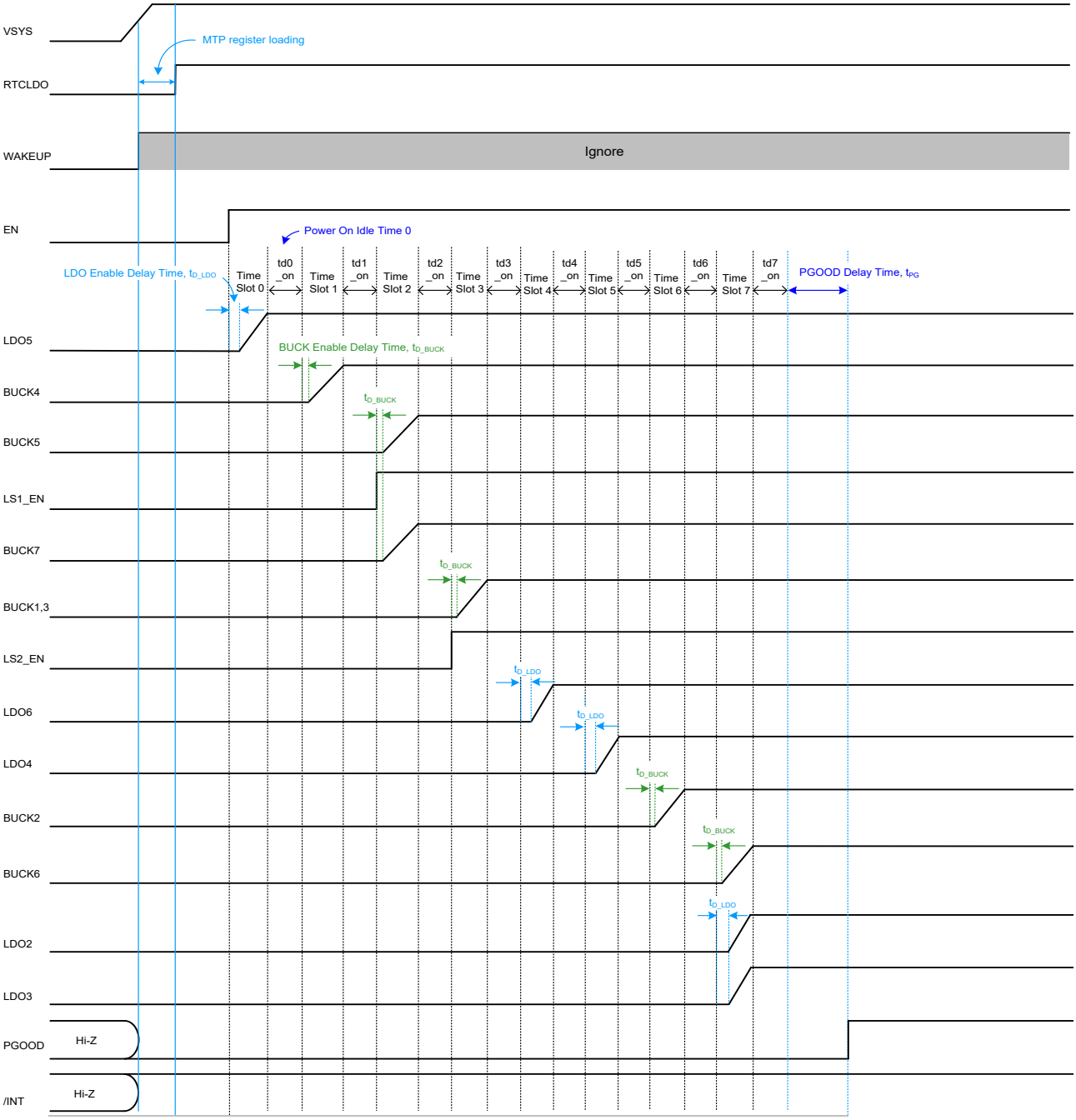
Table 9. APW7720-05 Power-on Sequence (No self-refresh mode supported) (Note 6)

Time Slot 0	Idle Time 0	Time Slot 1	Idle Time 1	Time Slot 2	Idle Time 2	Time Slot 3	Idle Time 3	Time Slot 4	Idle Time 4	PGOOD Delay Time
BUCK7	0.2ms	BUCK1+ BUCK3 (2-Phase), LDO6	10ms	LDO4, LDO5	10ms	BUCK2, BUCK4	10ms	BUCK5, BUCK6, LDO2, LDO3	0.2ms	10ms

Note 6: The power-off sequence is the reverse of the power-on sequence.

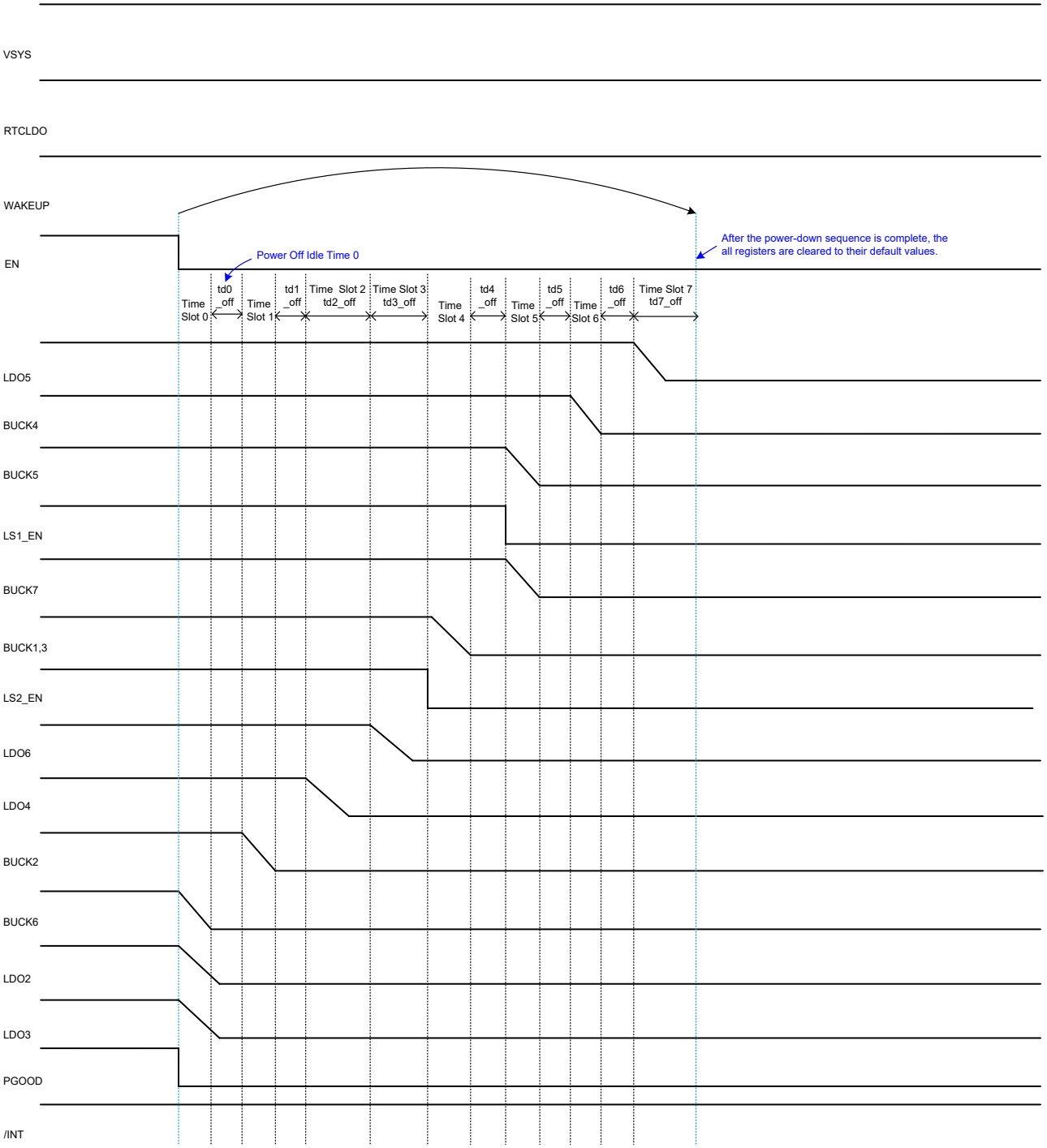
Timing Chart

APW7720-00 Power On Sequence



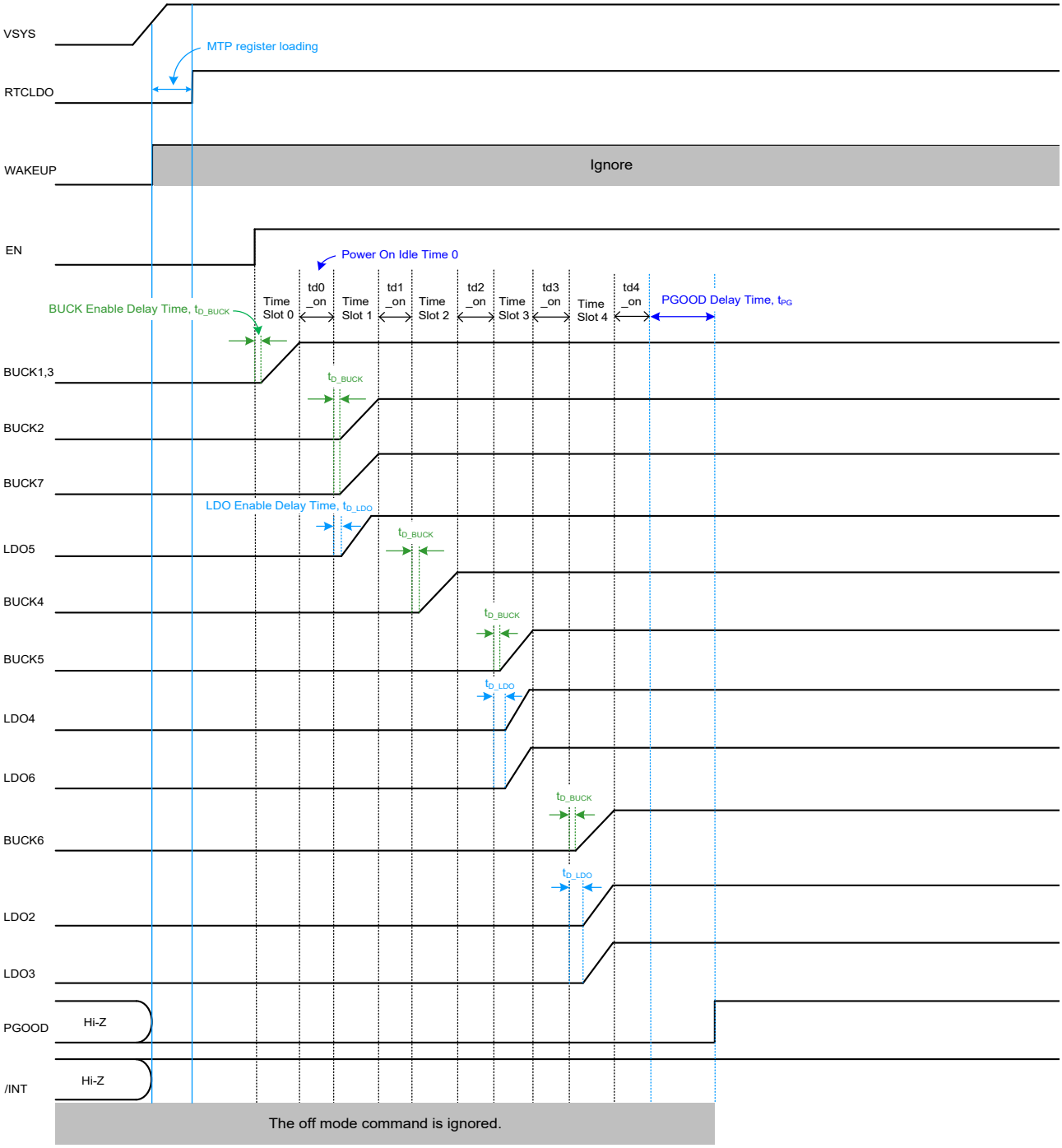
Timing Chart (Cont.)

APW7720-00 Power Off Sequence in Normal Operation



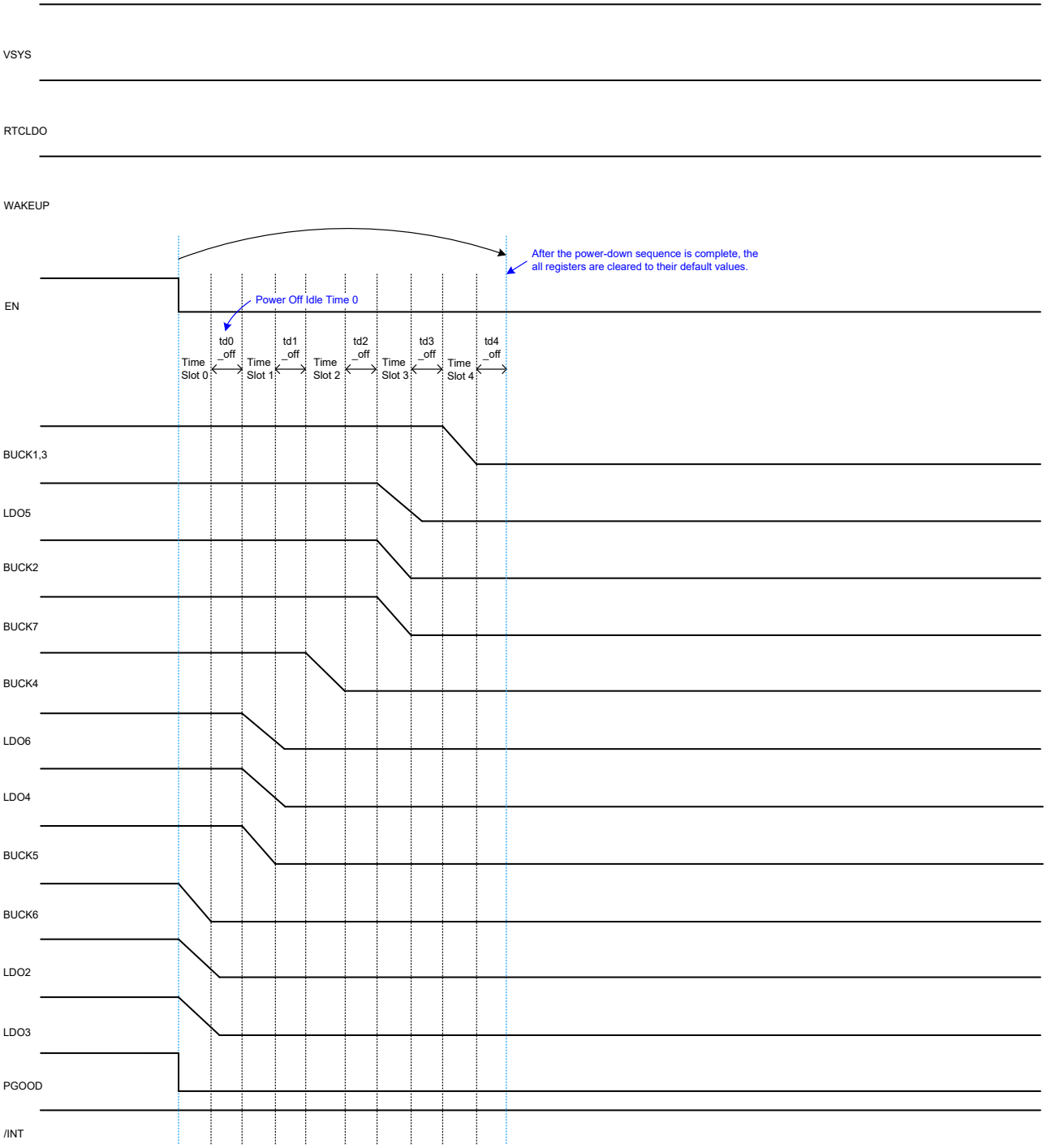
Timing Chart (Cont.)

APW7720-03 Power On Sequence



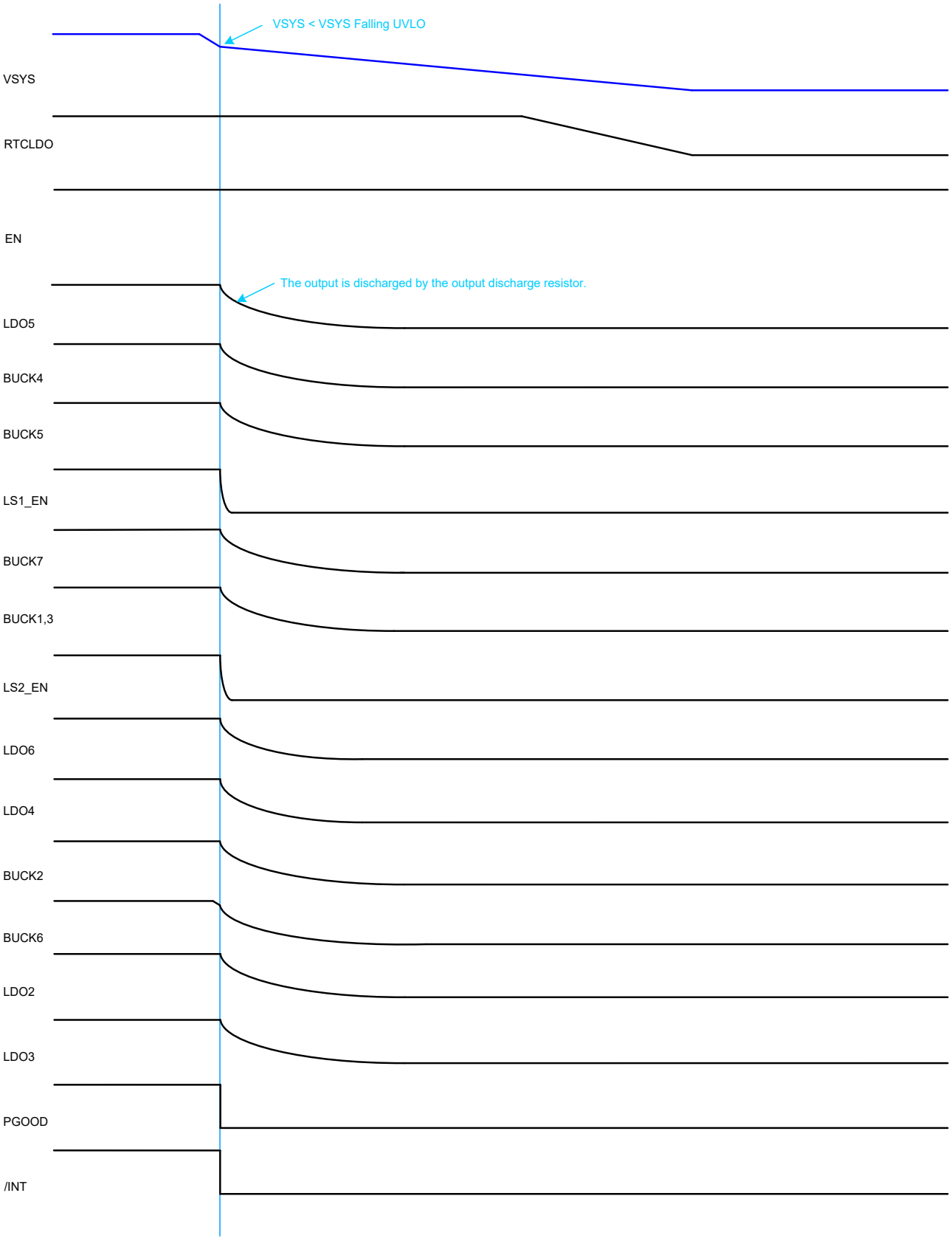
Timing Chart (Cont.)

APW7720-03 Power Off Sequence in Normal Operation



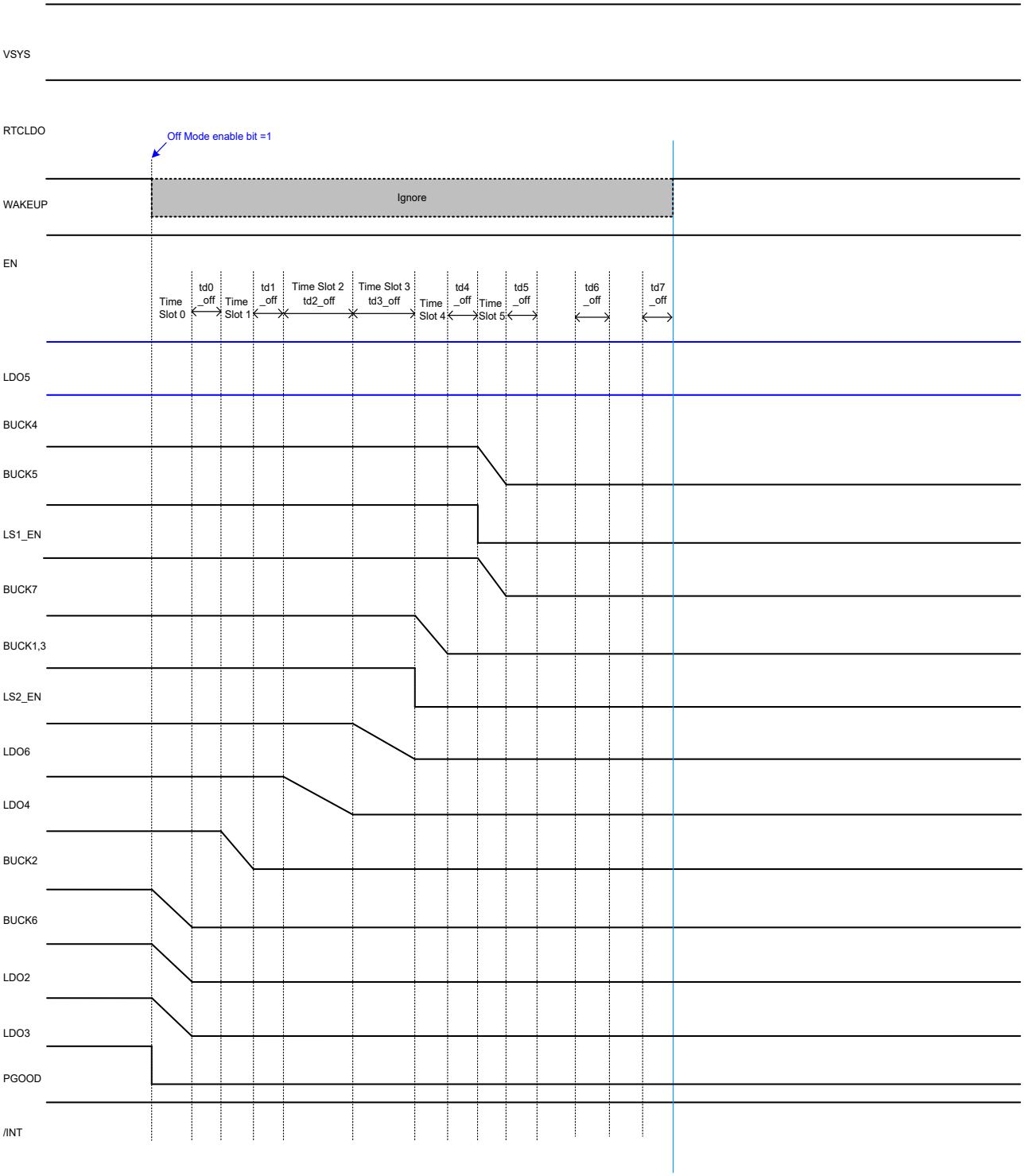
Timing Chart (Cont.)

VSYS UVLO Shutdown Sequence



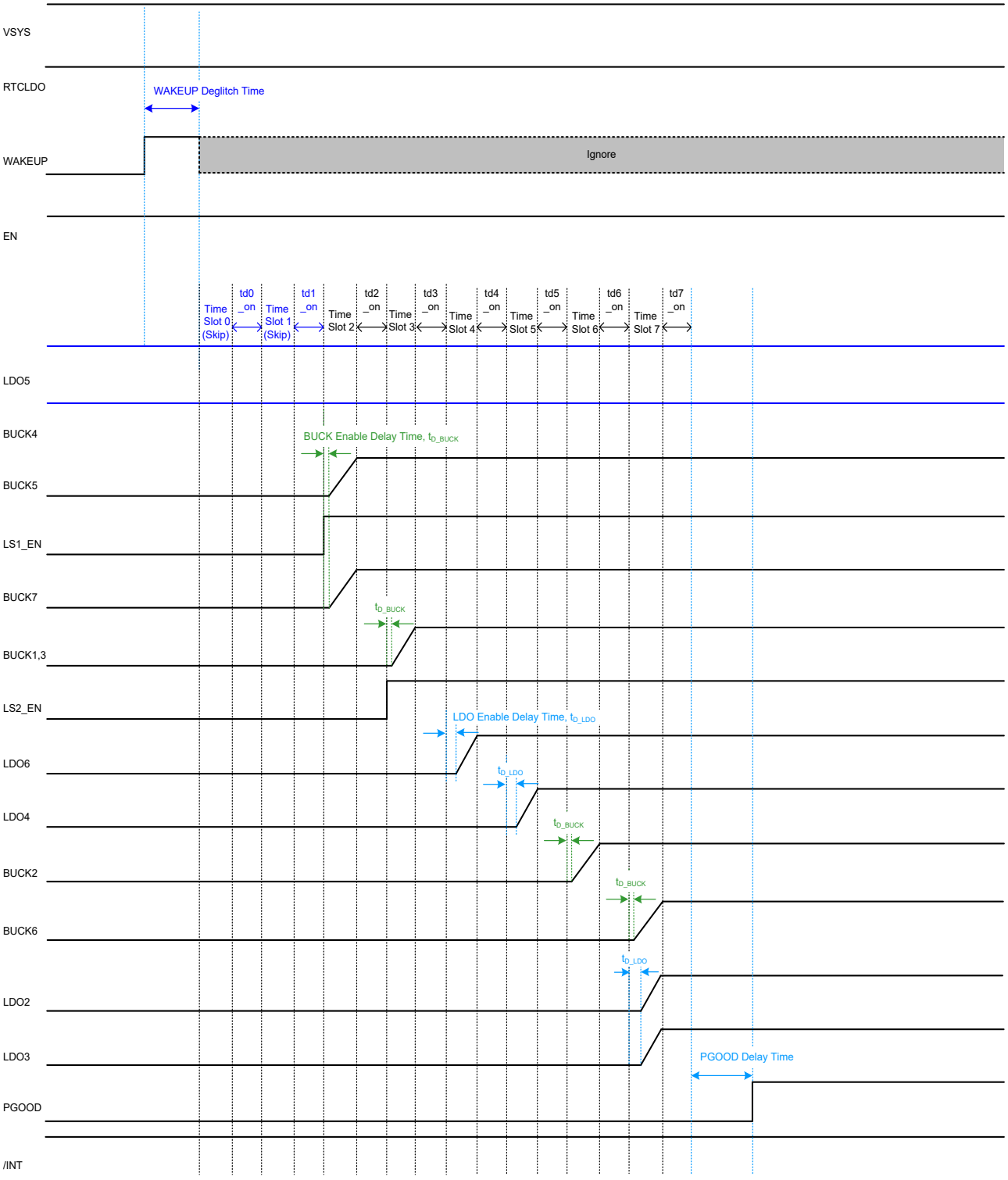
Timing Chart (Cont.)

APW7720-00 Off Mode Sequence (BUCK4, LDO5 still enabled)



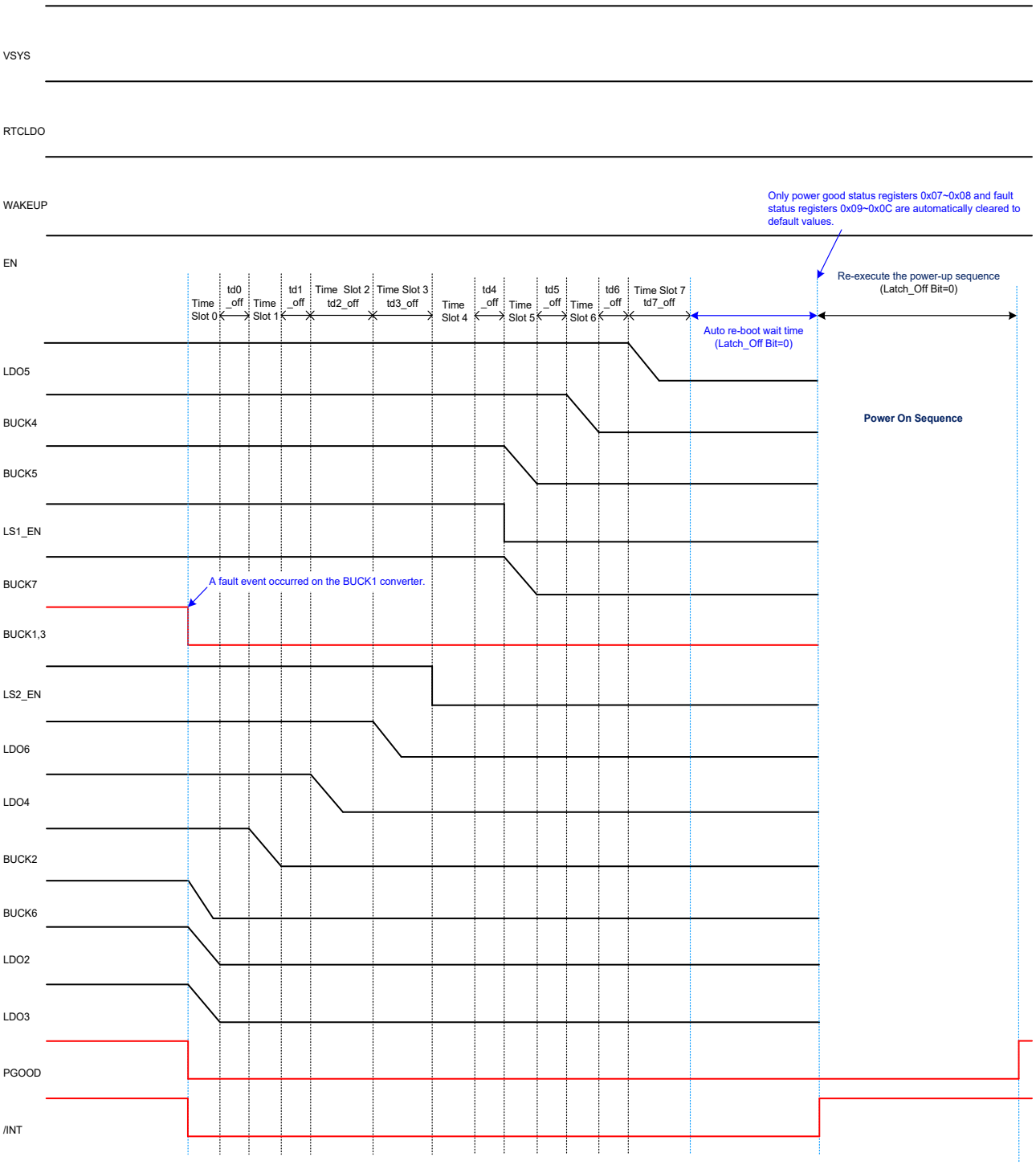
Timing Chart (Cont.)

APW7720-00 Wakeup Sequence in OFF Mode



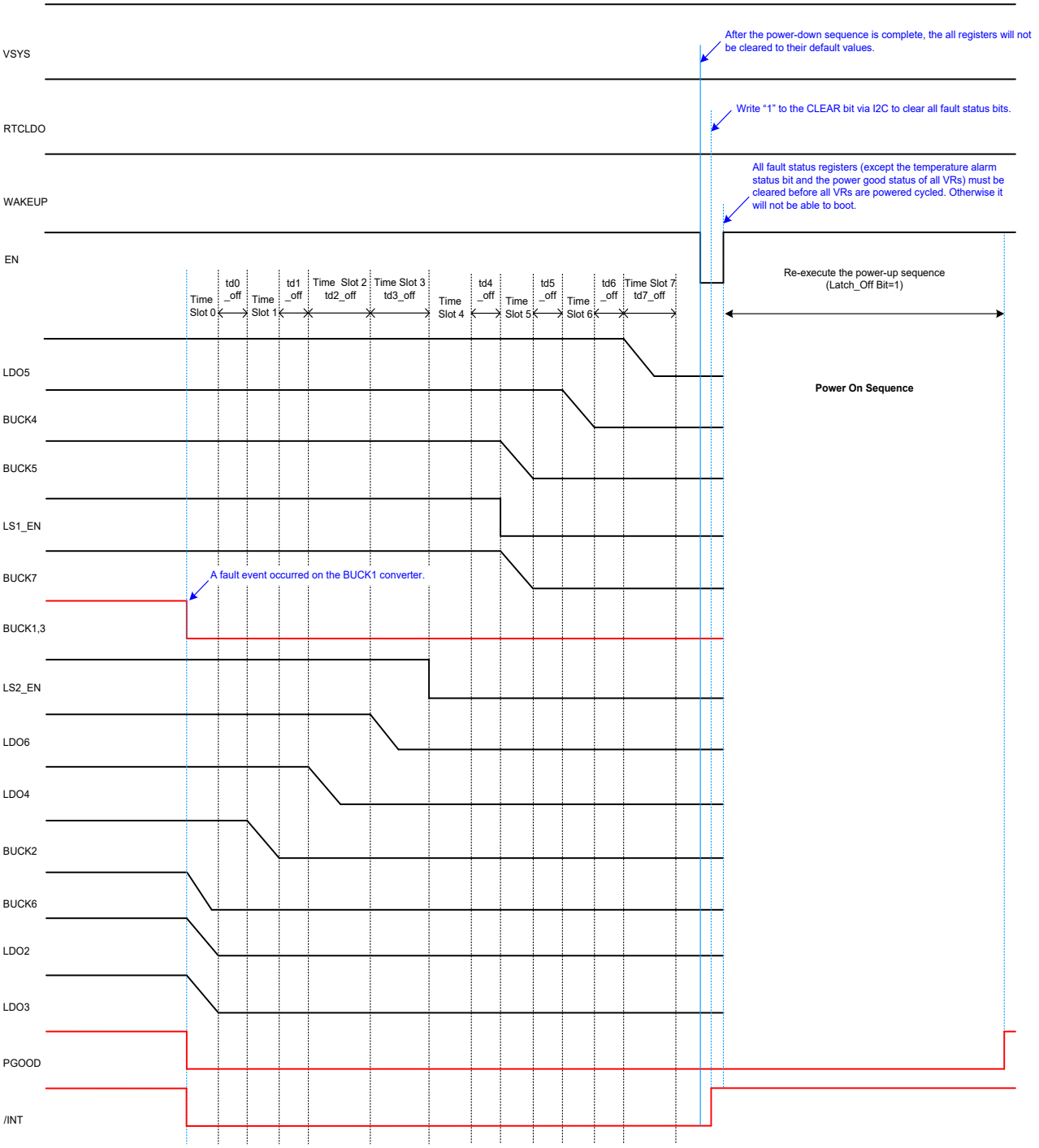
Timing Chart (Cont.)

APW7720-00 VR Fault Sequence (Auto-reboot Mode)



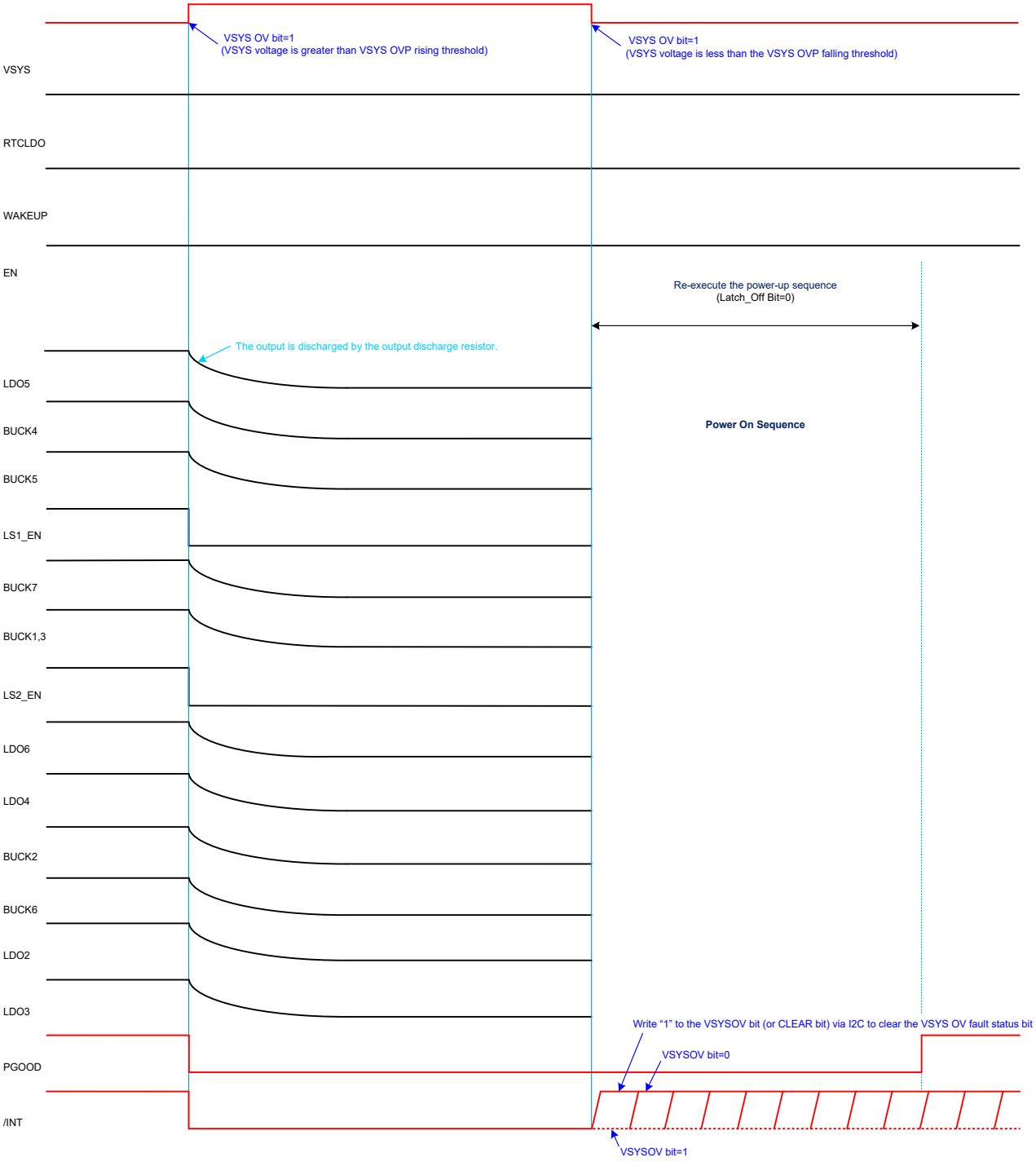
Timing Chart (Cont.)

APW7720-00 VR Fault Sequence (Latch Off Mode)



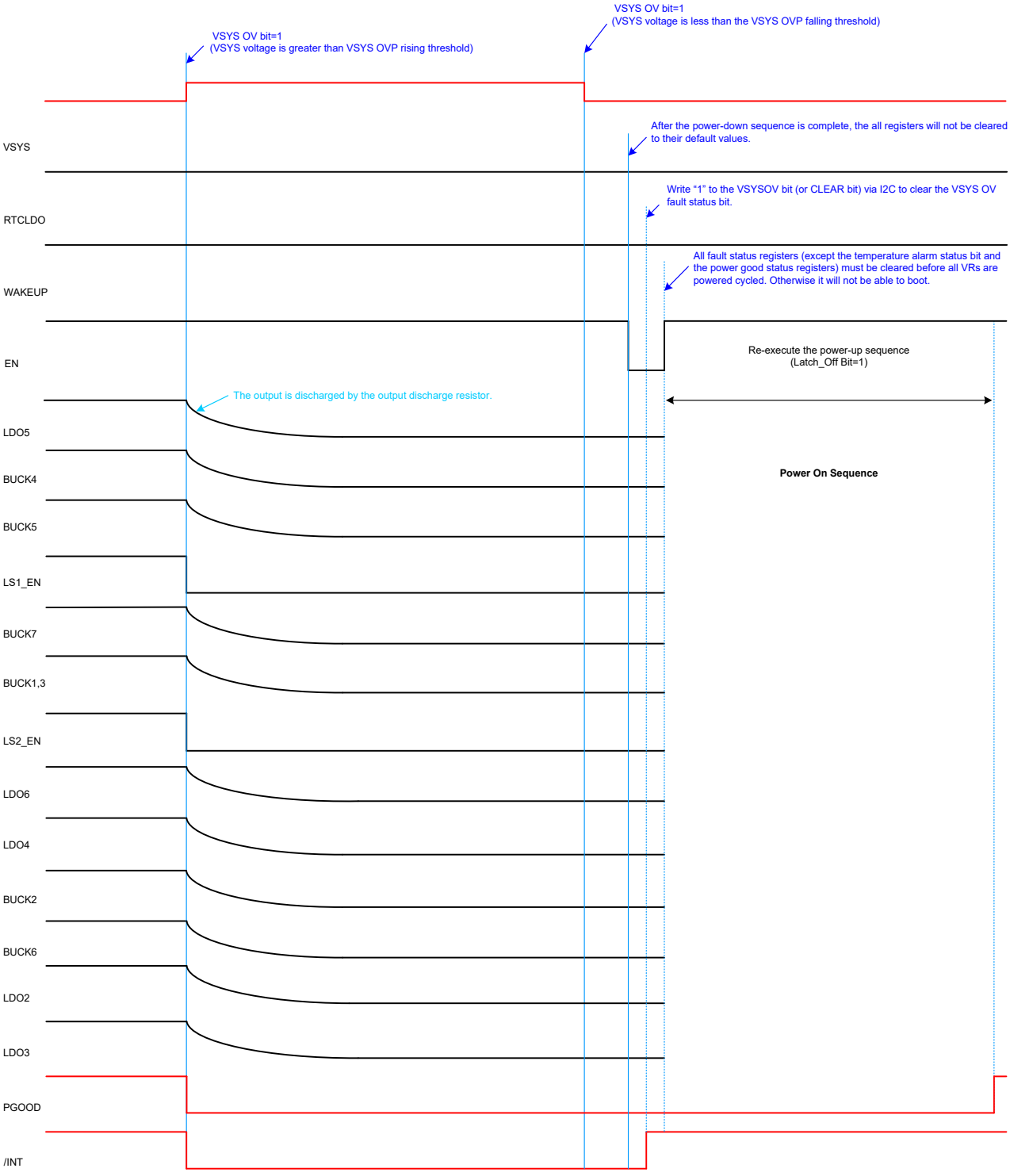
Timing Chart (Cont.)

VSYS Over-voltage Fault Sequence (Auto-reboot Mode)



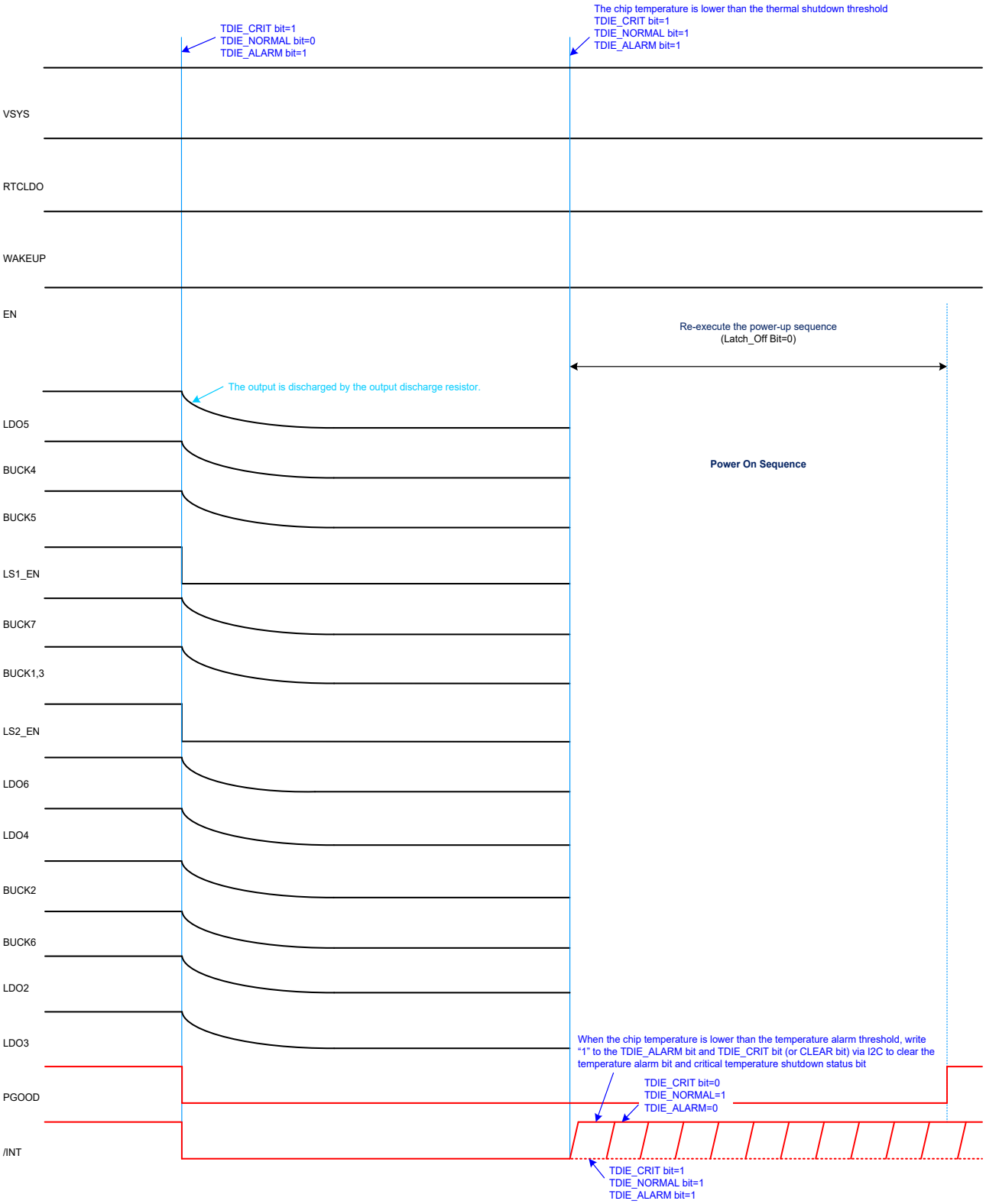
Timing Chart (Cont.)

VSYS Over-voltage Fault Sequence (Latch Off Mode)



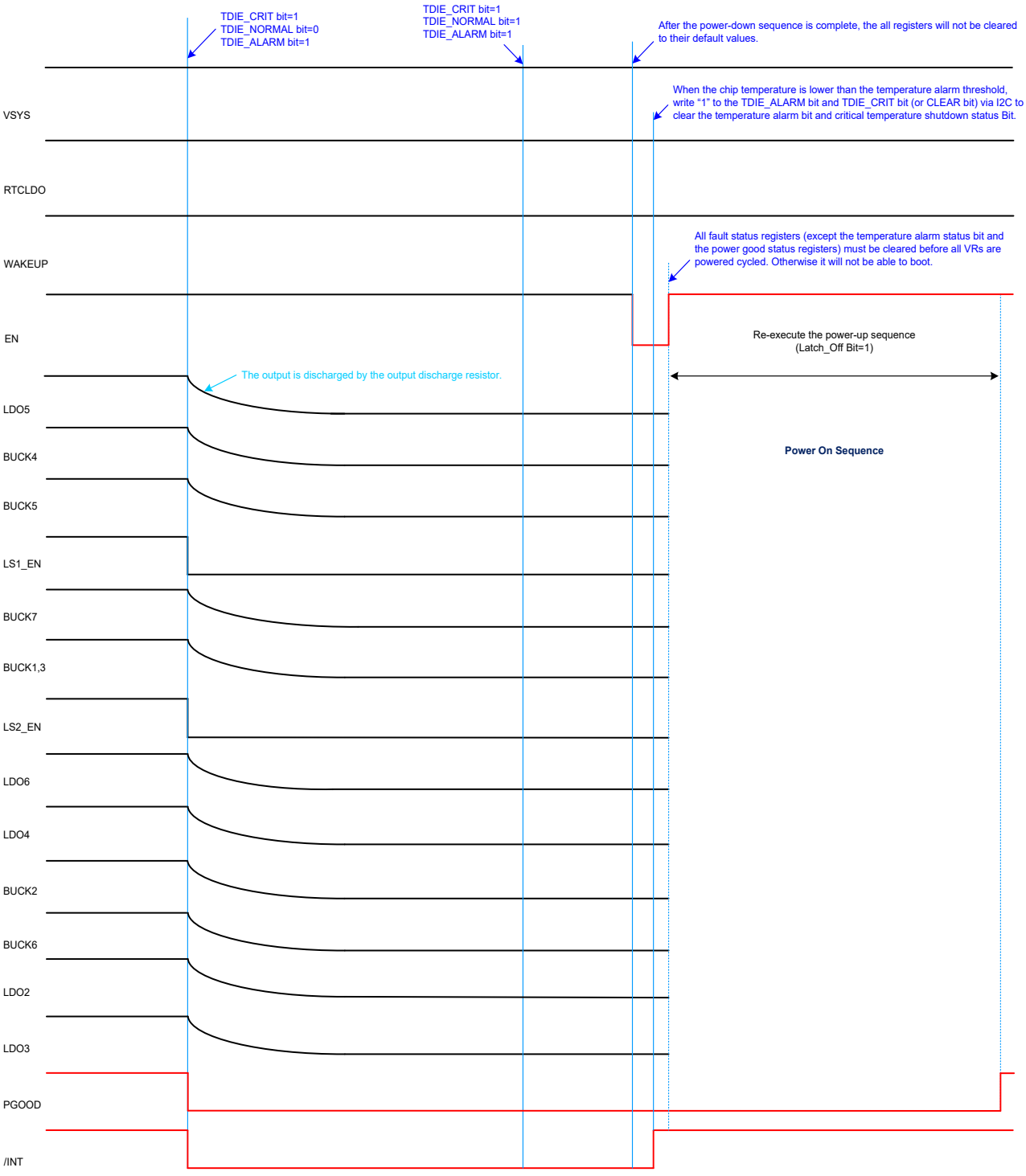
Timing Chart (Cont.)

Critical Temperature Shutdown Sequence (Auto-reboot Mode)



Timing Chart (Cont.)

Critical Temperature Shutdown Sequence (Latch Off Mode)



Timing Chart (Cont.)

Auto reboot mode vs. latch off mode comparison table

Operating Condition	Auto Reboot Mode	Latch Off Mode
VR Fault (Output OVP, Output UVP)	When a VR fault occurs and the PMIC completes the power-off sequence on its own, the PMIC will perform an automatic reboot. At this time, the power good status registers 0x07~0x08 and VR fault status registers 0x09~0x0C will be automatically cleared to the default value.	Status registers 0x07~0x0C must be manually cleared via I^2C by writing 1 to the CLEAR bit 0x13[0] or overwriting 1 to the fault bit of the status register 0x07~0x0C. **The VR fault status registers (except the power good status registers) must be cleared before all VRs are powered cycled. Otherwise the PMIC will not be able to reboot by toggling EN signal.**
VSYS OVP (Input OVP)	When the VSYS voltage falls below the VSYS OVP falling threshold, the PMIC re-executes the power-on sequence. VSYS OV status bit 0x0D[3] needs to be cleared manually via I^2C by writing 1 to the CLEAR bit 0x13[0] or overwriting 1 to VSYS OV status bit 0x0D[3].	VSYS OV status bit 0x0D[3] must be manually cleared via I^2C by writing 1 to the CLEAR bit 0x13[0] or overwriting 1 to VSYS OV status bit 0x0D[3]. **The VSYS OV status bit must be cleared before all VRs are powered cycled. Otherwise the PMIC will not be able to reboot by toggling EN signal.**
Thermal Shutdown	When the junction temperature falls below the thermal shutdown hysteresis temperature, the PMIC re-executes the power-up sequence. TDIE_CRIT status bit 0x0D[1] and TDIE_ALARM status bit 0xD[2] need to be cleared manually via I^2C by writing 1 to the CLEAR bit 0x13[0] or overwriting 1 to TDIE_CRIT status bit 0x0D[1] and TDIE_ALARM status bit 0x0D[2].	TDIE_CRIT status bit 0x0D[1] and TDIE_ALARM status bit 0xD[2] must be cleared manually via I^2C by writing 1 to the CLEAR bit 0x13[0] or overwriting 1 to TDIE_CRIT status bit 0x0D[1] and TDIE_ALARM status bit 0x0D[2]. **The TDIE_CRIT status bit (except the TDIE_ALARM status bit) must be cleared before all VRs are powered cycled. Otherwise the PMIC will not be able to reboot by toggling EN signal.**
Set EN=H to L (no fault event occurs)	All registers are cleared to default values. If the PMIC is performing power-off sequence but has not yet completed it, and the PMIC is re-enabled by EN, all registers will not be cleared to their default values.	

Operating Condition	When the power-off sequence is completed, set EN from high to low	When the power-off sequence is not completed, set EN from high to low
A fault event occurs in auto-reboot mode	(Before the auto-reboot, set EN from H to L) All registers are not reset to their default values.	All registers are reset to their default values.
A fault event occurs in latch off mode	All registers are not reset to their default values.	All registers are reset to their default values.

I²C Programming

I²C SERIAL CONTROL INTERFACE

I²C Overview

APW7720 PMIC is a slave-only device interfacing with an I²C Host Controller supporting the following transfer modes: Standard Mode – 100kbps, Fast Mode – 400kbps and Fast Mode – 1Mbps. The APW7720 PMIC is accessed using a 7-bit addressing scheme. The PMIC I²C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A hight-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the R/$\overline{W}$ bit a zero indicates a transmission (WRITE), a “one” indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7720 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

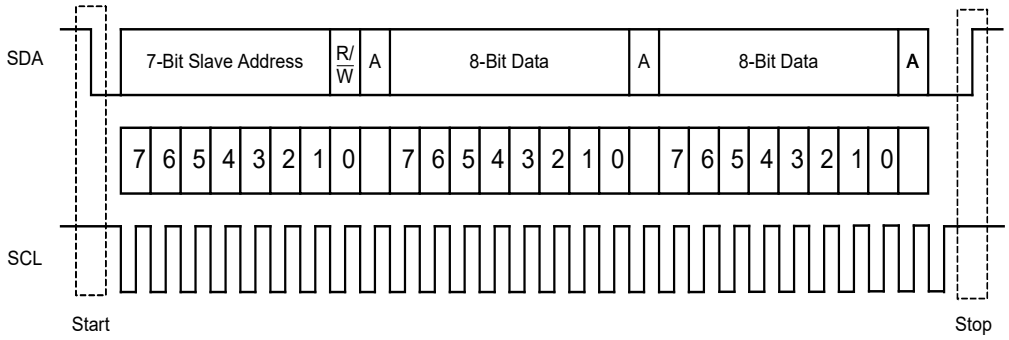


Figure 3. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. The device 7-bit address is defined as “0100100” (24h).

I²C Programming (Cont.)

Single-Byte Transfer

The serial control interface supports single-byte R/$\overline{W}$ operations for sub-addresses 0x00 to 0xFF.
Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7720 also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7720. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 2, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit determines the direction of the data transfer. For a write data transfer, the R/$\overline{W}$ bit will be a 0. After receiving the correct I²C device address and the R/$\overline{W}$ bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7720 internal memory address being accessed. After receiving the address byte, the APW7720 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7720 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

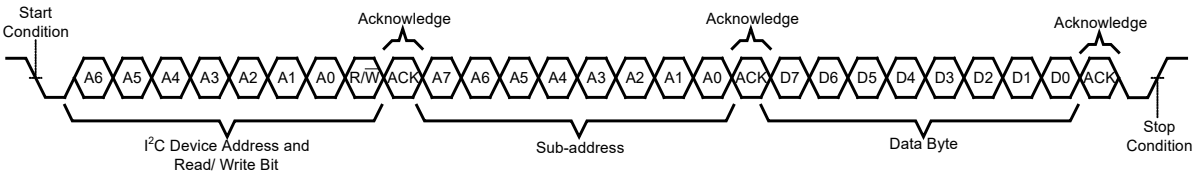


Figure 4. Single-Byte Write Transfer

Single-Byte Read

As shown in Figure 3, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/$\overline{W}$ bit becomes a 0. After receiving the APW7720 address and the R/$\overline{W}$ bit, APW7720 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7720 address and the R/W bit again. This time the R/$\overline{W}$ bit becomes a 1, indicating a read transfer. After receiving the address and the R/$\overline{W}$ bit, the APW7720 again responds with an acknowledge bit. Next, the APW7720 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

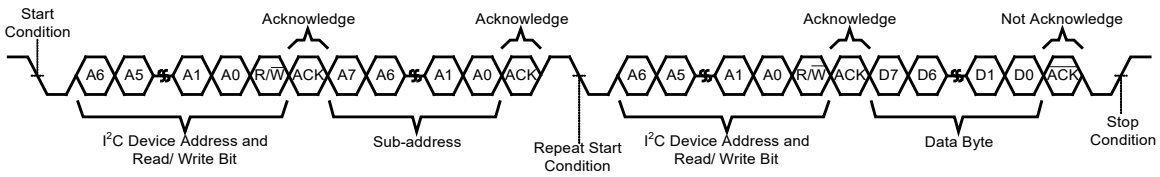


Figure 5. Single-Byte Read Transfer

I²C Programming (Cont.)

Symbol	Parameter	I²C mode (Open Drain)		Unit
		Min.	Max.	
I²C INTERFACE AC CHARACTERISTICS (Note 4)				
f_{OSCL}	Clock Frequency	0.01	1	MHz
t_{HIGH}	Clock High Pulse Width Time	260	-	ns
t_{LOW}	Clock Low Pulse Width Time	500	-	ns
$t_{TIMEOUT}$	Detect Clock Input Low Time	10	50	ms
t_R	Rise Time of I²C SDA/SCL	-	120	ns
t_F	Fall Time of I²C SDA/SCL	-	120	ns
$t_{SU:DAT}$	Data in Setup Time	50	-	ns
$t_{HD:DI}$	Data in Hold Time	0	-	ns
$t_{SU:STA}$	Start Condition Setup Time	260	-	ns
$t_{HD:STA}$	Start Condition Hold Time	260	-	ns
$t_{SU:STO}$	Stop Condition Setup Time	260	-	ns
t_{BUF}	Time between Stop Condition and next Start Condition	500	-	ns
$t_{HD:DAT}$	SDA Data Out Hold Time	0.5	350	ns

Note 4: Guarantee by design, not production test.

Timing Diagram

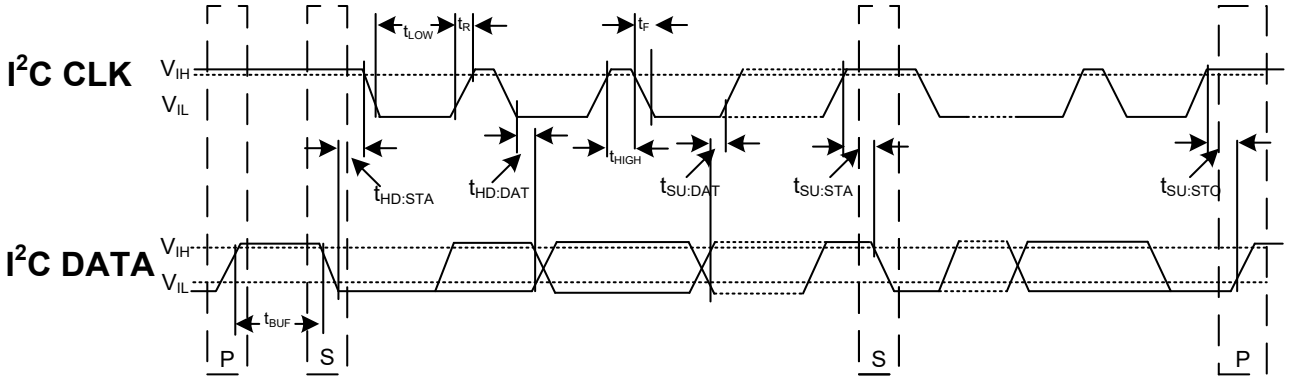


Figure 6: I²C Common AC Specification

Register Map

Key: Gray=Read Only; Green=Write-1-to-Clear; Yellow=Write Only

ADDRESS	REGISTER NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0x00	VENDOR_RSVD	-	VENDOR_RSVD								00
0x01	VENDOR_ID	R	VENDOR_ID[3:0]				REVISION[3:0]				12
0x02	OFF_MODE_EN_0	R/W	OFF_ MODE	OFF_ MODE_ EN_ BUCK7	OFF_ MODE_ EN_ BUCK6	OFF_ MODE_ EN_ BUCK5	OFF_ MODE_ EN_ BUCK4	OFF_ MODE_ EN_ BUCK3	OFF_ MODE_ EN_ BUCK2	OFF_ MODE_ EN_ BUCK1	00
0x03	OFF_MODE_EN_1	R/W	RSVD	OFF_ MODE_ EN_LDO6	OFF_ MODE_ EN_LDO5	OFF_ MODE_ EN_LDO4	OFF_ MODE_ EN_LDO3	OFF_ MODE_ EN_LDO2	OFF_ MODE_ EN_LS2_ EN	OFF_ MODE_ EN_LS1_ EN	00
0x04	REG_ CONTROL_0	R/W	RSVD	SD_ BUCK7	SD_ BUCK6	SD_ BUCK5	SD_ BUCK4	SD_ BUCK3	SD_ BUCK2	SD_ BUCK1	7F
0x05	REG_ CONTROL_1	R/W	RSVD	SD_LDO6	SD_LDO5	SD_LDO4	SD_LDO3	SD_LDO2	SD_LS2_ EN	SD_LS1_ EN	7F
0x06	WD_CNOTROL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WDT_RST	00
0x07	PG_BUCK_ STATUS	R	PGOOD	BUCK7PG	BUCK6PG	BUCK5PG	BUCK4PG	BUCK3PG	BUCK2PG	BUCK1PG	00
0x08	PG_LDO_STATUS	R	RSVD	RSVD	RSVD	LDO6PG	LDO5PG	LDO4PG	LDO3PG	LDO2PG	00
0x09	OV_BUCK_ STATUS	R	RSVD	BUCK7OV	BUCK6OV	BUCK5OV	BUCK4OV	BUCK3OV	BUCK2OV	BUCK1OV	00
0x0A	OV_LDO_STATUS	R	RSVD	RSVD	RSVD	LDO6OV	LDO5OV	LDO4OV	LDO3OV	LDO2OV	00
0x0B	UV_BUCK_ STATUS	R	RSVD	BUCK7UV	BUCK6UV	BUCK5UV	BUCK4UV	BUCK3UV	BUCK2UV	BUCK1UV	00
0x0C	UV_LDO_STATUS	R	RSVD	RSVD	RSVD	LDO6UV	LDO5UV	LDO4UV	LDO3UV	LDO2UV	00
0x0D	FAULT_STATUS	R	RSVD	RSVD	RSVD	RSVD	VSYSOV	TDIE _ALARM	TDIE_ CRIT	TDIE _NORMAL	01
0x0E	OV_BUCK_MASK	R/W	RSVD	MBUCK7OV	MBUCK6OV	MBUCK5OV	MBUCK4OV	MBUCK3OV	MBUCK2OV	MBUCK1OV	00
0x0F	OV_LDO_MASK	R/W	RSVD	RSVD	RSVD	MLDO6OV	MLDO5OV	MLDO4OV	MLDO3OV	MLDO2OV	00
0x10	UV_BUCK_MASK	R/W	RSVD	MBUCK7UV	MBUCK6UV	MBUCK5UV	MBUCK4UV	MBUCK3UV	MBUCK2UV	MBUCK1UV	00
0x11	UV_LDO_MASK	R/W	RSVD	RSVD	RSVD	MLDO6UV	MLDO5UV	MLDO4UV	MLDO3UV	MLDO2UV	00
0x12	FAULT _MASK	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MVSYS_ OV	MTDIE _ALARM	MTDIE _CRIT	00
0x13	FAULT_CLEAR	W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CLEAR	00
0x14 ~ 0x17	VENDOR_RSVD	R/W	VENDOR_RSVD								00

Note 7: Registers 0x14 to 0x1D, 0x35 to 0x36, and 0x7E to 0xFF are vendor-reserved registers. The System Management Controller (SMC) is prohibited from writing to these registers.

APW7720-00 MTP Register Map

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x18	VENDOR_RSVD	R/W	VENDOR_RSVD								55
0x19	VENDOR_RSVD	R/W	VENDOR_RSVD								AA
0x1A	SLAVE_ID	R/W	SLAVE_ID								48
0x1B	IC_ID	R/W	IC_ID								00
0x1C	USER_VERSION	R/W	USER_VERSION_ID								00
0x1D	PMIC_CFG_0	R/W	VENDOR_RSVD								24
0x1E	VBUCK1SET	R/W	VBUCK1SET								50
0x1F	VBUCK2SET	R/W	VBUCK2SET								50
0x20	VBUCK3SET	R/W	VBUCK3SET								50
0x21	VBUCK4SET	R/W	VBUCK4SET								5A
0x22	VBUCK5SET	R/W	VBUCK5SET								1B
0x23	VBUCK6SET	R/W	VBUCK6SET								E6
0x24	VBUCK7SET	R/W	VBUCK7SET								50
0x25	LDO2_CFG	R/W	MLDOSEL	MLDO2PG	VLDO2SET						2E
0x26	LDO3_CFG	R/W	RSVD	MLDO3PG	VLDO3SET						2E
0x27	LDO4_CFG	R/W	RSVD	MLDO4PG	VLDO4SET						3C
0x28	LDO5_CFG	R/W	RSVD	MLDO5PG	VLDO5SET						10
0x29	LDO6_CFG	R/W	RSVD	MLDO6PG	VLDO6SET						14
0x2A	BUCK1_CFG	R/W	RSVD	MBUCK1PG	PWM_BUCK1		RSVD	FS_BUCK1			31
0x2B	BUCK2_CFG	R/W	RSVD	MBUCK2PG	PWM_BUCK2		RSVD	FS_BUCK2			32
0x2C	BUCK3_CFG	R/W	RSVD	MBUCK3PG	PWM_BUCK3		RSVD	FS_BUCK3			31
0x2D	BUCK4_CFG	R/W	RSVD	MBUCK4PG	PWM_BUCK4		RSVD	FS_BUCK4			32
0x2E	BUCK5_CFG	R/W	RSVD	MBUCK5PG	PWM_BUCK5		RSVD	FS_BUCK5			32
0x2F	BUCK6_CFG	R/W	RSVD	MBUCK6PG	PWM_BUCK6		RSVD	FS_BUCK6			32
0x30	BUCK7_CFG	R/W	RSVD	MBUCK7PG	PWM_BUCK7		RSVD	FS_BUCK7			32
0x31	BUCK_RU_1	R/W	RSVD		BUCK7RU		BUCK6RU		BUCK5RU		00
0x32	BUCK_RU_0	R/W	BUCK4RU		BUCK3RU		BUCK2RU		BUCK1RU		00
0x33	BUCK_RD_1	R/W	RSVD		BUCK7RD		BUCK6RD		BUCK5RD		00
0x34	BUCK_RD_0	R/W	BUCK4RD		BUCK3RD		BUCK2RD		BUCK1RD		00
0x35	PMIC_CFG_1	R/W	VENDOR_RSVD								-
0x36	VENDOR_RSVD	R/W	RSVD								-
0x37	TIMER	R/W	PGDELAY				WDTMR				3D

Note 7: Registers 0x14 to 0x1D, 0x35 to 0x36, and 0x7E to 0xFF are vendor-reserved registers. The System Management Controller (SMC) is prohibited from writing to these registers.

APW7720-00 MTP Register Map (Cont.)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x38	PON_IDLE_TIME_0	R/W	RSVD		PON_TSLOT1_IDLE			PON_TSLOT0_IDLE			00
0x39	PON_IDLE_TIME_1	R/W	RSVD		PON_TSLOT3_IDLE			PON_TSLOT2_IDLE			00
0x3A	PON_IDLE_TIME_2	R/W	RSVD		PON_TSLOT5_IDLE			PON_TSLOT4_IDLE			00
0x3B	PON_IDLE_TIME_3	R/W	RSVD		PON_TSLOT7_IDLE			PON_TSLOT6_IDLE			00
0x3C	PON_IDLE_TIME_4	R/W	RSVD		PON_TSLOT9_IDLE			PON_TSLOT8_IDLE			00
0x3D	PON_IDLE_TIME_5	R/W	RSVD		PON_TSLOT11_IDLE			PON_TSLOT10_IDLE			00
0x3E	PON_IDLE_TIME_6	R/W	RSVD		PON_TSLOT13_IDLE			PON_TSLOT12_IDLE			00
0x3F	POFF_IDLE_TIME_0	R/W	RSVD		POFF_TSLOT1_IDLE			POFF_TSLOT0_IDLE			00
0x40	POFF_IDLE_TIME_1	R/W	RSVD		POFF_TSLOT3_IDLE			POFF_TSLOT2_IDLE			00
0x41	POFF_IDLE_TIME_2	R/W	RSVD		POFF_TSLOT5_IDLE			POFF_TSLOT4_IDLE			00
0x43	POFF_IDLE_TIME_3	R/W	RSVD		POFF_TSLOT7_IDLE			POFF_TSLOT6_IDLE			00
0x43	POFF_IDLE_TIME_4	R/W	RSVD		POFF_TSLOT9_IDLE			POFF_TSLOT8_IDLE			00
0x44	POFF_IDLE_TIME_5	R/W	RSVD		POFF_TSLOT11_IDLE			POFF_TSLOT10_IDLE			00
0x45	POFF_IDLE_TIME_6	R/W	RSVD		POFF_TSLOT13_IDLE			POFF_TSLOT12_IDLE			00
0x46	PON_SEQ_TIME_SLOT0_H	R/W	PON_TSLOT0_EN	PON_TSLOT0_BUCK7_EN	PON_TSLOT0_BUCK6_EN	PON_TSLOT0_BUCK5_EN	PON_TSLOT0_BUCK4_EN	PON_TSLOT0_BUCK3_EN	PON_TSLOT0_BUCK2_EN	PON_TSLOT0_BUCK1_EN	80
0x47	PON_SEQ_TIME_SLOT0_L	R/W	RSVD	PON_TSLOT0_LDO6_EN	PON_TSLOT0_LDO5_EN	PON_TSLOT0_LDO4_EN	PON_TSLOT0_LDO3_EN	PON_TSLOT0_LDO2_EN	PON_TSLOT0_LS2_EN	PON_TSLOT0_LS1_EN	20
0x48	PON_SEQ_TIME_SLOT1_H	R/W	PON_TSLOT1_EN	PON_TSLOT1_BUCK7_EN	PON_TSLOT1_BUCK6_EN	PON_TSLOT1_BUCK5_EN	PON_TSLOT1_BUCK4_EN	PON_TSLOT1_BUCK3_EN	PON_TSLOT1_BUCK2_EN	PON_TSLOT1_BUCK1_EN	88
0x49	PON_SEQ_TIME_SLOT1_L	R/W	RSVD	PON_TSLOT1_LDO6_EN	PON_TSLOT1_LDO5_EN	PON_TSLOT1_LDO4_EN	PON_TSLOT1_LDO3_EN	PON_TSLOT1_LDO2_EN	PON_TSLOT1_LS2_EN	PON_TSLOT1_LS1_EN	00
0x4A	PON_SEQ_TIME_SLOT2_H	R/W	PON_TSLOT2_EN	PON_TSLOT2_BUCK7_EN	PON_TSLOT2_BUCK6_EN	PON_TSLOT2_BUCK5_EN	PON_TSLOT2_BUCK4_EN	PON_TSLOT2_BUCK3_EN	PON_TSLOT2_BUCK2_EN	PON_TSLOT2_BUCK1_EN	D0
0x4B	PON_SEQ_TIME_SLOT2_L	R/W	RSVD	PON_TSLOT2_LDO6_EN	PON_TSLOT2_LDO5_EN	PON_TSLOT2_LDO4_EN	PON_TSLOT2_LDO3_EN	PON_TSLOT2_LDO2_EN	PON_TSLOT2_LS2_EN	PON_TSLOT2_LS1_EN	01
0x4C	PON_SEQ_TIME_SLOT3_H	R/W	PON_TSLOT3_EN	PON_TSLOT3_BUCK7_EN	PON_TSLOT3_BUCK6_EN	PON_TSLOT3_BUCK5_EN	PON_TSLOT3_BUCK4_EN	PON_TSLOT3_BUCK3_EN	PON_TSLOT3_BUCK2_EN	PON_TSLOT3_BUCK1_EN	81
0x4D	PON_SEQ_TIME_SLOT3_L	R/W	RSVD	PON_TSLOT3_LDO6_EN	PON_TSLOT3_LDO5_EN	PON_TSLOT3_LDO4_EN	PON_TSLOT3_LDO3_EN	PON_TSLOT3_LDO2_EN	PON_TSLOT3_LS2_EN	PON_TSLOT3_LS1_EN	02
0x4E	PON_SEQ_TIME_SLOT4_H	R/W	PON_TSLOT4_EN	PON_TSLOT4_BUCK7_EN	PON_TSLOT4_BUCK6_EN	PON_TSLOT4_BUCK5_EN	PON_TSLOT4_BUCK4_EN	PON_TSLOT4_BUCK3_EN	PON_TSLOT4_BUCK2_EN	PON_TSLOT4_BUCK1_EN	80
0x4F	PON_SEQ_TIME_SLOT4_L	R/W	RSVD	PON_TSLOT4_LDO6_EN	PON_TSLOT4_LDO5_EN	PON_TSLOT4_LDO4_EN	PON_TSLOT4_LDO3_EN	PON_TSLOT4_LDO2_EN	PON_TSLOT4_LS2_EN	PON_TSLOT4_LS1_EN	40
0x50	PON_SEQ_TIME_SLOT5_H	R/W	PON_TSLOT5_EN	PON_TSLOT5_BUCK7_EN	PON_TSLOT5_BUCK6_EN	PON_TSLOT5_BUCK5_EN	PON_TSLOT5_BUCK4_EN	PON_TSLOT5_BUCK3_EN	PON_TSLOT5_BUCK2_EN	PON_TSLOT5_BUCK1_EN	80
0x51	PON_SEQ_TIME_SLOT5_L	R/W	RSVD	PON_TSLOT5_LDO6_EN	PON_TSLOT5_LDO5_EN	PON_TSLOT5_LDO4_EN	PON_TSLOT5_LDO3_EN	PON_TSLOT5_LDO2_EN	PON_TSLOT5_LS2_EN	PON_TSLOT5_LS1_EN	10
0x52	PON_SEQ_TIME_SLOT6_H	R/W	PON_TSLOT6_EN	PON_TSLOT6_BUCK7_EN	PON_TSLOT6_BUCK6_EN	PON_TSLOT6_BUCK6_EN	PON_TSLOT6_BUCK4_EN	PON_TSLOT6_BUCK3_EN	PON_TSLOT6_BUCK2_EN	PON_TSLOT6_BUCK1_EN	82
0x53	PON_SEQ_TIME_SLOT6_L	R/W	RSVD	PON_TSLOT6_LDO6_EN	PON_TSLOT6_LDO5_EN	PON_TSLOT6_LDO4_EN	PON_TSLOT6_LDO3_EN	PON_TSLOT6_LDO2_EN	PON_TSLOT6_LS2_EN	PON_TSLOT6_LS1_EN	00

APW7720-00 MTP Register Map (Cont.)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x54	PON_SEQ_TIME_SLOT7_H	R/W	PON_TSLOT7_EN	PON_TSLOT7_BUCK7_EN	PON_TSLOT7_BUCK6_EN	PON_TSLOT7_BUCK5_EN	PON_TSLOT7_BUCK4_EN	PON_TSLOT7_BUCK3_EN	PON_TSLOT7_BUCK2_EN	PON_TSLOT7_BUCK1_EN	A0
0x55	PON_SEQ_TIME_SLOT7_L	R/W	RSVD	PON_TSLOT7_LDO6_EN	PON_TSLOT7_LDO5_EN	PON_TSLOT7_LDO4_EN	PON_TSLOT7_LDO3_EN	PON_TSLOT7_LDO2_EN	PON_TSLOT7_LS2_EN	PON_TSLOT7_LS1_EN	0C
0x56	PON_SEQ_TIME_SLOT8_H	R/W	PON_TSLOT8_EN	PON_TSLOT8_BUCK7_EN	PON_TSLOT8_BUCK6_EN	PON_TSLOT8_BUCK5_EN	PON_TSLOT8_BUCK4_EN	PON_TSLOT8_BUCK3_EN	PON_TSLOT8_BUCK2_EN	PON_TSLOT8_BUCK1_EN	00
0x57	PON_SEQ_TIME_SLOT8_L	R/W	RSVD	PON_TSLOT8_LDO6_EN	PON_TSLOT8_LDO5_EN	PON_TSLOT8_LDO4_EN	PON_TSLOT8_LDO3_EN	PON_TSLOT8_LDO2_EN	PON_TSLOT8_LS2_EN	PON_TSLOT8_LS1_EN	00
0x58	PON_SEQ_TIME_SLOT9_H	R/W	PON_TSLOT9_EN	PON_TSLOT9_BUCK7_EN	PON_TSLOT9_BUCK6_EN	PON_TSLOT9_BUCK5_EN	PON_TSLOT9_BUCK4_EN	PON_TSLOT9_BUCK3_EN	PON_TSLOT9_BUCK2_EN	PON_TSLOT9_BUCK1_EN	00
0x59	PON_SEQ_TIME_SLOT9_L	R/W	RSVD	PON_TSLOT9_LDO6_EN	PON_TSLOT9_LDO5_EN	PON_TSLOT9_LDO4_EN	PON_TSLOT9_LDO3_EN	PON_TSLOT9_LDO2_EN	PON_TSLOT9_LS2_EN	PON_TSLOT9_LS1_EN	00
0x5A	PON_SEQ_TIME_SLOT10_H	R/W	PON_TSLOT10_EN	PON_TSLOT10_BUCK8_EN	PON_TSLOT10_BUCK6_EN	PON_TSLOT10_BUCK5_EN	PON_TSLOT10_BUCK4_EN	PON_TSLOT10_BUCK3_EN	PON_TSLOT10_BUCK2_EN	PON_TSLOT10_BUCK1_EN	00
0x5B	PON_SEQ_TIME_SLOT10_L	R/W	RSVD	PON_TSLOT10_LDO6_EN	PON_TSLOT10_LDO5_EN	PON_TSLOT10_LDO4_EN	PON_TSLOT10_LDO3_EN	PON_TSLOT10_LDO2_EN	PON_TSLOT10_LS2_EN	PON_TSLOT10_LS1_EN	00
0x5C	PON_SEQ_TIME_SLOT11_H	R/W	PON_TSLOT11_EN	PON_TSLOT11_BUCK8_EN	PON_TSLOT11_BUCK6_EN	PON_TSLOT11_BUCK5_EN	PON_TSLOT11_BUCK4_EN	PON_TSLOT11_BUCK3_EN	PON_TSLOT11_BUCK2_EN	PON_TSLOT11_BUCK1_EN	00
0x5D	PON_SEQ_TIME_SLOT11_L	R/W	RSVD	PON_TSLOT11_LDO6_EN	PON_TSLOT11_LDO5_EN	PON_TSLOT11_LDO4_EN	PON_TSLOT11_LDO3_EN	PON_TSLOT11_LDO2_EN	PON_TSLOT11_LS2_EN	PON_TSLOT11_LS1_EN	00
0x5E	PON_SEQ_TIME_SLOT12_H	R/W	PON_TSLOT12_EN	PON_TSLOT12_BUCK8_EN	PON_TSLOT12_BUCK6_EN	PON_TSLOT12_BUCK5_EN	PON_TSLOT12_BUCK4_EN	PON_TSLOT12_BUCK3_EN	PON_TSLOT12_BUCK2_EN	PON_TSLOT12_BUCK1_EN	00
0x5F	PON_SEQ_TIME_SLOT12_L	R/W	RSVD	PON_TSLOT12_LDO6_EN	PON_TSLOT12_LDO5_EN	PON_TSLOT12_LDO4_EN	PON_TSLOT12_LDO3_EN	PON_TSLOT12_LDO2_EN	PON_TSLOT12_LS2_EN	PON_TSLOT12_LS1_EN	00
0x60	PON_SEQ_TIME_SLOT13_H	R/W	PON_TSLOT13_EN	PON_TSLOT13_BUCK8_EN	PON_TSLOT13_BUCK6_EN	PON_TSLOT13_BUCK5_EN	PON_TSLOT13_BUCK4_EN	PON_TSLOT13_BUCK3_EN	PON_TSLOT13_BUCK2_EN	PON_TSLOT13_BUCK1_EN	00
0x61	PON_SEQ_TIME_SLOT13_L	R/W	RSVD	PON_TSLOT13_LDO6_EN	PON_TSLOT13_LDO5_EN	PON_TSLOT13_LDO4_EN	PON_TSLOT13_LDO3_EN	PON_TSLOT13_LDO2_EN	PON_TSLOT13_LS2_EN	PON_TSLOT13_LS1_EN	00
0x62	POFF_SEQ_TIME_SLOT0_H	R/W	POFF_TSLOT0_EN	POFF_TSLOT0_BUCK7_EN	POFF_TSLOT0_BUCK6_EN	POFF_TSLOT0_BUCK5_EN	POFF_TSLOT0_BUCK4_EN	POFF_TSLOT0_BUCK3_EN	POFF_TSLOT0_BUCK2_EN	POFF_TSLOT0_BUCK1_EN	A0
0x63	POFF_SEQ_TIME_SLOT0_L	R/W	RSVD	POFF_TSLOT0_LDO6_EN	POFF_TSLOT0_LDO5_EN	POFF_TSLOT0_LDO4_EN	POFF_TSLOT0_LDO3_EN	POFF_TSLOT0_LDO2_EN	POFF_TSLOT0_LS2_EN	POFF_TSLOT0_LS1_EN	0C
0x64	POFF_SEQ_TIME_SLOT1_H	R/W	POFF_TSLOT1_EN	POFF_TSLOT1_BUCK7_EN	POFF_TSLOT1_BUCK6_EN	POFF_TSLOT1_BUCK5_EN	POFF_TSLOT1_BUCK4_EN	POFF_TSLOT1_BUCK3_EN	POFF_TSLOT1_BUCK2_EN	POFF_TSLOT1_BUCK1_EN	82
0x65	POFF_SEQ_TIME_SLOT1_L	R/W	RSVD	POFF_TSLOT1_LDO6_EN	POFF_TSLOT1_LDO5_EN	POFF_TSLOT1_LDO4_EN	POFF_TSLOT1_LDO3_EN	POFF_TSLOT1_LDO2_EN	POFF_TSLOT1_LS2_EN	POFF_TSLOT1_LS1_EN	00

APW7720-00 MTP Register Map (Cont.)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x66	POFF_SEQ_TIME_SLOT2_H	R/W	POFF_TSLOT2_EN	POFF_TSLOT2_BUCK7_EN	POFF_TSLOT2_BUCK6_EN	POFF_TSLOT2_BUCK5_EN	POFF_TSLOT2_BUCK4_EN	POFF_TSLOT2_BUCK3_EN	POFF_TSLOT2_BUCK2_EN	POFF_TSLOT2_BUCK1_EN	80
0x68	POFF_SEQ_TIME_SLOT2_L	R/W	RSVD	POFF_TSLOT2_LDO6_EN	POFF_TSLOT2_LDO5_EN	POFF_TSLOT2_LDO4_EN	POFF_TSLOT2_LDO3_EN	POFF_TSLOT2_LDO2_EN	POFF_TSLOT2_LS2_EN	POFF_TSLOT2_LS1_EN	10
0x68	POFF_SEQ_TIME_SLOT3_H	R/W	POFF_TSLOT3_EN	POFF_TSLOT3_BUCK7_EN	POFF_TSLOT3_BUCK6_EN	POFF_TSLOT3_BUCK5_EN	POFF_TSLOT3_BUCK4_EN	POFF_TSLOT3_BUCK3_EN	POFF_TSLOT3_BUCK2_EN	POFF_TSLOT3_BUCK1_EN	80
0x69	POFF_SEQ_TIME_SLOT3_L	R/W	RSVD	POFF_TSLOT3_LDO6_EN	POFF_TSLOT3_LDO5_EN	POFF_TSLOT3_LDO4_EN	POFF_TSLOT3_LDO3_EN	POFF_TSLOT3_LDO2_EN	POFF_TSLOT3_LS2_EN	POFF_TSLOT3_LS1_EN	40
0x6A	POFF_SEQ_TIME_SLOT4_H	R/W	POFF_TSLOT4_EN	POFF_TSLOT4_BUCK7_EN	POFF_TSLOT4_BUCK6_EN	POFF_TSLOT4_BUCK5_EN	POFF_TSLOT4_BUCK4_EN	POFF_TSLOT4_BUCK3_EN	POFF_TSLOT4_BUCK2_EN	POFF_TSLOT4_BUCK1_EN	81
0x6B	POFF_SEQ_TIME_SLOT4_L	R/W	RSVD	POFF_TSLOT4_LDO6_EN	POFF_TSLOT4_LDO5_EN	POFF_TSLOT4_LDO4_EN	POFF_TSLOT4_LDO3_EN	POFF_TSLOT4_LDO2_EN	POFF_TSLOT4_LS2_EN	POFF_TSLOT4_LS1_EN	02
0x6C	POFF_SEQ_TIME_SLOT5_H	R/W	POFF_TSLOT5_EN	POFF_TSLOT5_BUCK7_EN	POFF_TSLOT5_BUCK6_EN	POFF_TSLOT5_BUCK5_EN	POFF_TSLOT5_BUCK4_EN	POFF_TSLOT5_BUCK3_EN	POFF_TSLOT5_BUCK2_EN	POFF_TSLOT5_BUCK1_EN	D0
0x6D	POFF_SEQ_TIME_SLOT5_L	R/W	RSVD	POFF_TSLOT5_LDO6_EN	POFF_TSLOT5_LDO5_EN	POFF_TSLOT5_LDO4_EN	POFF_TSLOT5_LDO3_EN	POFF_TSLOT5_LDO2_EN	POFF_TSLOT5_LS2_EN	POFF_TSLOT5_LS1_EN	01
0x6E	POFF_SEQ_TIME_SLOT6_H	R/W	POFF_TSLOT6_EN	POFF_TSLOT6_BUCK7_EN	POFF_TSLOT6_BUCK6_EN	POFF_TSLOT6_BUCK5_EN	POFF_TSLOT6_BUCK4_EN	POFF_TSLOT6_BUCK3_EN	POFF_TSLOT6_BUCK2_EN	POFF_TSLOT6_BUCK1_EN	88
0x6F	POFF_SEQ_TIME_SLOT6_L	R/W	RSVD	POFF_TSLOT6_LDO6_EN	POFF_TSLOT6_LDO5_EN	POFF_TSLOT6_LDO4_EN	POFF_TSLOT6_LDO3_EN	POFF_TSLOT6_LDO2_EN	POFF_TSLOT6_LS2_EN	POFF_TSLOT6_LS1_EN	00
0x70	POFF_SEQ_TIME_SLOT7_H	R/W	POFF_TSLOT7_EN	POFF_TSLOT7_BUCK7_EN	POFF_TSLOT7_BUCK6_EN	POFF_TSLOT7_BUCK5_EN	POFF_TSLOT7_BUCK4_EN	POFF_TSLOT7_BUCK3_EN	POFF_TSLOT7_BUCK2_EN	POFF_TSLOT7_BUCK1_EN	80
0x71	POFF_SEQ_TIME_SLOT7_L	R/W	RSVD	POFF_TSLOT7_LDO6_EN	POFF_TSLOT7_LDO5_EN	POFF_TSLOT7_LDO4_EN	POFF_TSLOT7_LDO3_EN	POFF_TSLOT7_LDO2_EN	POFF_TSLOT7_LS2_EN	POFF_TSLOT7_LS1_EN	20
0x72	POFF_SEQ_TIME_SLOT8_H	R/W	POFF_TSLOT8_EN	POFF_TSLOT8_BUCK7_EN	POFF_TSLOT8_BUCK6_EN	POFF_TSLOT8_BUCK5_EN	POFF_TSLOT8_BUCK4_EN	POFF_TSLOT8_BUCK3_EN	POFF_TSLOT8_BUCK2_EN	POFF_TSLOT8_BUCK1_EN	00
0x73	POFF_SEQ_TIME_SLOT8_L	R/W	RSVD	POFF_TSLOT8_LDO6_EN	POFF_TSLOT8_LDO5_EN	POFF_TSLOT8_LDO4_EN	POFF_TSLOT8_LDO3_EN	POFF_TSLOT8_LDO2_EN	POFF_TSLOT8_LS2_EN	POFF_TSLOT8_LS1_EN	00
0x74	POFF_SEQ_TIME_SLOT9_H	R/W	POFF_TSLOT9_EN	POFF_TSLOT9_BUCK7_EN	POFF_TSLOT9_BUCK6_EN	POFF_TSLOT9_BUCK5_EN	POFF_TSLOT9_BUCK4_EN	POFF_TSLOT9_BUCK3_EN	POFF_TSLOT9_BUCK2_EN	POFF_TSLOT9_BUCK1_EN	00
0x75	POFF_SEQ_TIME_SLOT9_L	R/W	RSVD	POFF_TSLOT9_LDO6_EN	POFF_TSLOT9_LDO5_EN	POFF_TSLOT9_LDO4_EN	POFF_TSLOT9_LDO3_EN	POFF_TSLOT9_LDO2_EN	POFF_TSLOT9_LS2_EN	POFF_TSLOT9_LS1_EN	00
0x76	POFF_SEQ_TIME_SLOT10_H	R/W	POFF_TSLOT10_EN	POFF_TSLOT10_BUCK7_EN	POFF_TSLOT10_BUCK6_EN	POFF_TSLOT10_BUCK5_EN	POFF_TSLOT10_BUCK4_EN	POFF_TSLOT10_BUCK3_EN	POFF_TSLOT10_BUCK2_EN	POFF_TSLOT10_BUCK1_EN	00
0x77	POFF_SEQ_TIME_SLOT10	R/W	RSVD	POFF_TSLOT10_LDO6_EN	POFF_TSLOT10_LDO5_EN	POFF_TSLOT10_LDO4_EN	POFF_TSLOT10_LDO3_EN	POFF_TSLOT10_LDO2_EN	POFF_TSLOT10_LS2_EN	POFF_TSLOT10_LS1_EN	00
0x78	POFF_SEQ_TIME_SLOT11_H	R/W	POFF_TSLOT11_EN	POFF_TSLOT11_BUCK7_EN	POFF_TSLOT11_BUCK6_EN	POFF_TSLOT11_BUCK5_EN	POFF_TSLOT11_BUCK4_EN	POFF_TSLOT11_BUCK3_EN	POFF_TSLOT11_BUCK2_EN	POFF_TSLOT11_BUCK1_EN	00
0x79	POFF_SEQ_TIME_SLOT11_L	R/W	RSVD	POFF_TSLOT11_LDO6_EN	POFF_TSLOT11_LDO5_EN	POFF_TSLOT11_LDO4_EN	POFF_TSLOT11_LDO3_EN	POFF_TSLOT11_LDO2_EN	POFF_TSLOT11_LS2_EN	POFF_TSLOT11_LS1_EN	00

APW7720-00 MTP Register Map (Cont.)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7A	POFF_SEQ_TIME_SLOT12_H	R/W	POFF_TSLOT12_EN	POFF_TSLOT12_BUCK7_EN	POFF_TSLOT12_BUCK6_EN	POFF_TSLOT12_BUCK5_EN	POFF_TSLOT12_BUCK4_EN	POFF_TSLOT12_BUCK3_EN	POFF_TSLOT12_BUCK2_EN	POFF_TSLOT12_BUCK1_EN	00
0x7B	POFF_SEQ_TIME_SLOT12_L	R/W	RSVD	POFF_TSLOT12_LDO6_EN	POFF_TSLOT12_LDO5_EN	POFF_TSLOT12_LDO4_EN	POFF_TSLOT12_LDO3_EN	POFF_TSLOT12_LDO2_EN	POFF_TSLOT12_LS2_EN	POFF_TSLOT12_LS1_EN	00
0x7C	POFF_SEQ_TIME_SLOT13_H	R/W	POFF_TSLOT13_EN	POFF_TSLOT13_BUCK7_EN	POFF_TSLOT13_BUCK6_EN	POFF_TSLOT13_BUCK5_EN	POFF_TSLOT13_BUCK4_EN	POFF_TSLOT13_BUCK3_EN	POFF_TSLOT13_BUCK2_EN	POFF_TSLOT13_BUCK1_EN	00
0x7D	POFF_SEQ_TIME_SLOT13_L	R/W	RSVD	POFF_TSLOT13_LDO6_EN	POFF_TSLOT13_LDO5_EN	POFF_TSLOT13_LDO4_EN	POFF_TSLOT13_LDO3_EN	POFF_TSLOT13_LDO2_EN	POFF_TSLOT13_LS2_EN	POFF_TSLOT13_LS1_EN	00
0x7E ~ 0xFF	VENDOR_RSVD	R/W	RSVD								-

Note 7: Registers 0x14 to 0x1D, 0x35 to 0x36, and 0x7E to 0xFF are vendor-reserved registers. The System Management Controller (SMC) is prohibited from writing to these registers.

Register Description

VENDOR & REVISION ID Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x01	VENDOR_ID	VENDOR_ID				REVISION_ID				R	11h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:4]	VENDOR_ID	This is used to identify the Vendor ID.									0001
D[3:0]	REVISION_ID	The first stepping starts with '0000' and increment by 1 for each new metal layer stepping.									0001

OFF Mode Enable Register 0

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x02	OFF_MODE_EN_0	OFF_MODE	OFF_MODE_EN_BUCK7	OFF_MODE_EN_BUCK6	OFF_MODE_EN_BUCK5	OFF_MODE_EN_BUCK4	OFF_MODE_EN_BUCK3	OFF_MODE_EN_BUCK2	OFF_MODE_EN_BUCK1	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	OFF_MODE	OFF Mode Enable Bit. This bit can only be set when the PGOOD signal is high. 0 = Do not execute off mode (when a rising edge signal occurs on the WAKEUP pin, the OFF_MODE bit is automatically cleared to "0") 1 = Execute off mode. The operation mode of the DC/DC converter is converted to Auto Mode.									0
D[6]	OFF_MODE_EN_BUCK7	BUCK7 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[5]	OFF_MODE_EN_BUCK6	BUCK6 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[4]	OFF_MODE_EN_BUCK5	BUCK5 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[3]	OFF_MODE_EN_BUCK4	BUCK4 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[2]	OFF_MODE_EN_BUCK3	BUCK3 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[1]	OFF_MODE_EN_BUCK2	BUCK2 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0
D[0]	OFF_MODE_EN_BUCK1	BUCK1 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode									0

Register Description (Cont.)

OFF Mode Enable Register 1

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x03	OFF_MODE_EN_1	RSVD	OFF_MODE_EN_LDO6	OFF_MODE_EN_LDO5	OFF_MODE_EN_LDO4	OFF_MODE_EN_LDO3	OFF_MODE_EN_LDO2	OFF_MODE_EN_LS2_EN	OFF_MODE_EN_LS1_EN	R/W	00h

Bit	NAME	FUNCTION	DEFAULT
D[7]	RSVD	Reserved	0
D[6]	OFF_MODE_EN_LDO6	LDO6 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[5]	OFF_MODE_EN_LDO5	LDO5 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[4]	OFF_MODE_EN_LDO4	LDO4 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[3]	OFF_MODE_EN_LDO3	LDO3 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[2]	OFF_MODE_EN_LDO2	LDO2 regulator enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[1]	OFF_MODE_EN_LS2_EN	LS2_EN enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0
D[0]	OFF_MODE_EN_LS1_EN	LS1_EN enable bit in off mode 0 = Same as power off sequence; 1 = Still enable in off mode	0

Register Description (Cont.)

Regulator Control Register 0

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x04	REG_ CONTROL_0	RSVD	SD_ BUCK7	SD_ BUCK6	SD_ BUCK5	SD_ BUCK4	SD_ BUCK3	SD_ BUCK2	SD_ BUCK1	R/W	7Fh

Bit	NAME	FUNCTION	DEFAULT
D[7]	RSVD	Reserved	0
D[6]	SD_BUCK7	BUCK7 regulator shutdown bit 0 = BUCK7 is enabled; 1 = BUCK7 is disabled (BUCK7PG[0]=0)	1
D[5]	SD_BUCK6	BUCK6 regulator shutdown bit 0 = BUCK6 is enabled; 1 = BUCK6 is disabled (BUCK6PG[0]=0)	1
D[4]	SD_BUCK5	BUCK5 regulator shutdown bit 0 = BUCK5 is enabled; 1 = BUCK5 is disabled (BUCK5PG[0]=0)	1
D[3]	SD_BUCK4	BUCK4 regulator shutdown bit 0 = BUCK4 is enabled; 1 = BUCK4 is disabled (BUCK4PG[0]=0)	1
D[2]	SD_BUCK3	BUCK3 regulator shutdown bit 0 = BUCK3 is enabled; 1 = BUCK3 is disabled (BUCK3PG[0]=0)	1
D[1]	SD_BUCK2	BUCK2 regulator shutdown bit 0 = BUCK2 is enabled; 1 = BUCK2 is disabled (BUCK2PG[0]=0)	1
D[0]	SD_BUCK1	BUCK1 regulator shutdown bit 0 = BUCK1 is enabled; 1 = BUCK1 is disabled (BUCK1PG[0]=0)	1

Note 8: When PMIC exits shutdown mode (EN signal changes from low to high or PMIC is woken up), PMIC updates the REG_ CONTROL_0 register and the REG_CONTROL_1 register based on the power on sequence time slot register 0~13 settings.
Note 9: These bits can only be set when the PGOOD signal is high and have no effect on the PGOOD signal.
Note 10: Once any voltage regulator (including LS1_EN and LS2_EN) enters OFF mode, it cannot be re-enabled through the settings of the REG_CONTROL_0 or REG_CONTROL_1 registers.

Register Description (Cont.)

Regulator Control Register 1

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x05	REG_ CONTROL_1	RSVD	SD_LDO6	SD_LDO5	SD_LDO4	SD_LDO3	SD_LDO2	SD_LS2_ EN	SD_LS1_ EN	R/W	7Fh
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	RSVD	Reserved									0
D[6]	SD_LDO6	LDO6 regulator shutdown bit 0 = LDO6 is enabled; 1 = LDO6 is disabled (LDO6PG[0]=0)									1
D[5]	SD_LDO5	LDO5 regulator shutdown bit 0 = LDO5 is enabled; 1 = LDO5 is disabled (LDO5PG[0]=0)									1
D[4]	SD_LDO4	LDO4 regulator shutdown bit 0 = LDO4 is enabled; 1 = LDO4 is disabled (LDO4PG[0]=0)									1
D[3]	SD_LDO3	LDO3 regulator shutdown bit 0 = LDO3 is enabled; 1 = LDO3 is disabled (LDO3PG[0]=0)									1
D[2]	SD_LDO2	LDO2 regulator shutdown bit 0 = LDO2 is enabled; 1 = LDO2 is disabled (LDO2PG[0]=0)									1
D[1]	SD_LS2_EN	LS2_EN shutdown bit 0 = LS2_EN is enabled; 1 = LS2_EN is disabled									1
D[0]	SD_LS1_EN	LS1_EN shutdown bit 0 = LS1_EN is enabled; 1 = LS1_EN is disabled									1

Note 8: When PMIC exits shutdown mode (EN signal changes from low to high or PMIC is woken up), PMIC updates the REG_ CONTROL_0 register and the REG_CONTROL_1 register based on the power on sequence time slot register 0~13 settings.
Note 9: These bits can only be set when the PGOOD signal is high and have no effect on the PGOOD signal.
Note 10: Once any voltage regulator (including LS1_EN and LS2_EN) enters OFF mode, it cannot be re-enabled through the settings of the REG_CONTROL_0 or REG_CONTROL_1 registers.

Watchdog Control Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x06	WD_CNOTROL	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WDT_RST	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:1]	RSVD	Reserved									0000000
D[0]	WDT_RST	Watchdog timer reset bit. Write “1” to reset the watchdog timer when WDT_EN bit is enabled. 0 = Read 0 as usual, write 1 no effect; 1 = Write 1 to reset the watchdog timer (auto clear)									0

Note 11: When WDT_EN is enabled, write “1” to reset WDT_RST bit to reset watchdog timer, if watchdog timer is timeout, the PMIC will reset all registers (except the REG_CONTROL_0 and REG_CONTROL_1 registers) and auto reboot.

Register Description (Cont.)

Power Good Status Register: Monitor BUCK1~7 power good status and PGOOD status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x07	PG_BUCK_ STATUS	PGOOD	BUCK7PG	BUCK6PG	BUCK5PG	BUCK4PG	BUCK3PG	BUCK2PG	BUCK1PG	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	PGOOD	PGOOD Status 0 = Power Good 1 = Power Not Good									0
D[6]	BUCK7PG	BUCK7 power good indicator 0 = Power Good 1 = Power Not Good									0
D[5]	BUCK6PG	BUCK6 power good indicator 0 = Power Good 1 = Power Not Good									0
D[4]	BUCK5PG	BUCK5 power good indicator 0 = Power Good 1 = Power Not Good									0
D[3]	BUCK4PG	BUCK4 power good indicator 0 = Power Good 1 = Power Not Good									0
D[2]	BUCK3PG	BUCK3 power good indicator 0 = Power Good 1 = Power Not Good									0
D[1]	BUCK2PG	BUCK2 power good indicator 0 = Power Good 1 = Power Not Good									0
D[0]	BUCK1PG	BUCK1 power good indicator 0 = Power Good 1 = Power Not Good									0

Note 12: Write “1” to the BUCKxPG in PG_BUCK_STATUS register via I^2C to clear the BUCKx PG fault or write “1” to the PGOOD in PG_BUCK_STATUS register via I^2C to clear the BUCKx PG faults and the LDOx PG faults.

Power Good Status Register: Monitor LDO2~6 power good status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x08	PG_LDO_ STATUS	RSVD	RSVD	RSVD	LDO6PG	LDO5PG	LDO4PG	LDO3PG	LDO2PG	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:5]	RSVD	Reserved									000
D[4]	LDO6PG	LDO6 power good indicator 0 = Power Good 1 = Power Not Good									0
D[3]	LDO5PG	LDO5 power good indicator 0 = Power Good 1 = Power Not Good									0
D[2]	LDO4PG	LDO4 power good indicator 0 = Power Good 1 = Power Not Good									0
D[1]	LDO3PG	LDO3 power good indicator 0 = Power Good 1 = Power Not Good									0
D[0]	LDO2PG	LDO2 power good indicator 0 = Power Good 1 = Power Not Good									0

Note 13: Write “1” to the LDOxPG in PG_LDO_STATUS register via I^2C to clear the LDOx PG fault.

Register Description (Cont.)

Fault Status Register: Monitor BUCK1~7 regulator over-voltage status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x09	OV_BUCK_ STATUS	RSVD	BUCK7OV	BUCK6OV	BUCK5OV	BUCK4OV	BUCK3OV	BUCK2OV	BUCK1OV	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	RSVD	Reserved									0
D[6]	BUCK7OV	BUCK7 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[5]	BUCK6OV	BUCK6 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[4]	BUCK5OV	BUCK5 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[3]	BUCK4OV	BUCK4 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[2]	BUCK3OV	BUCK3 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[1]	BUCK2OV	BUCK2 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[0]	BUCK1OV	BUCK1 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0

Note 14: Write “1” to the BUCKxOV in OV_BUCK_STATUS register via I^2C to clear the BUCKx OV fault.

Fault Status Register: Monitor LDO2~6 regulator over-voltage status register.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0A	OV_LDO_ STATUS	RSVD	RSVD	RSVD	LDO6OV	LDO5OV	LDO4OV	LDO3OV	LDO2OV	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:5]	RSVD	Reserved									000
D[4]	LDO6OV	LDO6 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[3]	LDO5OV	LDO5 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[2]	LDO4OV	LDO4 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[1]	LDO3OV	LDO3 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0
D[0]	LDO2OV	LDO2 Output Over Voltage Status 0 = No Over Voltage 1 = Over Voltage									0

Note 15: Write “1” to the LDOxOV in OV_LDO_STATUS register via I^2C to clear the LDOx OV fault.

Register Description (Cont.)

Fault Status Register: Monitor BUCK1~7 regulator under-voltage status register.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0B	UV_BUCK_ STATUS	RSVD	BUCK7UV	BUCK6UV	BUCK5UV	BUCK4UV	BUCK3UV	BUCK2UV	BUCK1UV	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	RSVD	Reserved									0
D[6]	BUCK7UV	BUCK7 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[5]	BUCK6UV	BUCK6 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[4]	BUCK5UV	BUCK5 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[3]	BUCK4UV	BUCK4 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[2]	BUCK3UV	BUCK3 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[1]	BUCK2UV	BUCK2 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[0]	BUCK1UV	BUCK1 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0

Note 16: Write “1” to the BUCKxUV in UV_BUCK_STATUS register via I^2C to clear the BUCKx UV fault.

Fault Status Register: Monitor LDO2~6 regulator under-voltage status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0C	UV_LDO_ STATUS	RSVD	RSVD	RSVD	LDO6UV	LDO5UV	LDO4UV	LDO3UV	LDO2UV	R	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:5]	RSVD	Reserved									000
D[4]	LDO6UV	LDO6 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[3]	LDO5UV	LDO5 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[2]	LDO4UV	LDO4 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[1]	LDO3UV	LDO3 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0
D[0]	LDO2UV	LDO2 Output Under Voltage Status 0 = No Under Voltage 1 = Under Voltage									0

Note 17: Write “1” to the LDOxUV in UV_LDO_STATUS register via I^2C to clear the LDOx UV fault.

Register Description (Cont.)

Fault Status Register: Monitor VSYS over-voltage status and chip temperature status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0D	FAULT_STATUS	RSVD	RSVD	RSVD	RSVD	VSYSOV	TDIE_ ALARM	TDIE_ CRIT	TDIE_ NORMAL	R	01h

Bit	NAME	FUNCTION	DEFAULT
D[7:4]	RSVD	Reserved	0000
D[3]	VSYSOV (Note 18)	VSYS Over Voltage Status 0 = No Over Voltage 1 = Over Voltage	0
D[2]	TDIE_ALARM (Note 19)	Chip Temperature Alarm Status 0 = No Temperature Alarm 1 = Temperature Alarm (Chip temperature is over 125°C)	0
D[1]	TDIE_CRIT (Note 20)	Thermal Shutdown Status 0 = No Thermal Shutdown 1 = Thermal Shutdown	0
D[0]	TDIE_NORMAL	0 = Chip temperature is abnormal (Chip temperature > TSD threshold) 1 = Chip temperature is normal (Chip temperature < TSD threshold)	1

Note 18: To clear the VSYS over-voltage (OV) fault status, write “1” to the VSYSOV bit in the FAULT_STATUS register via I^2C.
Note 19: When the chip temperature falls below the temperature alarm threshold, write “1” to the TDIE_ALARM bit in the FAULT_STATUS register via I^2C to clear the chip temperature alarm fault status.
Note 20: The System Management Controller (SMC) can determine whether the chip temperature has returned to normal by checking if the TDIE_NORMAL bit is set to 1. To clear the thermal shutdown fault status, write “1” to the TDIE_CRIT bit in the FAULT_STATUS register via I^2C.

Register Description (Cont.)

BUCK1~7 Over Voltage Mask Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0E	OV_BUCK_MASK	RSVD	MBUCK7OV	MBUCK6OV	MBUCK5OV	MBUCK4OV	MBUCK3OV	MBUCK2OV	MBUCK1OV	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	RSVD	Reserved									0
D[6]	MBUCK7OV	Masks BUCK7 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[5]	MBUCK6OV	Masks BUCK6 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[4]	MBUCK5OV	Masks BUCK5 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[3]	MBUCK4OV	Masks BUCK4 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[2]	MBUCK3OV	Masks BUCK3 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[1]	MBUCK2OV	Masks BUCK2 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[0]	MBUCK1OV	Masks BUCK1 output over voltage IRQ 0 = Not Masked; 1 = Masked									0

LDO2~6 Over-Voltage Mask Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x0F	OV_LDO_MASK	RSVD	RSVD	RSVD	MLDO6OV	MLDO5OV	MLDO4OV	MLDO3OV	MLDO2OV	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:5]	RSVD	Reserved									000
D[4]	MLDO6OV	Masks LDO6 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[3]	MLDO5OV	Masks LDO5 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[2]	MLDO4OV	Masks LDO4 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[1]	MLDO3OV	Masks LDO3 output over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[0]	MLDO2OV	Masks LDO2 output over voltage IRQ 0 = Not Masked; 1 = Masked									0

Register Description (Cont.)

BUCK1~7 Under-Voltage Mask Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x10	UV_BUCK_MASK	RSVD	MBUCK7UV	MBUCK6UV	MBUCK5UV	MBUCK4UV	MBUCK3UV	MBUCK2UV	MBUCK1UV	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7]	RSVD	Reserved									0
D[6]	MBUCK7UV	Masks BUCK7 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[5]	MBUCK6UV	Masks BUCK6 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[4]	MBUCK5UV	Masks BUCK5 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[3]	MBUCK4UV	Masks BUCK4 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[2]	MBUCK3UV	Masks BUCK3 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[1]	MBUCK2UV	Masks BUCK2 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[0]	MBUCK1UV	Masks BUCK1 output under voltage IRQ 0 = Not Masked; 1 = Masked									0

LDO2~6 Under-Voltage Mask Register

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x11	UV_LDO_MASK	RSVD	RSVD	RSVD	MLDO6UV	MLDO5UV	MLDO4UV	MLDO3UV	MLDO2UV	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:5]	RSVD	Reserved									000
D[4]	MLDO6UV	Masks LDO6 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[3]	MLDO5UV	Masks LDO5 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[2]	MLDO4UV	Masks LDO4 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[1]	MLDO3UV	Masks LDO3 output under voltage IRQ 0 = Not Masked; 1 = Masked									0
D[0]	MLDO2UV	Masks LDO2 output under voltage IRQ 0 = Not Masked; 1 = Masked									0

Register Description (Cont.)

Fault Mask Register: This register is used to mask VSYS over voltage status, mask chip temperature alarm status, and mask critical temperature shutdown status.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x12	FAULT_MASK	RSVD	RSVD	RSVD	RSVD	RSVD	MVSYS_OV	MTDIE_ALARM	MTDIE_CRIT	R/W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:3]	RSVD	Reserved									00000
D[2]	MVSYS_OV	Masks VSYS over voltage IRQ 0 = Not Masked; 1 = Masked									0
D[1]	MTDIE_ALARM	Masks chip temperature alarm IRQ 0 = Not Masked; 1 = Masked									0
D[0]	MTDIE_CRIT	Masks critical temperature shutdown IRQ 0 = Not Masked; 1 = Masked									0

Fault Clear Register: When CLEAR in the FAULT_CLEAR register is written to “1”, all fault status are cleared, such as OV event, UV event, power good, etc.

ADDRESS	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x13	FAULT_CLEAR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CLEAR	W	00h
Bit	**NAME**	**FUNCTION**									**DEFAULT**
D[7:1]	RSVD	Reserved									0000000
D[0]	CLEAR	When this bit is written to “1” (auto-clear), all fault status including power good, output OV, output UV, VSYS OV, critical temperature shutdown, temperature alarm are cleared.									0

Application Information

Step-Down Converter Input Capacitor

The input capacitor can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic capacitors or tantalum capacitors, a high-quality ceramic capacitor (such as 1μF, 22μF in the application circuit) must be added and should be placed as close to the VIN pin as possible. This allows for optimal input voltage filtering and minimizes input voltage spikes that interfere with internal circuitry. It is recommended to use capacitors with X6S or X7R ceramic dielectrics as they are quite stable to temperature fluctuations.
When using ceramic capacitors on the input only, make sure they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple on the input. If the VIN voltage fluctuates significantly (for example, more than 5V ±5%), an appropriate electrolytic or tantalum capacitor must be added, such as the C_{BULK} capacitor shown in the application circuit.

Inductor Selection

For high efficiency, the inductor should have low DC resistance to minimize conduction losses. Especially at high switching frequencies, the core material has a greater impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductance value, the smaller the inductor ripple current, and the lower the conduction loss of the converter. Conversely, larger inductance values result in slower load transient response. A reasonable starting point for setting ripple current, ΔIL, is 30% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\times\Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

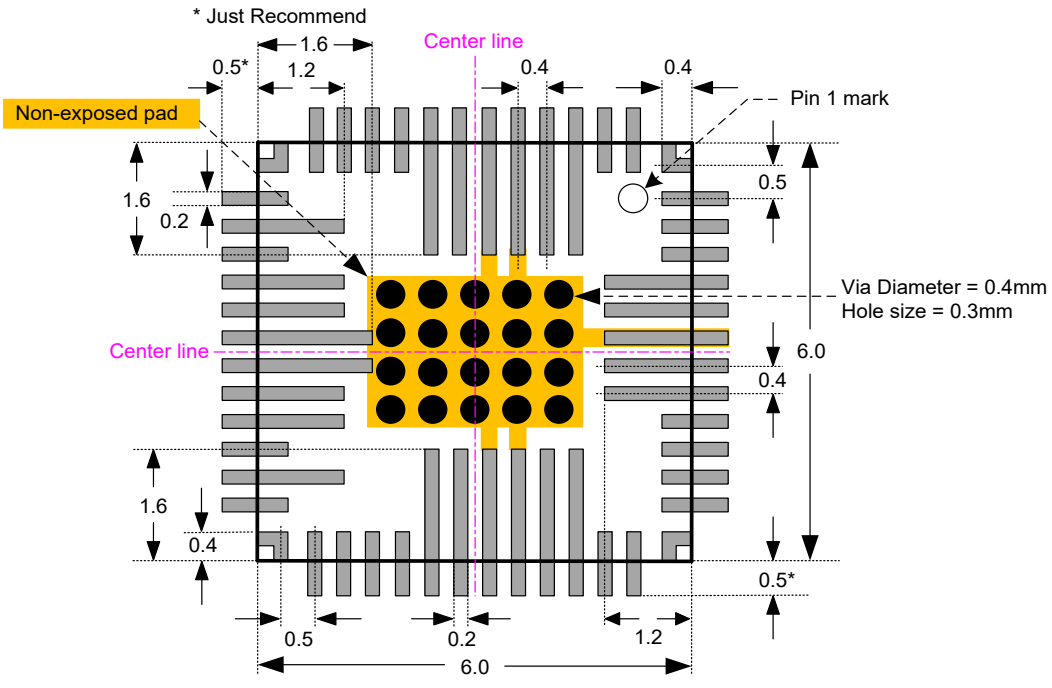
Application Information (Cont.)

Layout Consideration

For switching power supplies, layout is an important step in the design; especially at high peak currents and high switching frequencies. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. If the layout is not carefully done, the regulator might show noise issues and duty cycle jitter. Below is a checklist for your layout:

1. The VSYS decoupling capacitor must be placed close to the VSYS pin. Connect AGND to the negative terminal of the VSYS decoupling capacitor and to the large ground plane through a via. The AGND pin should not be connected directly to the ground plane through vias.
2. Place the inductor as close as possible to the corresponding LX pin (LX1 ~ LX7) to minimize copper traces and avoid coupling with other traces. Additionally, avoid using through-hole routing in the LX copper areas.
3. For two-phase applications, the PCB trace distance and width between LX1 and the positive pin of the output capacitor must be the same as the PCB trace distance and width between LX3 and the positive pin of the output capacitor.
4. Placing the output capacitor close to the load is beneficial to performance.
5. Use dedicated PCB traces to connect the FB1~FB7 pins to the positive terminal of their respective output capacitors. There should not be long traces between the output capacitors, as the resulting parasitic inductance and resistance will affect the stability of the COT regulator.
6. The trace from each power input pin (VIN1~VIN7) to the positive terminal of the decoupling capacitor should be as short and wide as possible. The trace from each PGND (PGND1~PGND7) pin to the negative terminal of the decoupling capacitor should be as short and wide as possible.
7. The ground of the output capacitor should be close to the ground of the input capacitor.
8. Use a wide copper plane to connect the input capacitor's ground to the output capacitor's ground, and place PGND vias (as many as possible) to minimize parasitic impedance.
9. Keep sensitive signal traces (such as FB1~FB7, SCL, SDA, etc.) away from high-frequency switching nodes. All sensitive PCB traces and components should be shielded with a ground plane.
10. Connect PGND1~PGND7 pad to a larger area of ground planes underneath with vias for proper heat dissipation. Place PGND vias (as many as possible and as close to PGND as possible) to minimize both parasitic impedance and thermal resistance.
11. Do not connect VINLDO2 directly to VIN6 using only PCB traces. The VINLDO2 (or VINLDO1) pad should be connected through a via to the larger VIN plane below.
12. Connect the VIN1~VIN7 pads to the larger VIN plane below through via holes, and increase the number of via holes as much as possible to reduce parasitic impedance.
13. Place the input capacitors of the VINLDO1 and VINLDO2 pins as close as possible to the pins.
14. The output capacitors of RTCLDO and LDO2~LDO6 pins are placed as close as possible to the pins.
15. Large current paths must have wide traces.

Recommended Minimum Footprint

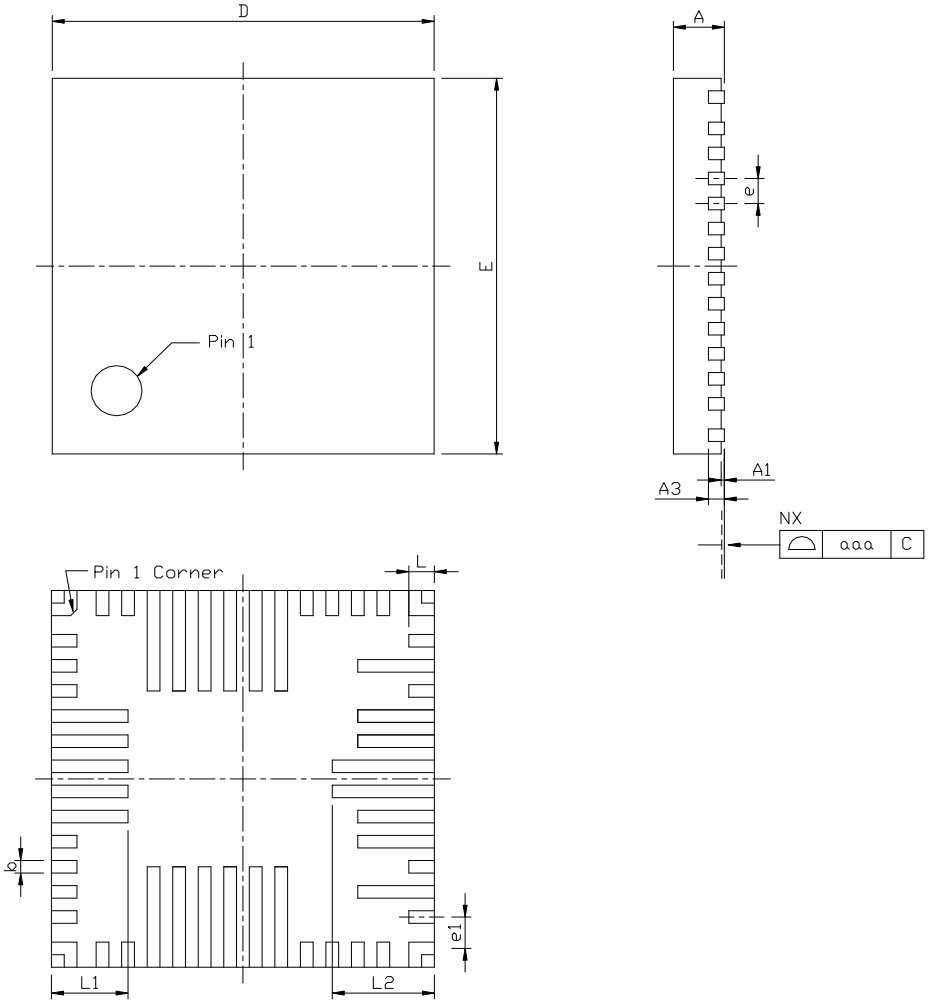


TQFN6x6-52B
(Top View)

Unit: mm

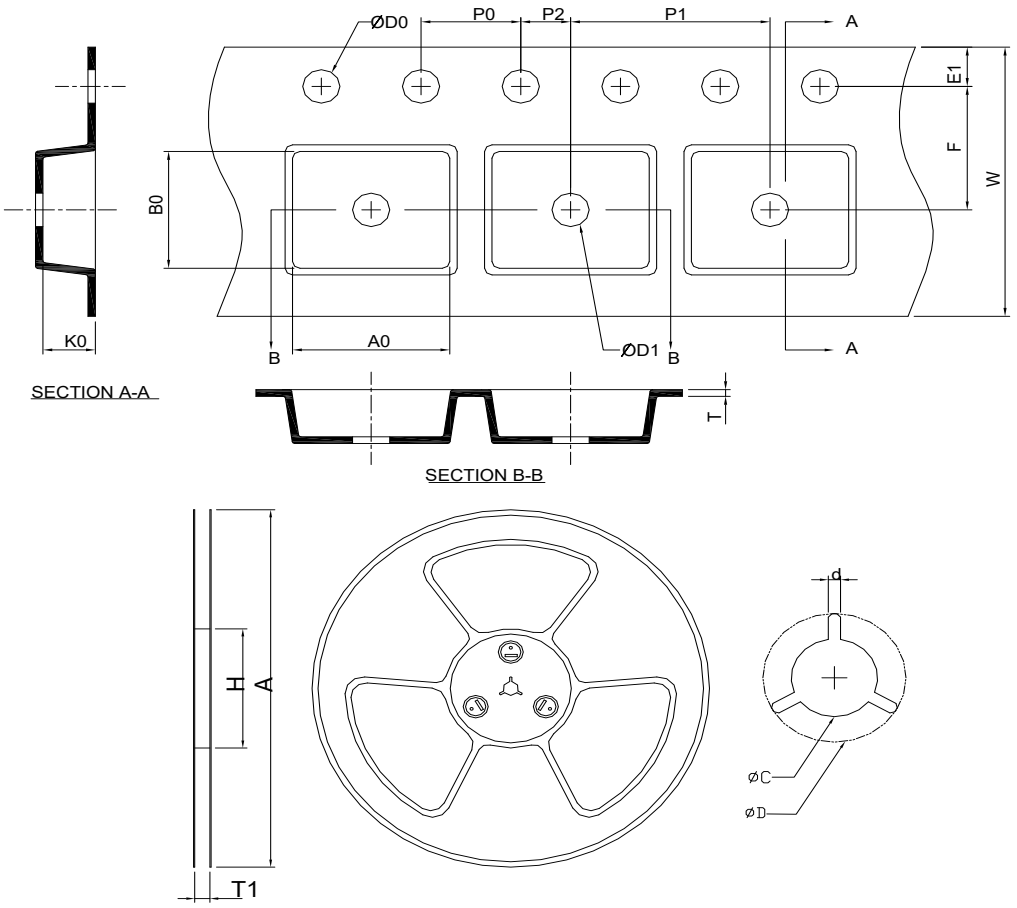
Package Information

TQFN6x6-52B



SYMBOL	TQFN6x6-52B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	5.90	6.10	0.232	0.240
E	5.90	6.10	0.232	0.240
e	0.40 BSC		0.016 BSC	
e1	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
L1	1.15	1.25	0.045	0.049
L2	1.55	1.65	0.061	0.065
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 6x6	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.30±0.20	6.30±0.20	1.00±0.20

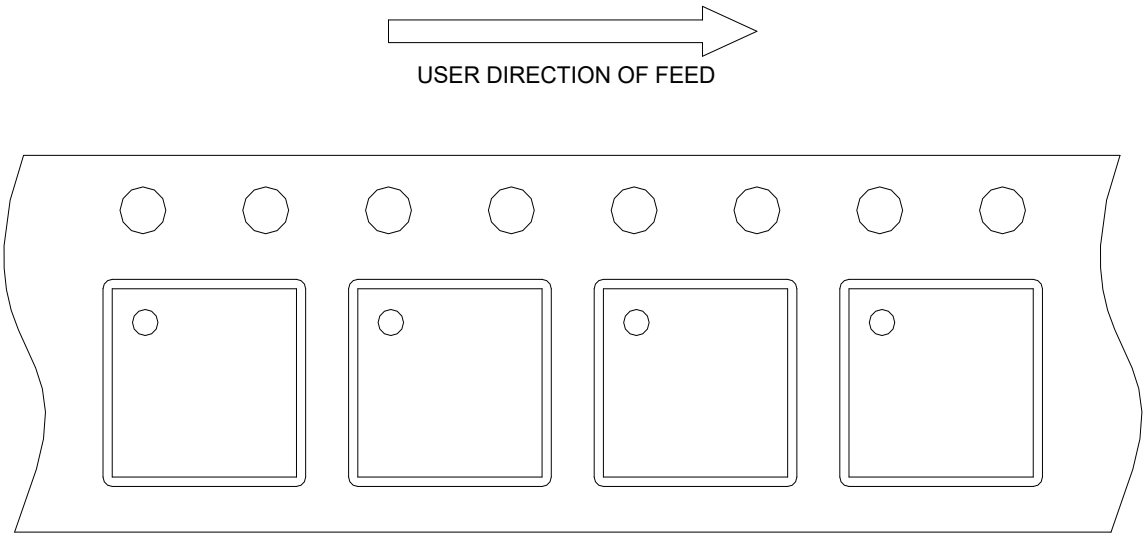
(mm)

Devices Per Unit

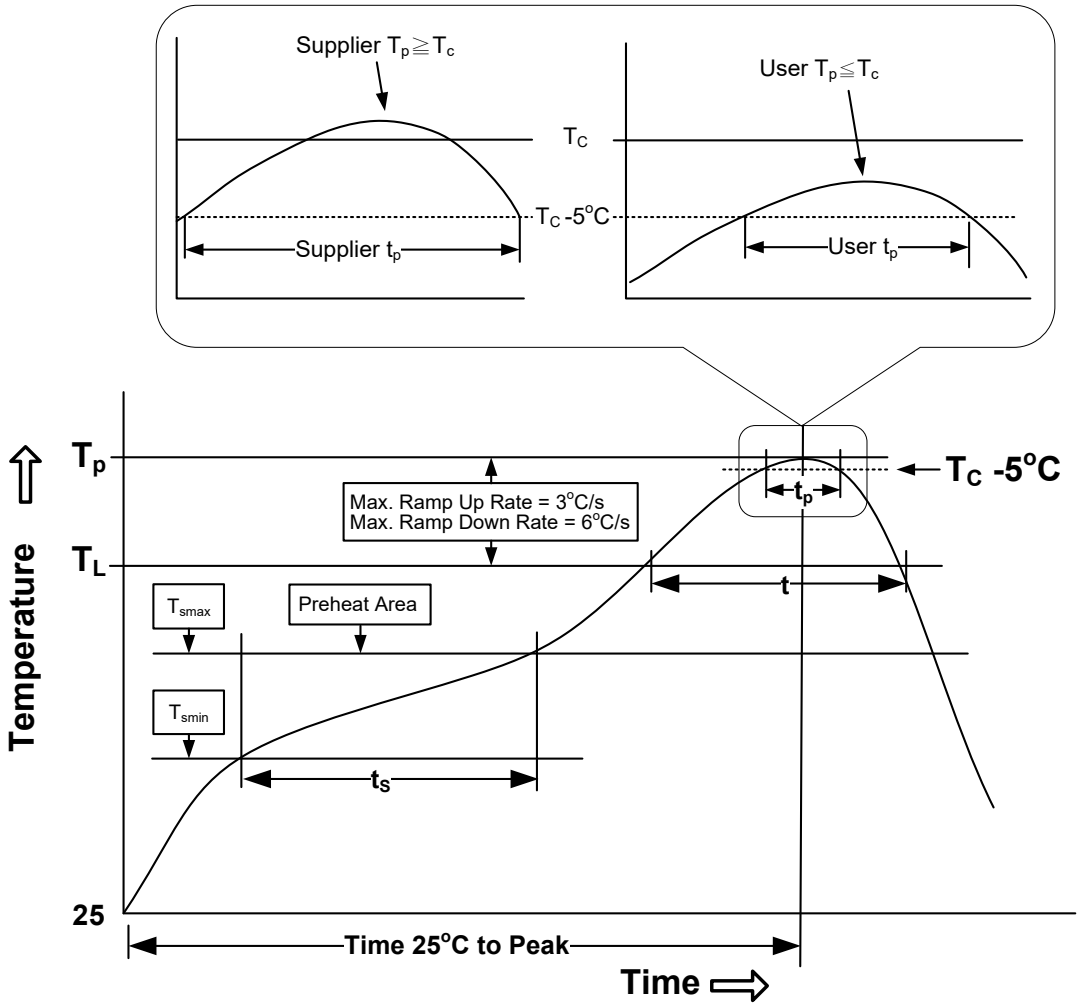
Package type	Packing	Quantity
TQFN 6x6	Tape & Reel	2500

Taping Direction Information

TQFN6x6-52B



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100°C 150°C 60-120 seconds	150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 9	See Classification Temp in table 10
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 9. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 10. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Duxing 1st Rd., East Dist.,
Hsinchu City 300096, Taiwan (R.O.C.)
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No.11, Ln. 218, Sec. 2, Zhongxing Rd., Xindian Dist.,
New Taipei City 231037, Taiwan (R.O.C.)
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838