HV Buck PWM Converter For LPDDR5

Features

- **Wide Operating Range from 4.5V to 24V Input Voltages**
- **Power-On-Reset Monitoring on VCC at 4.3V**
- **Support Dual Output VDD2 (8A), VDDQ (1A)**
- **Support Internal Power Sequency Control for Memory**
- **Built in Auto-PFM / Shutdown Control Schemes by EN Pin**
- **Built in DVFS Function by Mode Pin**
- **Built in Fixed Soft Start / Internal Stop Control**
- **Built in Over-Temperature Protection 160°C, hysteresis 25°C**
- **TQFN 4x4-32p**

HV 8A Buck Converter for VDD2

- **Built in Integrated Bootstrap Forward P-CH MOSFET**
- **Built in Integrated MOSFET H/S RDS (ON) 15mΩ & L/S RDS (ON) 8mΩ**
- **Selectable Switching Frequency by TON Pin**
- **Built in Open-Drain-Type POK function for PWM output**
- **UVP setting at 70% of VOUT & OVP setting at 125%**
- **Built in Current limit Protection using Low-side MOS sensing by CS setup**

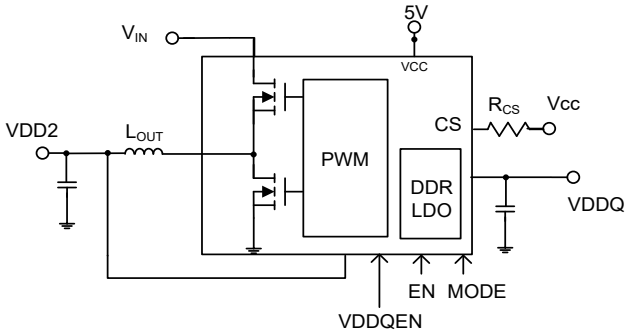
LV 1A LDO for VDDQ

- **Support VDDQ 1A output current**
- **Built in Individual Power On/Off Control by VDDQEN pin**
- **Built in Internal Soft-Start and Output Discharge**
- **Built in Current Limit Protection 1.5A (min.)**

Applications

- **LPDDR5 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Termination**

Simplified Application Circuit



General Description

The APW8863D integrates a synchronous buck PWM converter to generate VDD2, a sourcing and sinking LDO linear regulator to generate VDDQ. It offers the lowest total solution cost in system where space is at a premium.

The APW8863D provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8863D provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. On TQFN-32 Package, the Forced PWM Mode works nearly at constant frequency for low-noise requirements.

The APW8863D is equipped with accurate current-limit, output under-voltage, and output over-voltage protections. A Power-On- Reset function monitors the voltage on VCC prevents wrong operation during power on.

The LDO is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination.

The device integrates two power transistors to source and sink current up to 1A. It also incorporates current-limit and thermal shutdown protection.

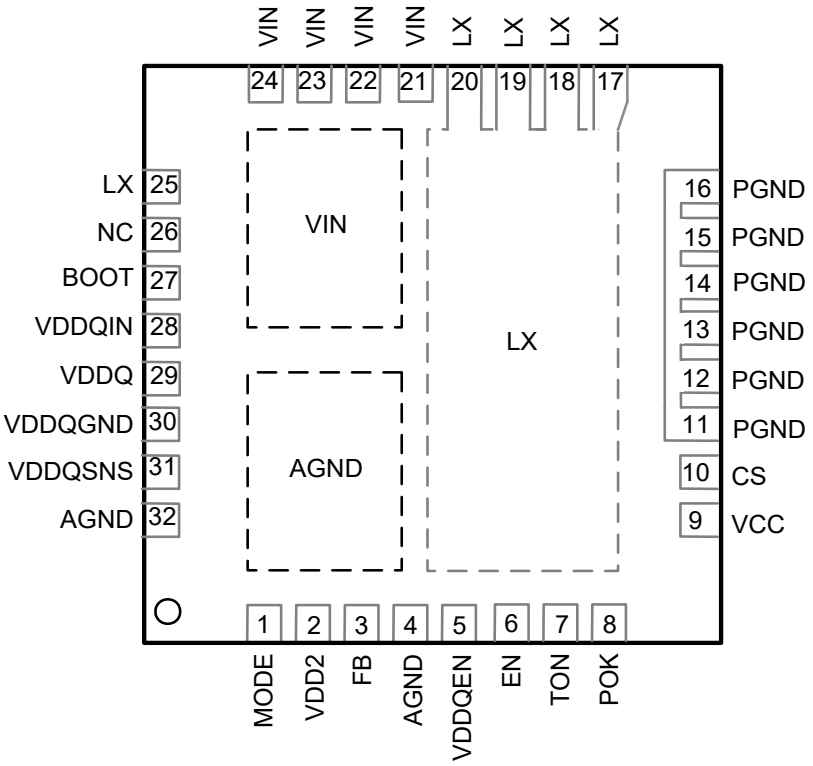
The output voltage of VDDQ (LDO) tracks the voltage at VDDQREF. The VDDQ output voltage is only requiring 20μF of ceramic output capacitance for stability and fast transient response. The VDDQEN and EN pins provide the sleep state for VDDQ (S3 state) and suspend state (S4/S5 state) for device, when EN and VDDQEN are both pulled low the device provides the soft-off for VDDQ.

Ordering and Marking Information

APW8863D □□ – □□□ Lead Free Code Handling Code Temperature Range Package Code	Package Code QB : TQFN 4x4-32 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Lead Free Code G : Green Part
APW8863D QB : 	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Pin Configuration



TQFN4x4-32
(Top View)

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to LX)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND) <20ns pulse width >20ns pulse width	 -5 ~ 40 -0.3 ~ 36	V
	LX Voltage (LX to GND) <20ns pulse width >20ns pulse width	 -8 ~ 36 -0.3 ~ 30	V
	PGND, VDDQGND to AGND Voltage	-0.3 ~ 0.3	V
	All Other Pins (CS, VDDQEN, EN, VDDQSNS, VDD2, VDDQIN, FB, POK, VDDQ, MODE to AGND)	-0.3 ~ 7	V
T_j	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient	48	°C/W
θ_{JC}	Thermal Resistance - Junction to Case	7	°C/W

Note 3: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{IN}	Converter Input Voltage	4.5 ~ 24	V
V_{VDD2}	Converter Output Voltage	0.9 ~2	V
V_{VDDQ}	LDO Output Voltage	0.3 ~ 0.5	V
I_{OUT}	Converter Output Current	0 ~ 8	A
I_{VDDQ}	LDO Output Current	-1A ~ +1A	A
C_{VCC}	VCC Capacitance	1~	µF
C_{VDDQ}	VDDQ Output Capacitance	20~80	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current	T_A=25°C, V_{VDDQEN}=V_{EN}=5V, no load, VCC Current	-	160	200	μA
I_{VCCSTB}	VCC Standby Current	T_A=25°C, V_{VDDQEN}=0V, V_{EN}=5V, no load, VCC Current	-	120	150	μA
I_{VCCSDN}	VCC Shutdown Current	T_A=25°C, V_{VDDQEN}=V_{EN}=0V, no load	-	0.1	1	μA
I_{VDDQIN}	VDDQIN Supply Current	T_A=25°C, V_{VDDQEN}=V_{EN}=5V, no load	-	1	10	μA
$I_{VDDQINSTB}$	VDDQIN Standby Current	T_A=25°C, V_{VDDQEN}=0V, V_{EN}=5V, no load	-	0.1	10	
$I_{VDDQINSDN}$	VDDQIN Shutdown Current	T_A=25°C, V_{VDDQEN}=V_{EN}=0V, no load	-	0.1	1	
POWER-ON-RESET						
	VCC POR Threshold	VCC Rising	4	4.3	4.45	V
	VCC POR Hysteresis		-	0.1	-	V
VDDQ OUTPUT (LDO)						
V_{VDDQ}	VDDQ Output Voltage	V_{VDDQIN}=V_{VDD2}=1.05V, R_{TOP}=11K, R_{GND}=10K	-	0.5	-	V
V_{VDDQ}	VDDQ Output Tolerance	V_{VDDQIN}=V_{VDD2}=1.05V, V_{VDD2}/2 - V_{VDDQ}, I_{VDDQ}=0A	-20	-	20	mV
		V_{VDDQIN}=V_{VDD2}=1.05V, V_{VDD2}/2 - V_{VDDQ}, I_{VDDQ}=±1A	-30	-	30	
T_{SSVTT}	VDDQ Soft Start Time	VDDQEN is go high to 0.95*VDDQ Regulation	5	15	22	us
I_{LIM}	Current-Limit	Sourcing Current (V_{VDDQIN}=1.05V) (V_{VDDQ}=0.5V) T_J=25°C	1.5	1.8	2.6	A
		Sinking Current (V_{VDDQIN}=1.05V) (V_{VDDQ}=0.5V) T_J=25°C	-2.6	-1.8	-1.2	
$R_{DS(ON)}$	VDDQ Power MOSFETs $R_{DS(ON)}$	Upper MOSFET	-	350	500	mΩ
		Lower MOSFET	-	350	500	
I_{VDDQLK}	VDDQ Leakage Current	V_{VDDQ}=1.25V, V_{VDDQEN}=0V, V_{EN}=5V, T_A=25°C	-1.0	-	1.0	μA
$I_{VDDQSNSLK}$	VDDQSNS Leakage Current	V_{VDDQ}=1.25V, T_A=25°C	-1.00	0.01	1.00	μA

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
VDD2 OUTPUT						
V_{VFB}	VFB Regulation Voltage	T_A=25°C	0.495	0.5	0.505	V
		T_A=-40°C to 85°C	0.4925	0.5	0.50575	V
		T_A=25°C, V_{VCC}=4.5V to 5.5V, V_{IN}=4.5V to 24V	-0.1	-	+0.1	%
		T_A=25°C, Load =0 to 8A, V_{VCC}=4.5V to 5.5V	-1	-	+1	%
	VFB Input Current	V_{VFB}=5V	-0.1	-	+0.1	μA
	VDD2 Discharge Current	V_{VDDQEN}=V_{EN}=0V, $V_{VDD2SNS}$=0.5V	15	25	-	mA
PWM CONTROLLERS						
F_{SW}	Operating Frequency	Adjustable Frequency	400	-	600	KHz
T_{SS}	Internal Soft Start Time	EN is High to 0.9*V_{OUT} Regulation	-	1.2	-	ms
T_{ONF}	Fast on time	V_{IN}=19V, V_{VDD2}=1.05V, R_{TON}=470KΩ	90	109	120	ns
$T_{OFF(MIN)}$	Minimum off time		-	300	-	ns
$T_{ON(MIN)}$	Slow on time		-	50	-	ns
	Zero-Crossing Threshold		-10	-0.5	10	mV
VDD2 PROTECTIONS						
	CS Pin Sink Current	T_A=25°C	15	17	22	μA
		Temperature Coefficient, On The Basis of 25°C	-	4500	-	ppm/°C
	OCP Comparator Offset	(V_{VCC} – V_{CS}) – (V_{LX} – PGND), V_{VCC} – V_{CS}=60mV	-21	0	21	mV
	VDD2 OVP Trip Threshold	V_{VDD2} Rising	117	125	130	%
	VDD2 OVP Debounce Delay	V_{FB} Rising, DV=10mV	-	3	-	μs
	VDD2 UVP Trip Threshold	V_{VDD2} Falling	60	70	80	%
	VDD2 UVP Trip Hysteresis		-	3	-	%
POK						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	84	90	93	%
		POK in from Higher (POK Goes High)	117	125	130	%
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1.0	μA
	POK Sink Current	V_{POK}=0.3V	2.5	7.5	-	mA
	POK Debounce Time		-	5	-	μs
	POK Soft Start Time	EN is High to POK Ready	-	2	-	ms
GATE DRIVERS						
$R_{ON(H)}$	High Side N-MOSFET $R_{DS(ON)}$		-	15	17	mΩ
$R_{ON(L)}$	Low Side N-MOSFET $R_{DS(ON)}$		-	8	12	mΩ
T_D	Dead Time	(Note 4)	-	20	-	ns
BOOTSTRAP DIODE						
	Forward Voltage	V_{VCC} – V_{BOOT}, I_F=10mA, T_A=25°C	-	0.1	0.3	V
	Reverse Leakage	V_{BOOT}=30V, V_{LX}=25V, V_{VCC}=5V, T_A=25°C	-	-	0.5	μA

Electrical Characteristics (Cont.)

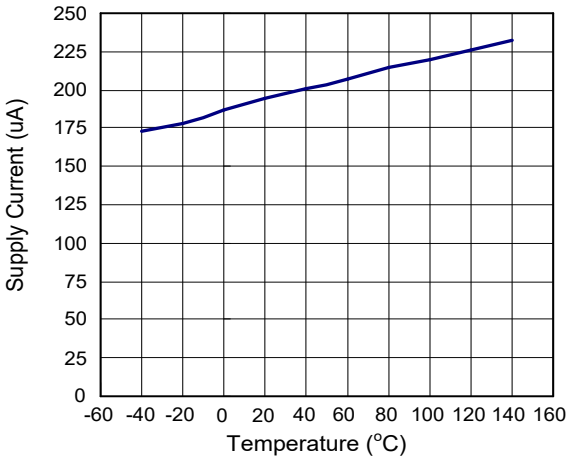
Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Specification			Unit
			Min.	Typ.	Max.	
LOGIC THRESHOLD						
V_{IH}	VDDQEN, EN and MODE High Threshold Voltage	VDDQEN, EN and MODE Rising	1.6	-	-	V
V_{IL}	VDDQEN, EN Low Threshold Voltage	VDDQEN, EN and MODE Falling	-	-	0.3	V
I_{ILEAK}	Logic Input Leakage Current	V_{VDDQEN}=V_{EN}=5V, T_A=25°C	-1	-	1	μA
THERMAL SHUTDOWN						
TSD	Thermal Shutdown Temperature	T_J Rising	-	160	-	°C
	Thermal Shutdown Hysteresis		-	25	-	°C

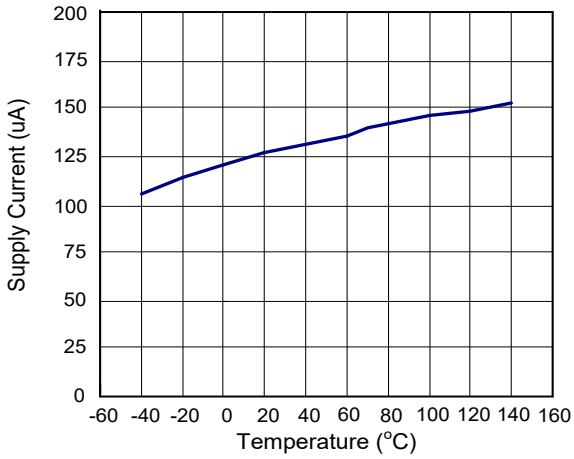
Note 4: Guaranteed by design.

Typical Operating Characteristics

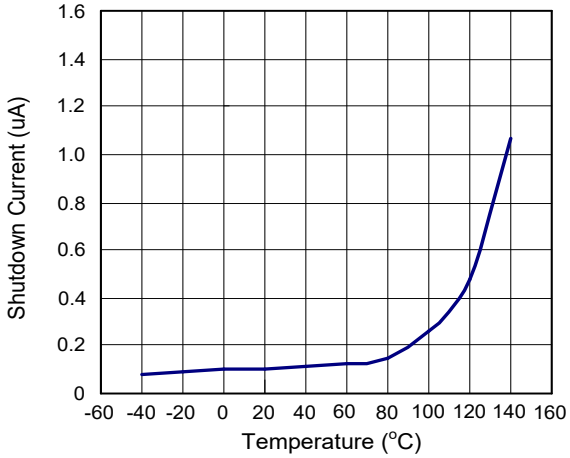
Supply Current In S0 VS Temperature



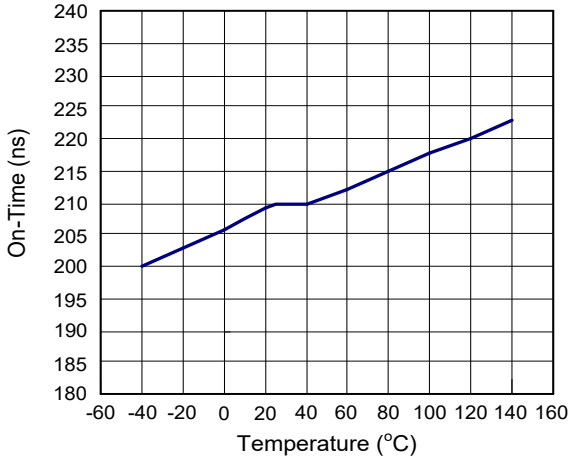
Supply Current In S3 VS Temperature



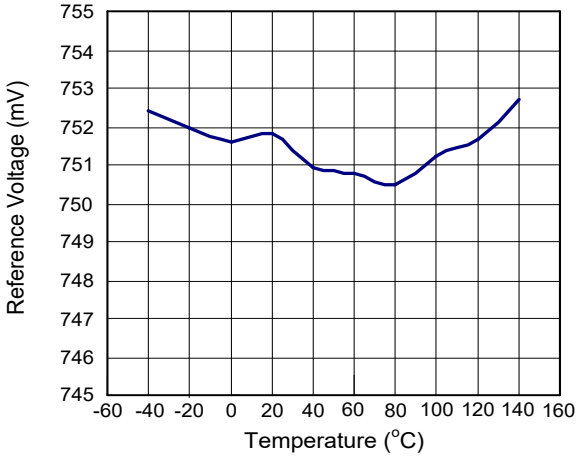
Shutdown Current VS Temperature



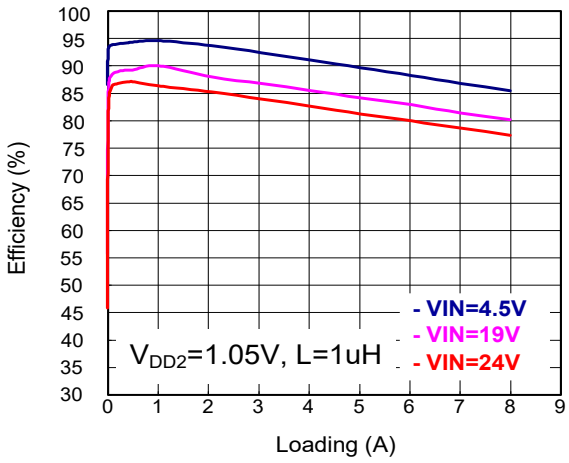
On-Time VS Temperature



Reference Voltage VS Temperature

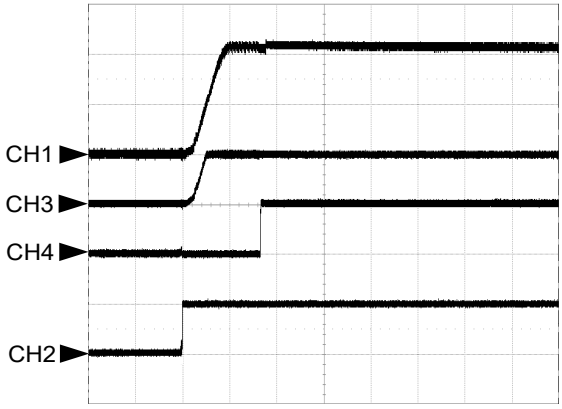


Efficiency VS Loading



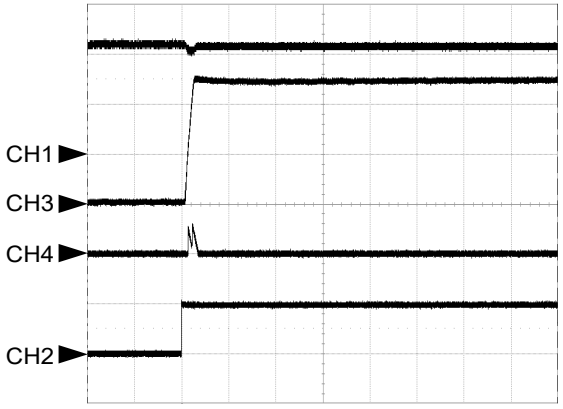
Operating Waveforms

Enable VCC - No Load



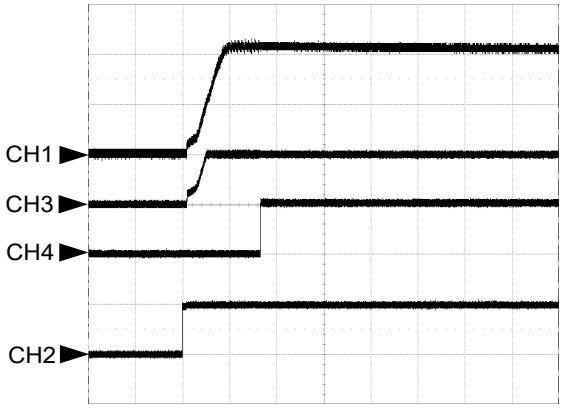
CH1: V_{VDD2}-500mV/div
CH2: V_{VCC}-5V/div
CH3: V_{VDDQ}-500mV/div
CH4: V_{POK}-5V/div
Time: 1ms/div

Enable VDDQEN – No Load



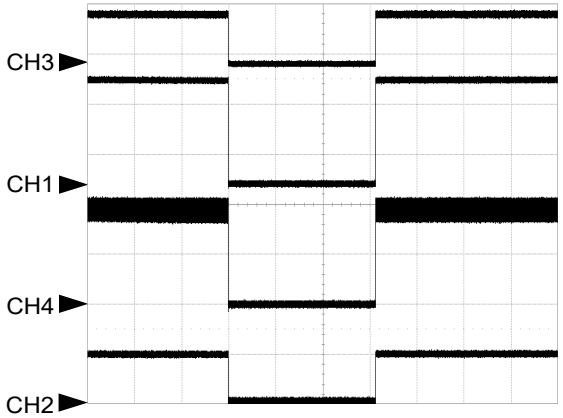
CH1: V_{VDD2}-500mV/div
CH2: V_{VDDQEN}-5V/div
CH3: V_{VDDQ}-200mV/div
CH4: I_L-5A/div
Time: 20us/div

POK- Enable EN/VDDQEN



CH1: V_{VDD2}-500mV/div
CH2: V_{VCC}-5V/div
CH3: V_{VDDQ}-500mV/div
CH4: V_{POK}-5V/div
Time: 1ms/div

OTP



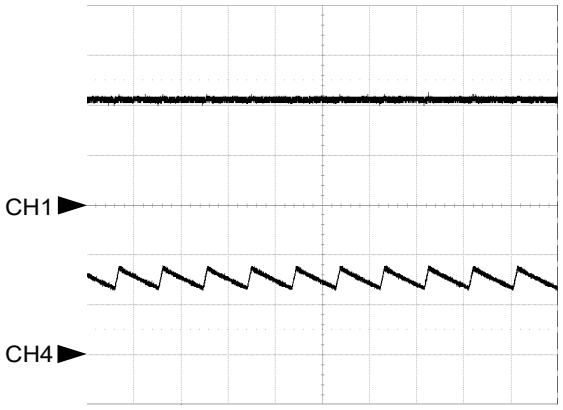
CH1: V_{VDD2}-500mV/div
CH2: V_{POK}-5V/div
CH3: V_{VDDQ}-500mV/div
CH4: I_L-5A/div
Time: 500ms/div

Operating Waveforms (Cont.)

UVP

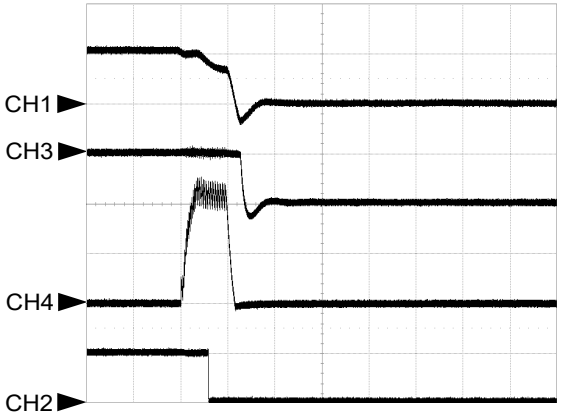
CH1: V_{VDD2}-500mV/div
CH2: V_{POK}-5V/div
CH3: V_{VDDQ}-500mV/div
CH4: I_L-5A/div
Time: 50us/div

Normal Operaion



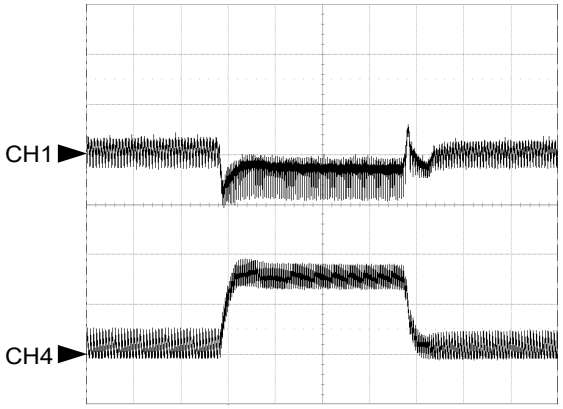
CH1: V_{VDD2}-500mV/div
CH4: I_L-5A/div
Time: 2us/div

OCP



CH1: V_{VDD2}-1V/div
CH2: V_{POK}-5V/div
CH1: V_{VDDQ}-500mV/div
CH4: I_L-5A/div
Time: 50us/div

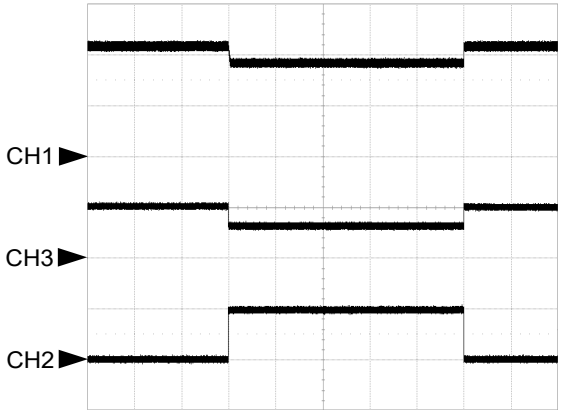
Load Transient-Load=0.8A<-->8A



CH1: V_{VDD2}-50mV/div
CH4: I_L-5A/div
Time: 50us/div

Operating Waveforms (Cont.)

Mode H/L

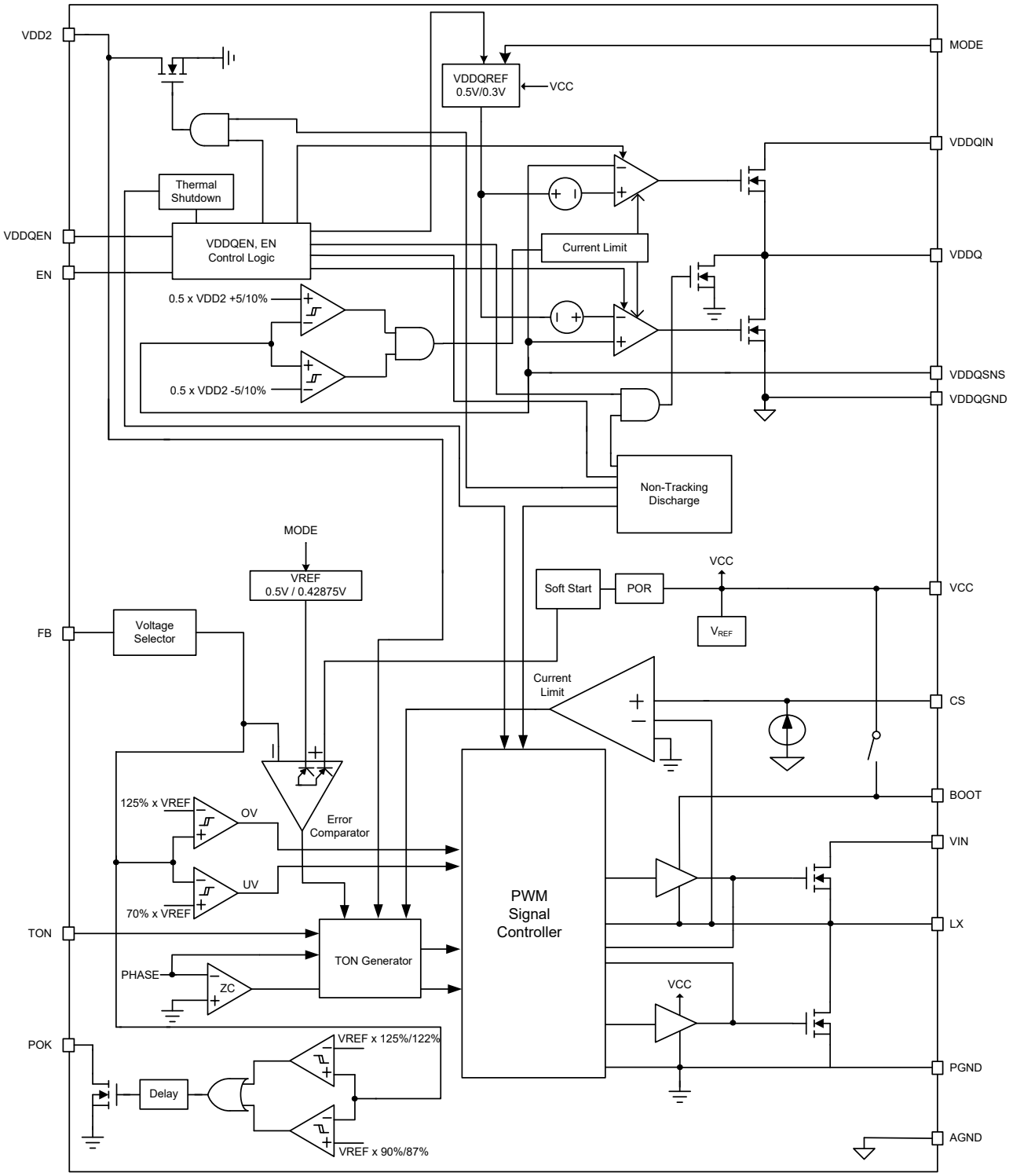


CH1: V_{VDD2}-500mV/div
CH2: V_{POK}-5V/div
CH3: V_{VDDQ}-500mV/div
Time: 2ms/div

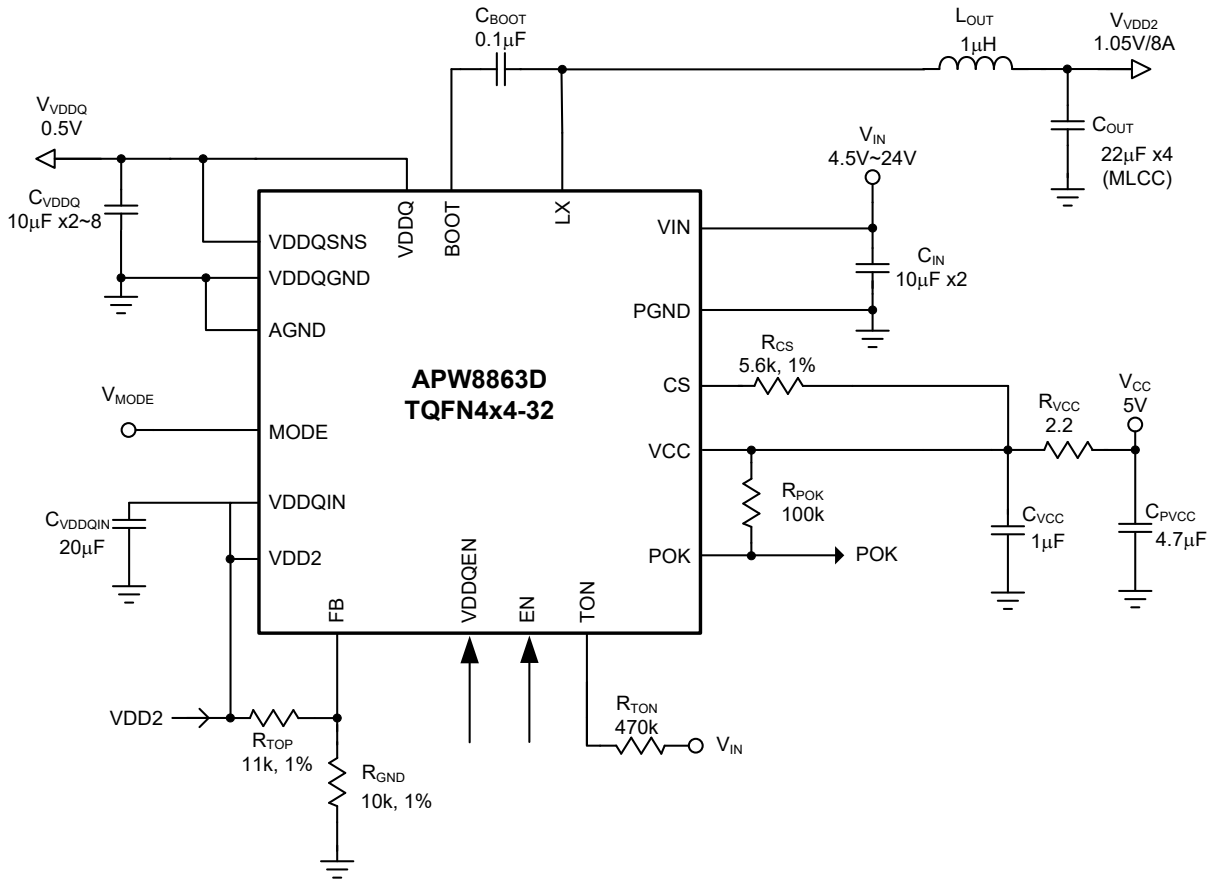
Pin Descriptions

NO. TQFN-32	NAME	FUNCTION
1	MODE	The mode pin is control output voltage of VDD2 and VDDQ. This pin is can be floating.
2	VDD2	VDD2 reference input for TON. Discharge current sinking terminal for VDD2 non-tracking discharge.
3	VFB	VDD2 output voltage setting pin.
4, 32	AGND	Signal Ground.
5	VDDQEN	VDDQEN signal input This pin can not floating.
6	EN	EN signal input. This pin can not floating.
7	TON	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{TON}=100KΩ ~ 600KΩ from TON pin to VIN pin.
8	POK	Power-good output pin. POK is an open drain output used to Indicate the status of the output voltage. When VDD2 output voltage is within the target range, it is in high state.
9	VCC	5V power supply voltage input pin for both internal control circuitry and low-side MOSFET gate driver.
10	CS	Over-current trip voltage setting input for $R_{DS(ON)}$ current sense scheme if connected to VCC through the voltage setting resistor.
11, 12, 13, 14, 15, 16	PGND	Power ground of the low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET.
17, 18, 19, 20, 25	LX	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. LX serves as the lower supply rail for the high-side gate driver.
21, 22, 23, 24	VIN	The pin is supply input.
26	NC	-
27	BOOT	Supply Input for the High-Side Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
28	VDDQIN	Supply voltage input for the VDDQ (LDO).
29	VDDQ	Power output for the VDDQ (LDO).
30	VDDQGND	Power ground output for the VDDQ (LDO).
31	VDDQSNS	Voltage sense input for the VDDQ (LDO). Connect to plus terminal of the VDDQ (LDO) output capacitor.

Block Diagram



Typical Application Circuit



Note 5: The VDDQ output ceramic capacitors is just recommend. in addition; R_{TOP} / R_{GND} suggest to less than 20K ohm is better.

Adjustable Output Voltage Regulator for VDD2

Function Description

The APW8863D integrates a synchronous buck PWM controller to generate VDD2, a sourcing and sinking LDO linear regulator to generate VDDQ. It provides a complete power supply for LPDDR5 memory system in a 32-pin TQFN package. User defined output voltage is also possible and can be adjustable from 0.9V to 2V. Input voltage range of the PWM converter is 4.5V to 24V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA.

The VDDQ LDO can source and sink up to 1A peak current with only 20μF ceramic output capacitor. The LDO input can be separated from VDD2 and optionally connected to a lower voltage by using VDDQIN pin. This helps reducing power dissipation in sourcing LX. The APW8863D is fully compatible to JEDEC LPDDR5 specifications at VDDQEN/EN sleep state (see Table 1). When both VDDQ and VDD2 are disabled, the non-tracking discharge mode discharges outputs using internal discharge MOSFETs that are connected to VDD2 and VDDQ.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on LX pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.3V typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 3.9V (typical), the POR disables the chip.

Soft-Start

The APW8863D integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows VDD2 soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1.2ms (typical) and independent of the LX switching frequency.

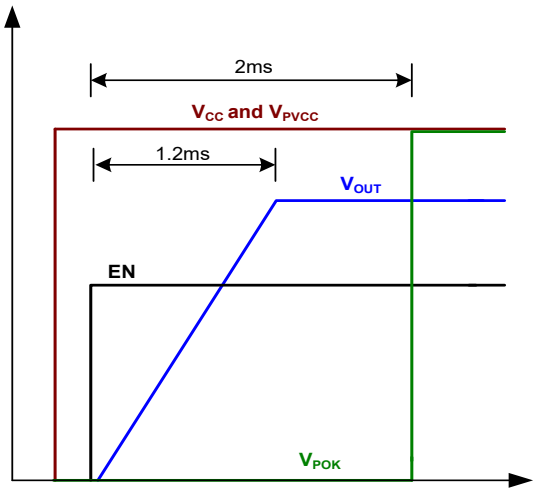


Figure 1. Soft-Start Sequence

During soft-start stage before the POK pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the internal digital soft start voltage equal the internal feedback voltage. This will ensure the output voltage starts from its existing voltage level.

The VDDQ LDO part monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VDDQ to GND or VDDQIN) conditions.
The VDDQ LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the VDDQ cannot start successfully.
APW8863D has an independent counter for each output, but the POK signal indicates only the status of VDD2 and does not indicate VDDQ power good externally.

Function Description (Cont.)

Power-Good Output (POK)

POK is an open-drain output and the POK comparator continuously monitors the output voltage. POK is actively held low in shutdown, and standby. When PWM converter's output voltage is greater than 95% of its target value, the internal open-drain device will be pulled low. After 63μs debounce time, the POK goes high. The POK goes low if V_{VDD2} output is 10% below or above its nominal regulation point.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after 2ms of PWM operations to ensure startup. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (70% of normal output voltage), APW8863D shuts down the output gradually and latches off both high and low side MOSFETs.

Over Voltage Protection (OVP)

The feedback voltage should increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over voltage protection comparator designed with a 1.5μs noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse.

When the OVP occurs, the POK pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, toggling VCC power-on-reset signal can only reset it.

PWM Converter Current Limit

The current-limit circuit employs a unique "valley" current sensing algorithm (Figure 2). CS pin should be connected to VCC through the trip voltage-setting resistor, R_{CS}. CS terminal sinks 5μA current, I_{CS}, and the current limit threshold is set to the voltage across the R_{CS}. The voltage between or AGND pin and LX pin monitors the inductor current so that LX pin should be connected to the drain terminal of the low side MOSFET. PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low side MOSFET.

If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage. The equation for the current limit threshold is as follows:

$$I_{LIMIT} = \frac{R_{CS} \times I_{CS}}{R_{DS(ON)}} + \frac{(V_{IN} - V_{VDDQ})}{2 \times L \times f_{SW}} \times \frac{V_{VDDQ}}{V_{IN}}$$

Where I_{LIMIT} is the desired current limit threshold, R_{CS} is the value of the current sense resistor connected to CS and VCC pins V_{CS} is the voltage across the R_{CS} resistor I_{RIPPLE} is inductor peak to peak current F_{SW} is the PWM switching frequency.

In a current limit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. If the output voltage becomes less than power good level, the V_{CS} is cut into half and the output voltage tends to be even lower. Eventually, it crosses the under voltage protection threshold and shutdown.

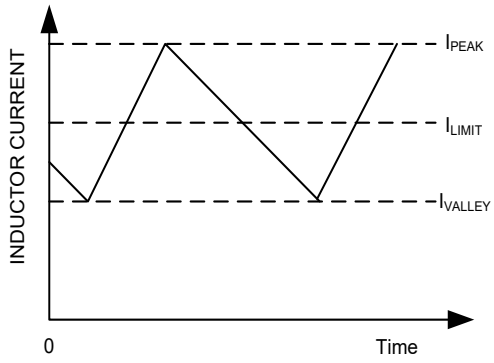


Figure 2. Current Limit Algorithm

VDDQ Sink/Source Regulator

The output voltage at VDDQ pin tracks the reference voltage applied at MODE pin. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VVDDQIN pin or sinking current to GND pin. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers.

Function Description (Cont.)

VDDQEN, EN Control

In the LPDDR5 memory applications, it is important to keep VDD2 always higher than VDDQ including both start-up and shutdown. The VDDQEN and EN signals control the VDDQ, VDD2 states and these pins should be connected to VDDQEN and EN signals respectively. The table1 shows the truth table of the VDDQEN and EN pins.
When both VDDQEN and EN are above the logic threshold voltage, the VDDQ and VDD2 are turned on at S0 state. When VDDQEN is low and EN is high, the VDD2 is kept on while the VDDQ voltage is disabled and left high impedance in VDDQEN state. When both VDDQEN and EN are low, the VDDQ and VDD2 are turned off and discharged to the ground.

Table1. The Truth Table of VDDQEN and EN pins

STATE	VDDQEN	EN	VDD2	VDDQ
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW8863D. When the junction temperature exceeds +160°C, PWM converter, VDDQ (LDO) are shut off, allowing the device to cool down. The regulator regu-lates the output again through initiation of a new soft-start cycle after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 25°C hysteresis lowers the average junction temperature during con-tinuous thermal overload conditions, extending life time of the device. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Programming the On-Time Control and PWM Switching Frequency

The APW8863D does not use a clock signal to produce PWM. The device uses the constant on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage V_{OUT} and inverse proportional to input voltage V_{IN}. In PWM, the on-time calculation is written as below equation.

$$T_{ON} = 6.3\times10^{-12}\times R_{TON}\left[\frac{\frac{2}{3}\times V_{VDDQ}}{V_{IN}}\right]$$

Where:
R_{TON} is the resistor connected from TON pin to LX pin. Furthermore, the approximate PWM switching frequency is written as:

$$T_{ON} = \frac{D}{F_{SW}} = F_{SW} = \frac{V_{OUT}/V_{IN}}{T_{ON}}$$

Where:
F_{SW} is the PWM switching frequency
APW8863D doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring V_{LX} voltage as input voltage to calculate on-time when the high-side MOSFET is turned on. And then, use the relationship between on-time and duty cycle to obtain the switching frequency.

Mode Function

The mode pin is control output voltage of VDD2 and VDDQ. If need to decrease output voltage of VDD2 and VDDQ then mode pin is pull high voltage or connect to more than 180K resistance. on the contrary; the output voltage of VDD2 and VDDQ was to high output voltage then mode pin is pull low voltage or connect to less than 30K resistance. In addition; This pin is can be floating.

Application Information

Output Voltage Selection

PWM can be also adjusted from 0.9V to 2V with a resistor-driver at FB between VDD2 and GND. Using 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.5V. Take the example, the output voltage of PWM is determined by:

$$V_{OUT} = 0.5 \times \left[1 + \frac{R_{TOP}}{R_{GND}}\right]$$

Where R_{TOP} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook applications, ceramic capacitors are recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Application Information (Cont.)

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

- Keep the switching nodes (BOOT, and LX) away from sensitive small signal nodes (FB and CS) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The VDDQIN is closed to VDD2 output, the connect VDDQIN and VDD2 output is short and wide trace. If other power is used as VDDQIN, the ceramic decoupling capacitor is closed to VDDQIN.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current limit stetting resistor should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the VDD2 and VDDQ output capacitors should be located right across their output pin as close as possible to the part to minimize parasitic. The input capacitor GND should be close to the output capacitor GND.
- It (VIN and LX nodes) should be a large plane for heat sinking.
- The APW8863D used ripple mode control. Build the resistor divider close to the FB pin so that the high impedance trace is shorter. And the FB pin traces can't be closed to the switching signal traces (BOOT, and LX).

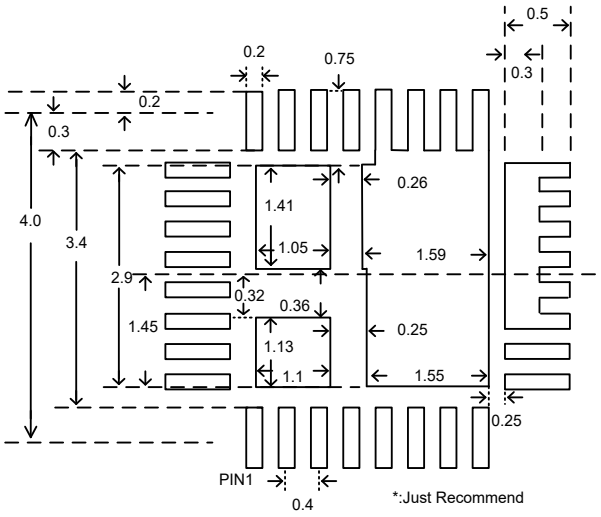
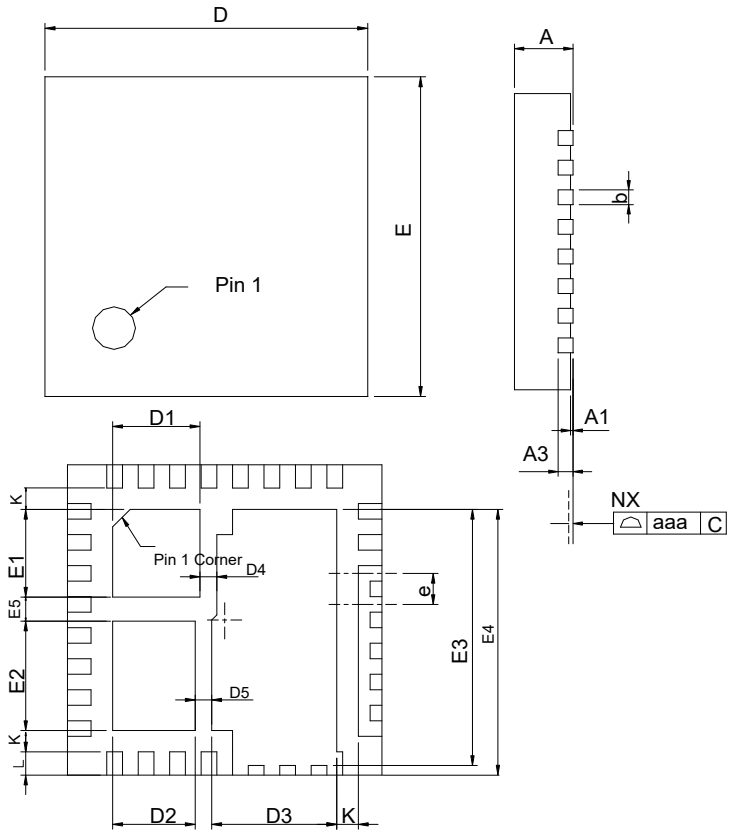


Figure 3. Recommended Minimum Footprint

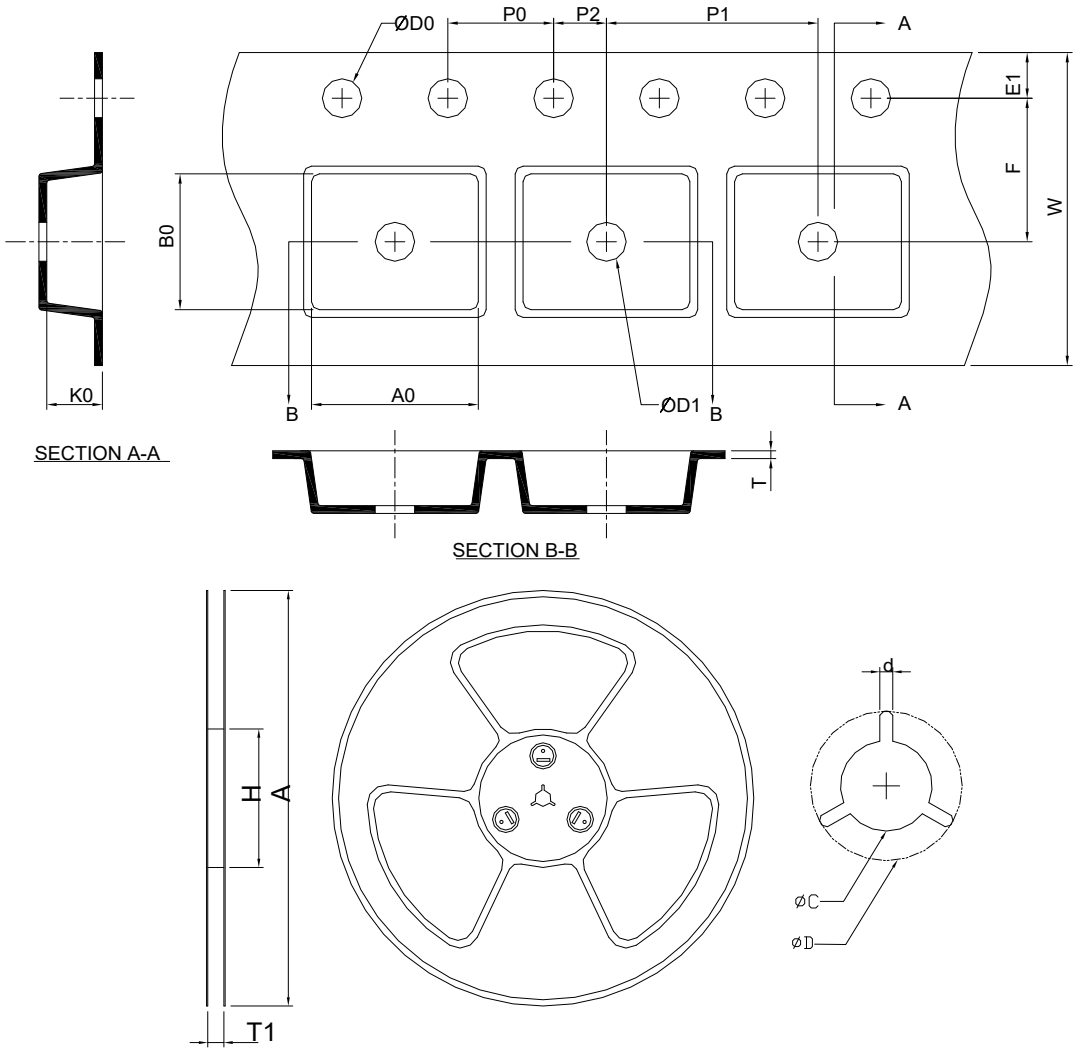
Package Information

TQFN4x4-32



SYMBOL	TQFN4*4-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	3.90	4.10	0.154	0.161
D1	1.01	1.21	0.040	0.048
D2	0.95	1.15	0.037	0.045
D3	1.49	1.69	0.059	0.067
D4	0.25 REF		0.010 REF	
D5	0.26 REF		0.010 REF	
E	3.90	4.10	0.154	0.161
E1	1.03	1.23	0.041	0.048
E2	1.31	1.51	0.052	0.059
E3	3.20	3.40	0.126	0.134
E4	3.45 REF		0.136 REF	
E5	0.36 REF		0.014 REF	
e	0.4 BSC		0.016 BSC	
L	0.25	0.35	0.010	0.014
K	0.24	0.26	0.009	0.010
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

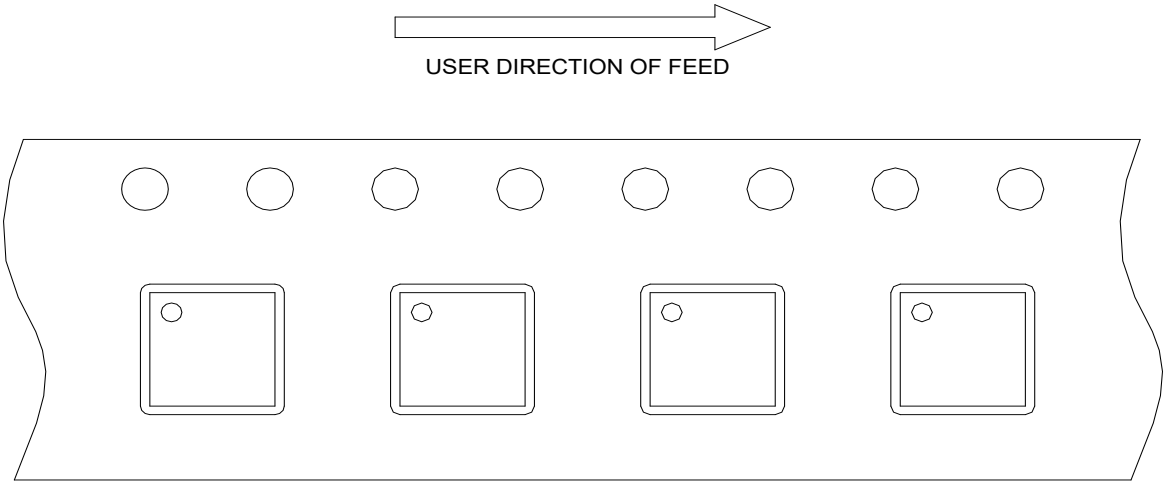
(mm)

Devices Per Unit

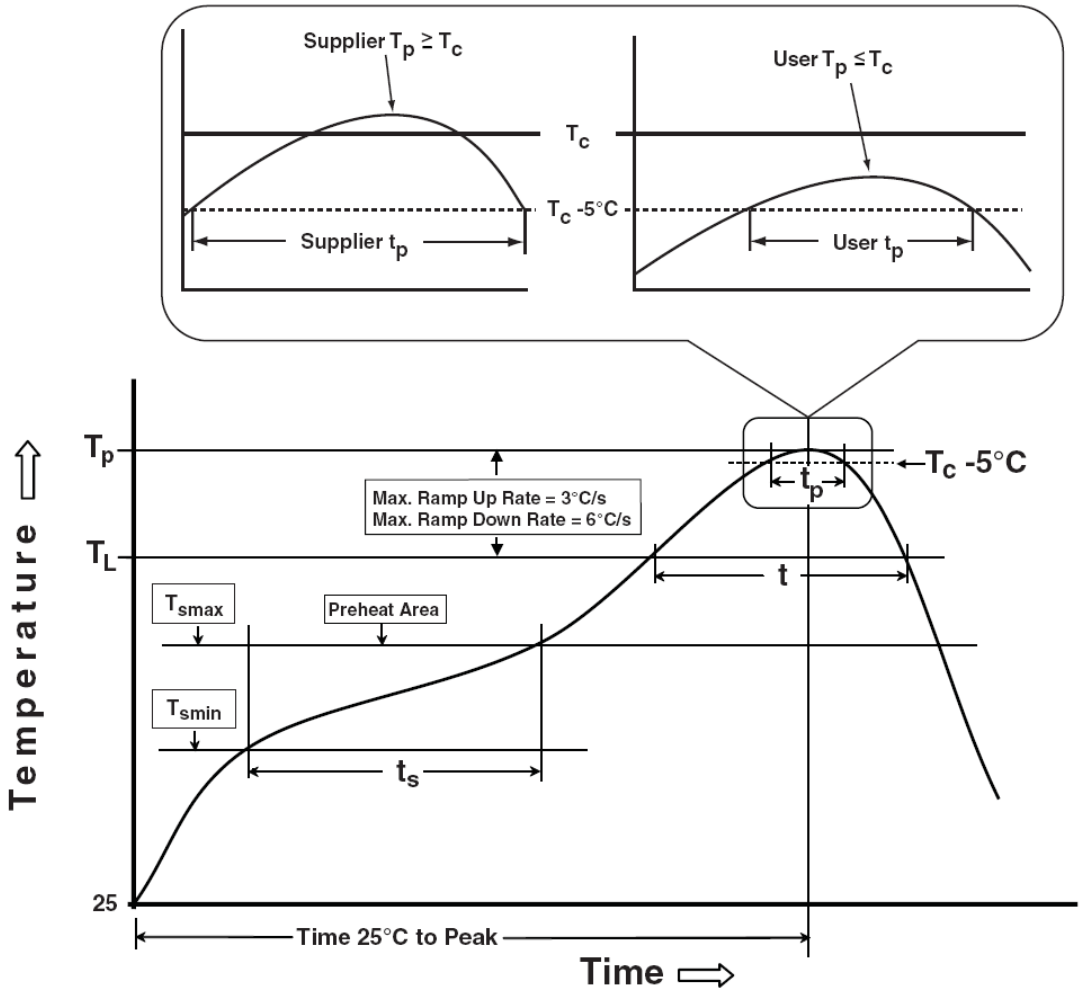
Package type	Packing	Quantity
TQFN4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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