APW9140

3A, 24V, 800kHz Synchronous Buck Converter with Ultrasonic Mode

Features

- **Input Voltage Range : 4.5V to 24V**
- **3A Output Current**
- **Low 55μA (typ.) Quiescent current**
- **Typical 0.6V ±1% Reference Voltage**
- **Fixed 800kHz Switching Frequency**
- **Excellent Light Load Efficiency by Pulse Skip Mode**
- **Stable with Low ESR Ceramic Capacitors**
- **5ms Integrated Soft Start**
- **Ultrasonic Mode (Fsw > 25kHz)**
- **100% Duty Cycle for USB PD Application**
- **Built in OVP, UVP, Current Limit and OTP**
- **Small TSOT-23-6A package**

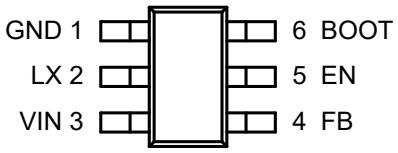
General Description

The APW9140 is a 3A synchronous buck converter with a current-mode control scheme that operates over a wide input voltage range of 4.5V to 24V and converts output voltages as low as 0.6V and as high as VIN with 100% duty cycle.
The APW9140 is equipped with an automatic skip mode operation to have high efficiency at light load.
The ultrasonic mode can keep switching frequency always higher than 25kHz at extra light load to prevent audible noise.
Power-on-reset, 5ms internal soft start and complete protections including under-voltage, over-voltage, over-temperature and current-limit are implemented into a single low cost TSOT-23-6A package.

Applications

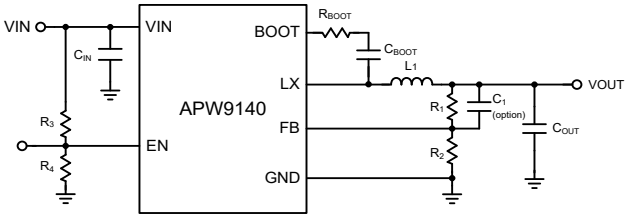
- **Notebook Computer & UMPC**
- **LCD Monitor/TV**
- **Consumer Application**

Pin Configuration (Top View)



TSOT-23-6A
Top View

Simplified Application Circuit



Ordering and Marking Information

APW9140 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code CT : TSOT-23-6 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW9140 CT : 	X - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}	VIN to GND	-0.3 ~ 26	V
V_{LX}	LX to GND	-0.3 ~ 26	V
V_{BOOT}	BOOT to GND	-0.3 ~ 5.5	V
$V_{I/O}$	FB, EN to GND	-0.3 ~ 6	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2)	100	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Control and Driver Supply Voltage	4.5 ~ 24	V
I_{OUT}	Converter Output Current	0 ~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

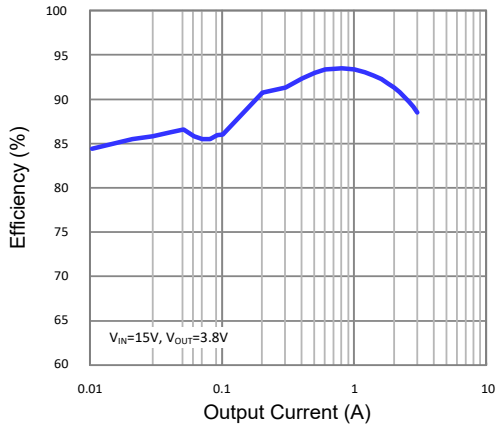
Unless otherwise specified, these specifications apply over V_{IN}=18V. T_A=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB}=0.7V	-	55	-	μA
I_{SHDN}	VIN Shutdown Supply Current	V_{EN}=GND	-	-	5	μA
POWER-ON-RESET (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	-	4.2	-	V
	VIN POR Hysteresis		-	0.44	-	V
ENABLE						
I_{EN}	EN Input Current	V_{EN}=2V	-	2	-	μA
V_{EN_H}	EN Enable Threshold	For Enable Chip	1.2	-	-	V
V_{EN_L}	EN shutdown Threshold	For Disable Chip	-	-	0.4	V
T_{D_EN}	EN Turn On Delay Time	When EN High to LX Switching	-	270	-	μs
R_{DIS}	Discharge Resistor	When EN goes Low	-	13	-	Ω
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	T_A=25°C	0.594	0.6	0.606	V
OSCILLATOR						
F_{OSC}	Oscillator Frequency		680	800	920	kHz
	Minimum Controllable On Time		-	70	-	ns
POWER MOSFET						
	High Side MOSFET Resistance		-	60	-	mΩ
	Low Side MOSFET Resistance		-	35	-	mΩ
	High Side MOSFET Leakage Current		-	-	1	μA
	Low Side MOSFET Leakage Current		-	-	1	μA
PROTECTIONS						
T_{ss}	Soft Start Time	V_{OUT} from 0% to 90%	-	5	-	ms
I_{LIM_H}	High Side MOSFET Current-Limit	Peak Current	-	5	-	A
I_{LIM_L}	Low Side MOSFET Current-Limit	Valley Current	-	4.5	-	A
	Over-Temperature Trip Point	Guarantee by design	-	150	-	°C
	Over-Temperature Hysteresis	Guarantee by design	-	30	-	°C
	Over Voltage Protection	Output Voltage Rising	-	125	-	%V_{REF}
	Under Voltage Protection		-	50	-	%V_{REF}

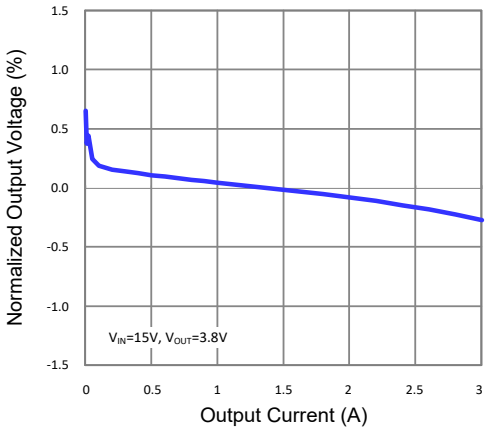
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=15V, T_A=25°C unless otherwise specified.

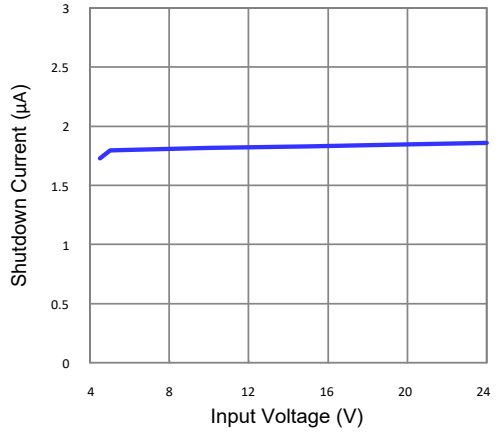
Efficiency vs. Output Current



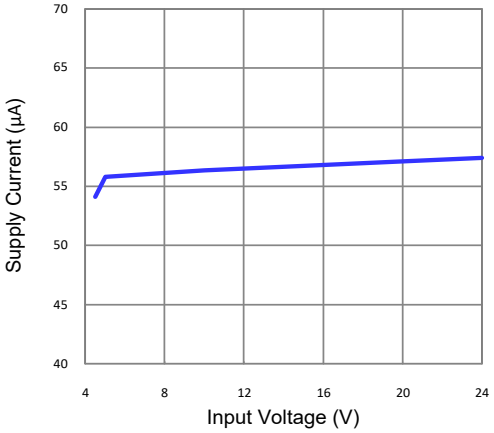
Load Regulation



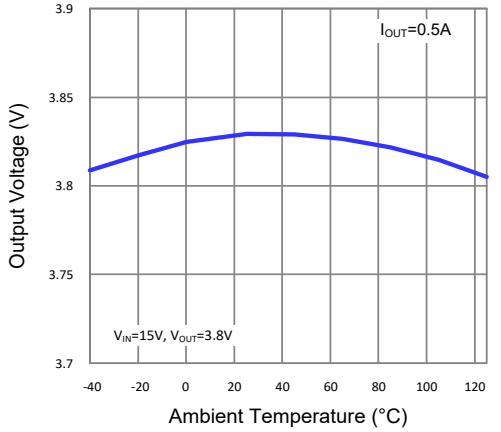
Shutdown Current vs. Input Voltage



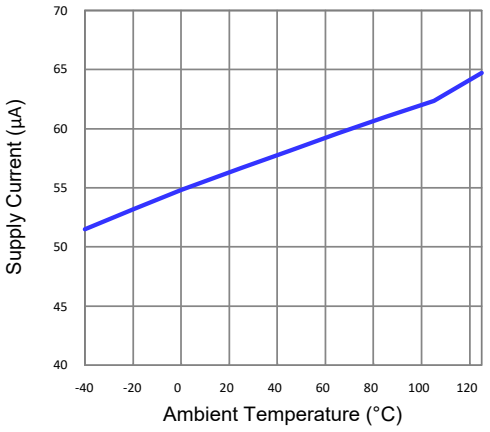
Supply Current vs. Input Voltage



Output Voltage vs. T_A



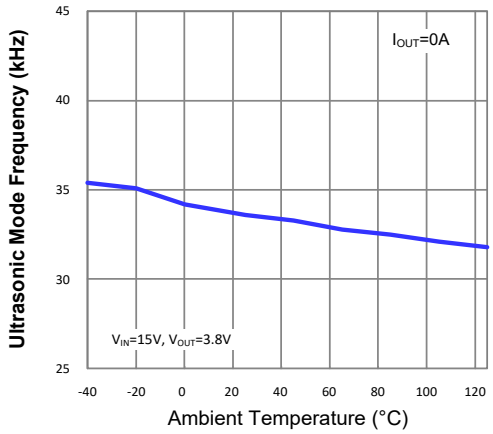
Supply Current vs. T_A



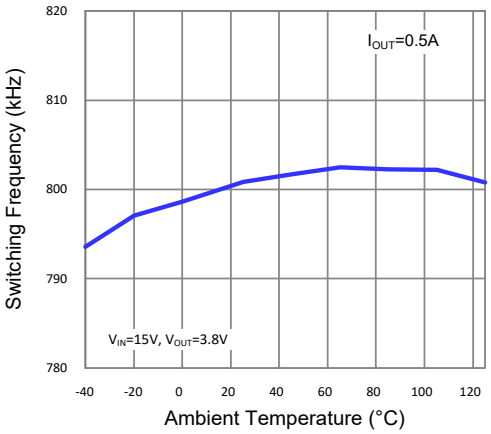
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=15V, T_A=25°C unless otherwise specified.

Ultrasonic Mode Frequency vs. T_A



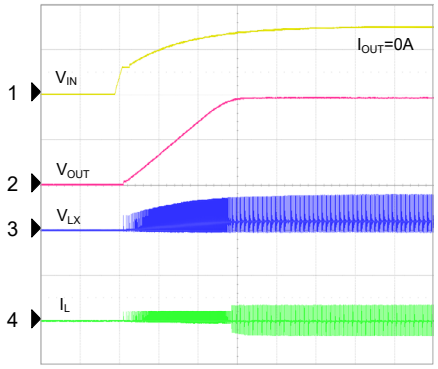
Switching Frequency vs. T_A



Operating Waveforms

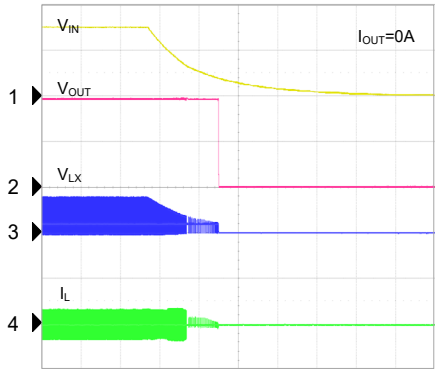
Refer to the typical application circuit. The test condition is V_{IN}=15V, T_A=25°C unless otherwise specified.

Start-Up by VIN



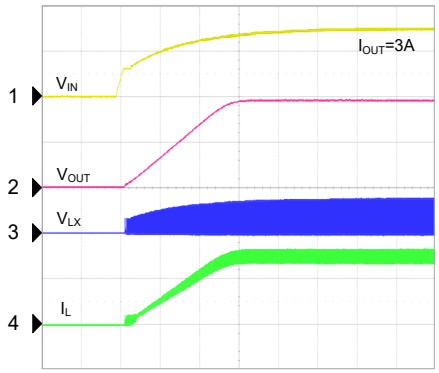
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 2ms/Div

Shutdown by VIN



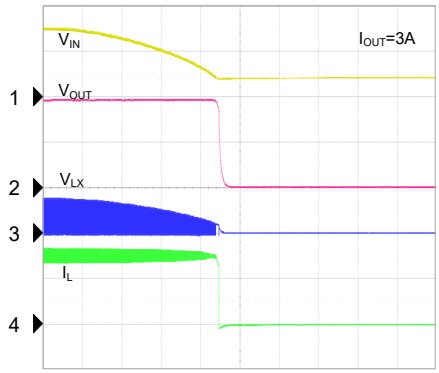
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 500ms/Div

Start-Up by VIN



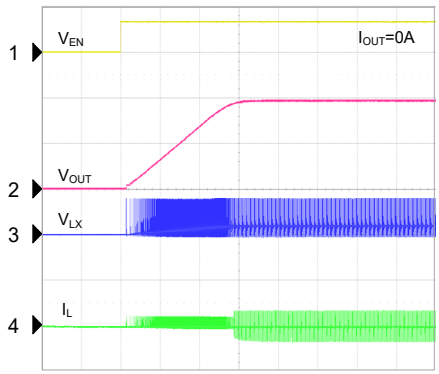
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 2ms/Div

Shutdown by VIN



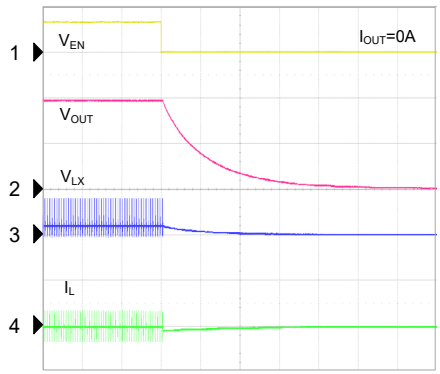
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 1ms/Div

Start-Up by Enable



CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 2ms/Div

Shutdown by Enable

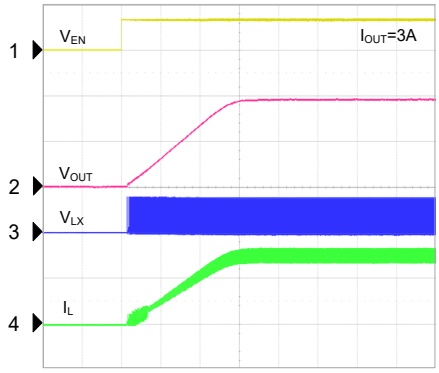


CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 500µs/Div

Operating Waveforms (Cont.)

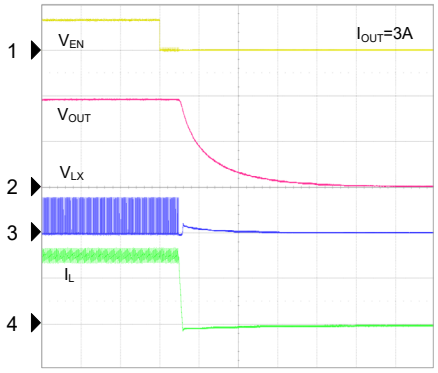
Refer to the typical application circuit. The test condition is V_{IN}=15V, T_A=25°C unless otherwise specified.

Start-Up by Enable



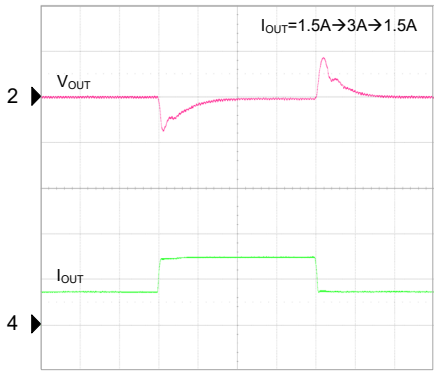
CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 2ms/Div

Shutdown by Enable



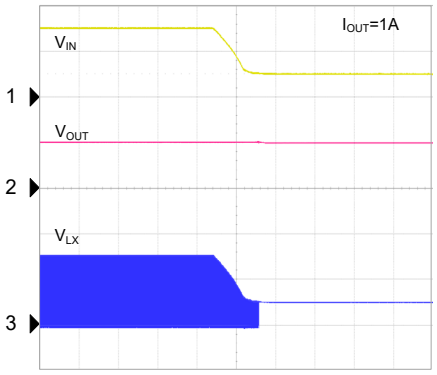
CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 50µs/Div

Load Transient Response



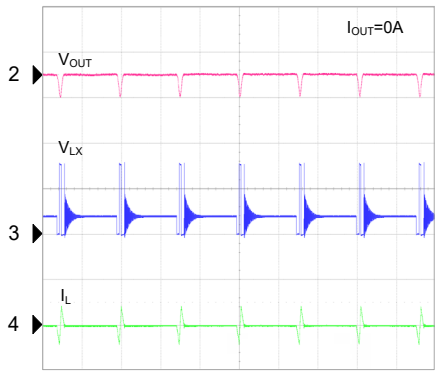
CH2: V_{OUT}, 200mV/Div, AC
CH4: I_{OUT}, 2A/Div
Time: 20µs/Div

100% Duty Operation



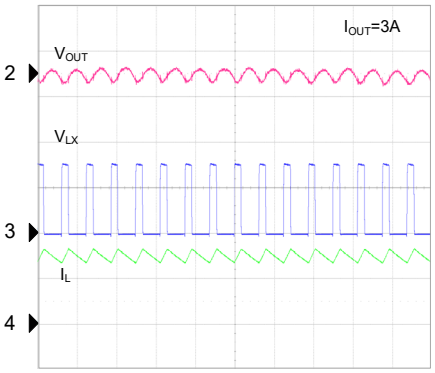
CH1: V_{IN}, 10V/Div
CH2: V_{OUT}, 5V/Div
CH3: V_{LX}, 10V/Div
Time: 20ms/Div

Output Ripple



CH2: V_{OUT}, 100mV/Div, AC
CH3: V_{LX}, 10V/Div
CH4: I_L, 2A/Div
Time: 20µs/Div

Output Ripple

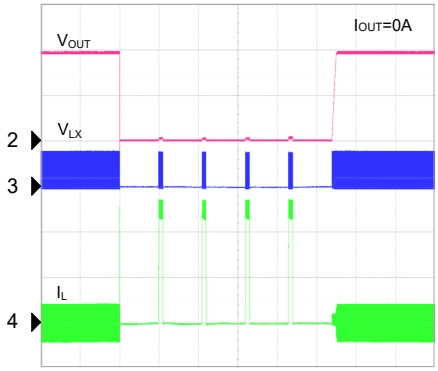


CH2: V_{OUT}, 20mV/Div, AC
CH3: V_{LX}, 10V/Div
CH4: I_L, 2A/Div
Time: 2µs/Div

Operating Waveforms (Cont.)

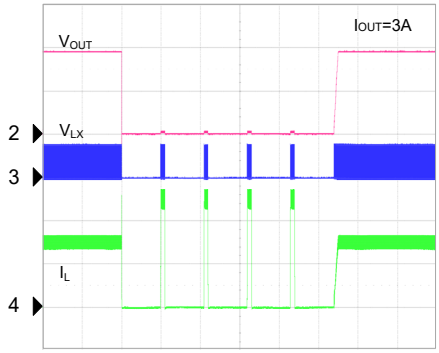
Refer to the typical application circuit. The test condition is V_{IN}=15V, T_A=25°C unless otherwise specified.

Short Entry and Recovery



CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 50ms/Div

Short Entry and Recovery

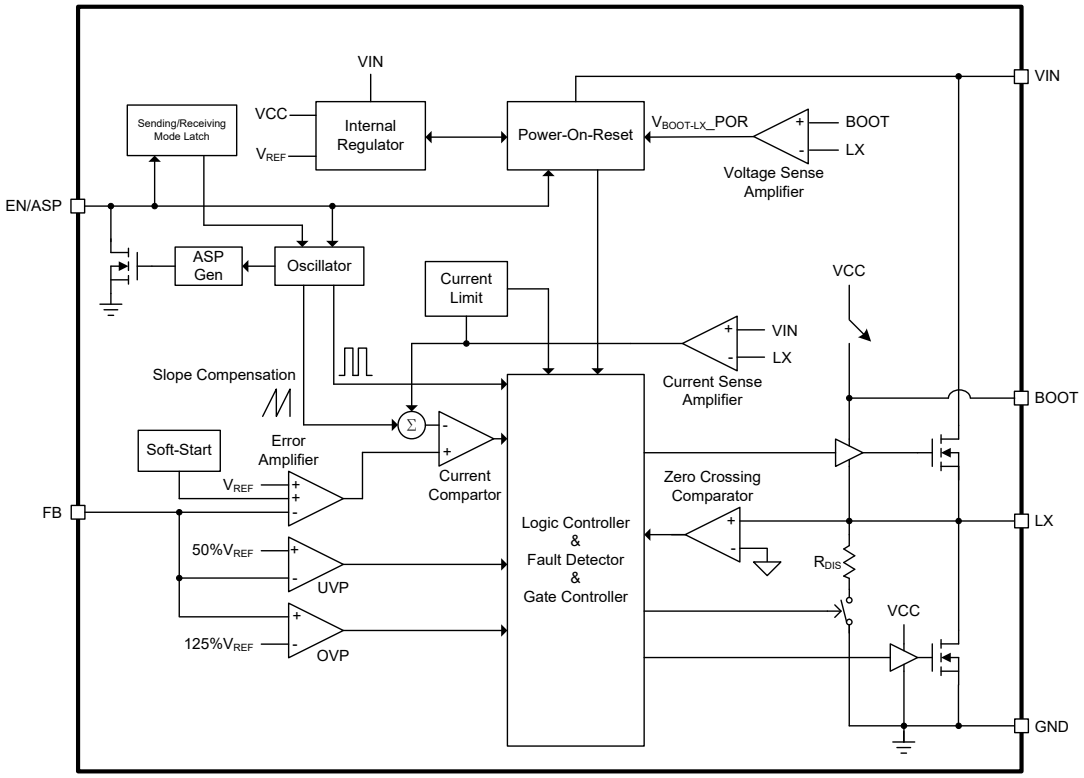


CH2: V_{OUT}, 2V/Div
CH3: V_{LX}, 20V/Div
CH4: I_L, 2A/Div
Time: 50ms/Div

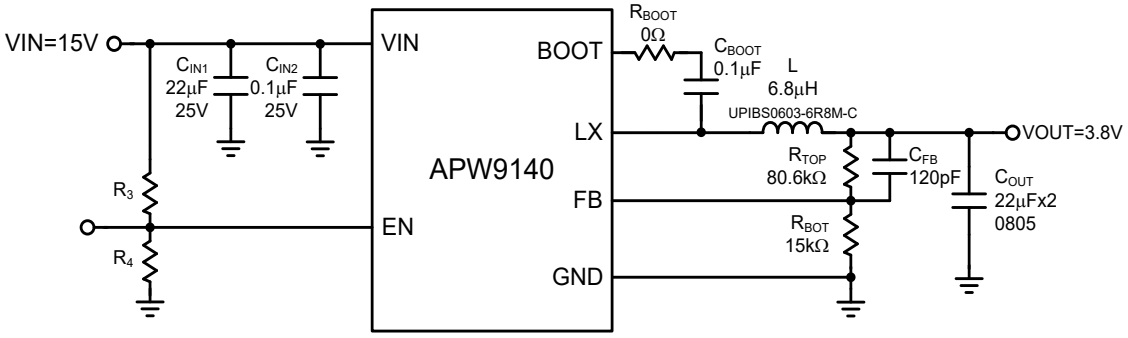
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	GND	Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
2	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
3	VIN	Power Input Pin. VIN supplies the power to the buck converter.
4	FB	Output Feedback Pin. FB senses the output voltage and regulates it. Connect the resistor divider from the output through. FB to the ground to set the output voltage.
5	EN	Enable Input. Drive EN high to turn the IC on and drive it low to turn the IC off.
6	BOOT	High-Side Gate Driver Supply Voltage Input Pin. A 0.1μF X5R ceramic capacitor is connected from this pin to the LX pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.

Block Diagram



Typical Application Circuit



Function Descriptions

Main Control Loop

The IC uses current mode control to regulate the output voltage. The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier. The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage.
The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Power-On-Reset (POR)

When the IC is powered up, the internal circuitry remains inactive until the VIN voltage exceeds the VIN POR high threshold voltage. When VIN is below the VIN POR low threshold voltage, the IC is turned off and the output discharge is triggered.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Current-Limit Protection and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When any output voltage drops below the UVP threshold, UVP is triggered and both converters enter hiccup mode.
In hiccup mode, the converters will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over current condition is removed, the IC will exit the hiccup mode.

Over-Voltage Protection

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Fast Discharge

When the EN signal goes low or the VIN voltage falls below the POR threshold, the IC is turned off and the output fast discharge is triggered.
The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.

Enable/Shutdown

The IC provides the EN pin, which is a digital input that turns the converter on or off. Drive EN high to turn the converter on and drive it low to turn it off.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(F_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to "Typical Application Circuits" The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Application Information (Cont.)

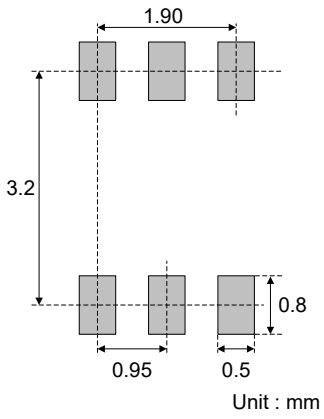
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN / PGND to capacitor less than 2mm respectively is recommended.
2. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
3. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
4. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
5. For better heat dissipation, it is strongly recommended to enlarge the thermal pad area as much as possible and place a large ground plane on each PCB layer below the thermal pad position, and place as many vias as possible from the top layer to the bottom layer on the thermal pad and around the ground plane.
6. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

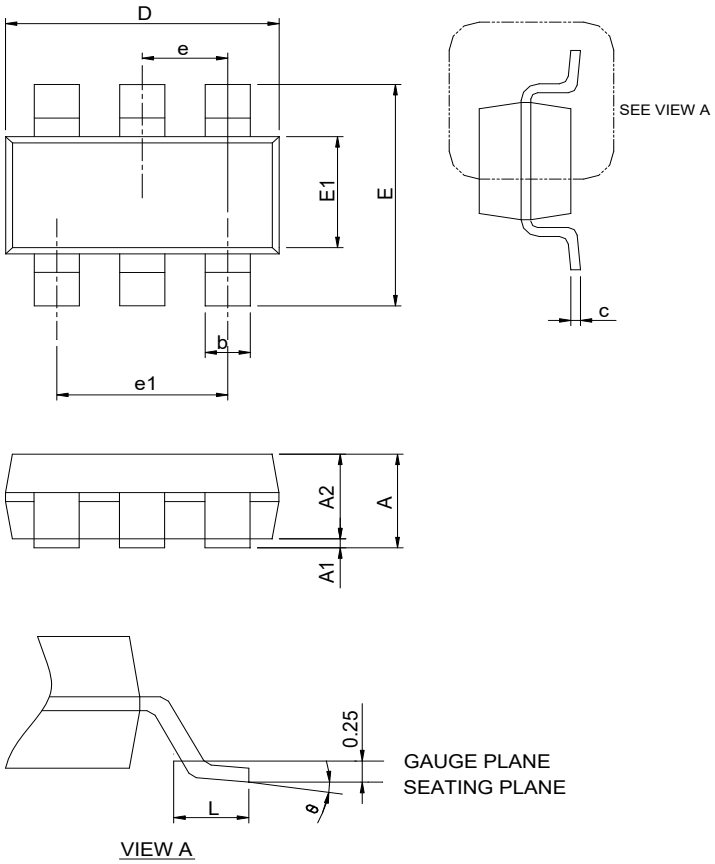
Recommended Minimum Footprint (Top View)

TSOT-23-6A



Package Information

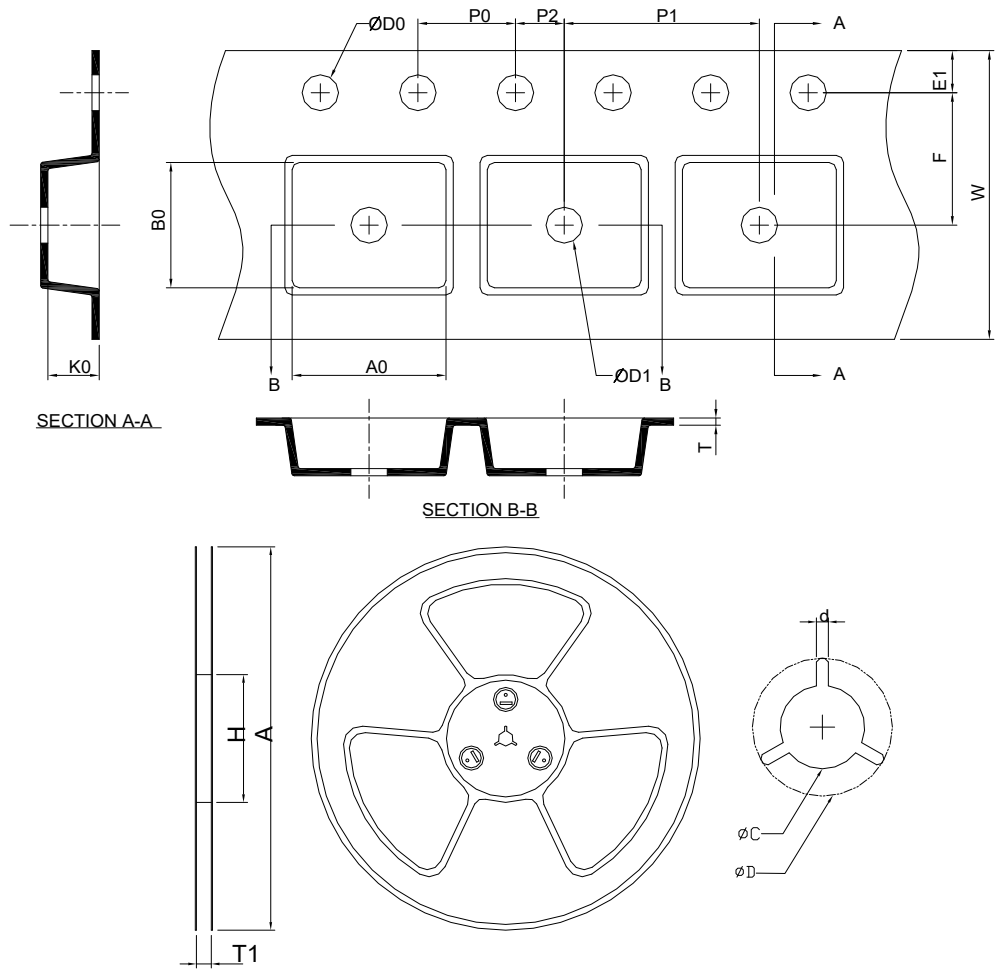
TSOT-23-6A



SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT 23-6A	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

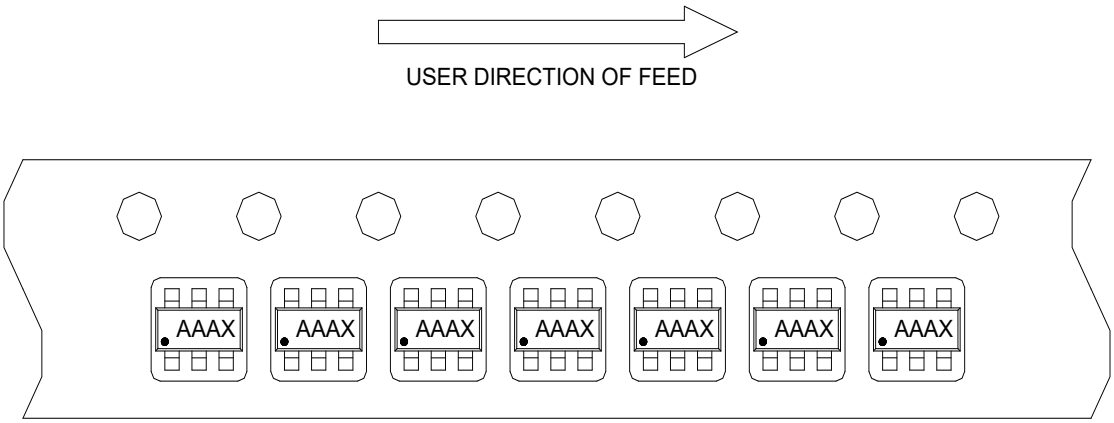
(mm)

Devices Per Unit

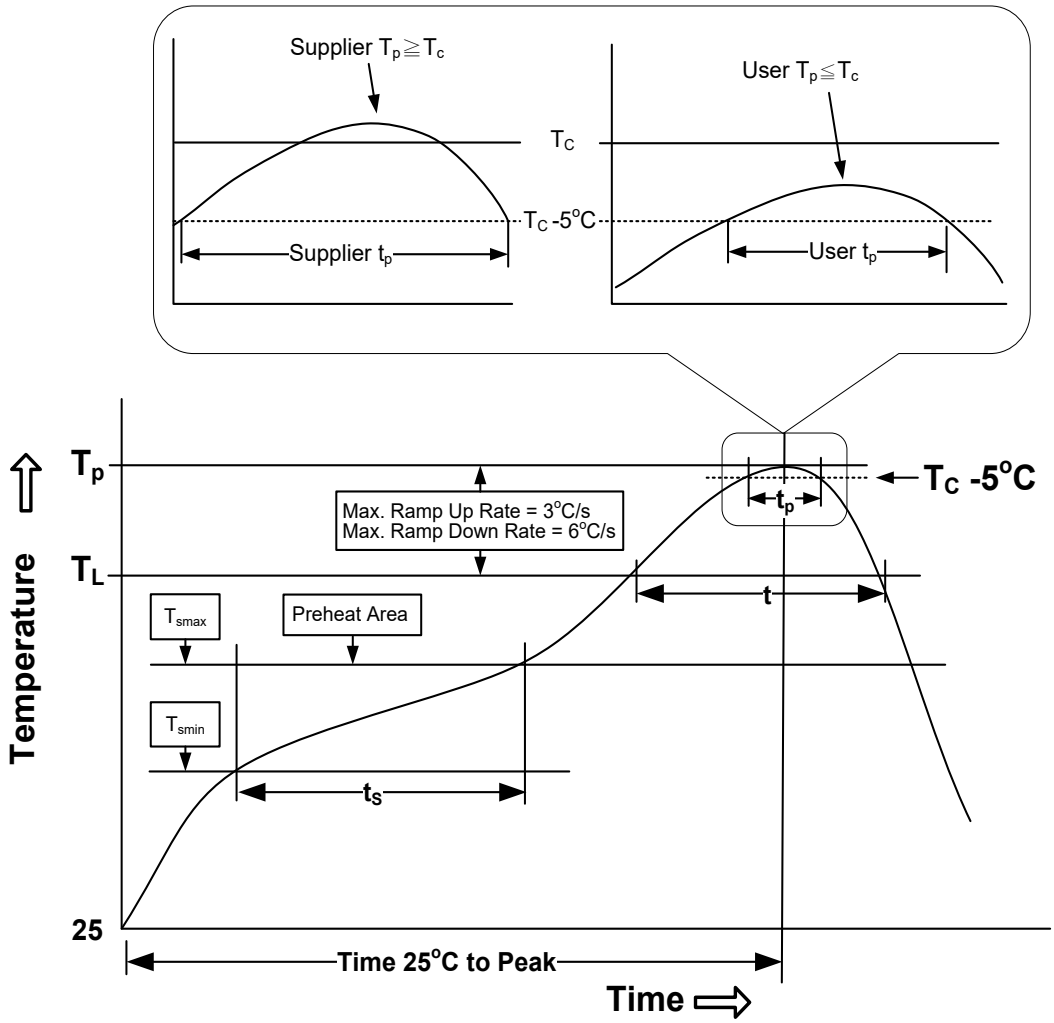
Package type	Packing	Quantity
TSOT-23-6A	Tape & Reel	3000

Taping Direction Information

TSOT-23-6A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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