APW9170C

2A, 5V Input, Synchronous Buck Converter

Features

- **Input Voltage Range: 2.7V to 5.5V**
- **Typical 0.6V Internal Reference Voltage**
- **2A Output Current**
- **Constant on Time Mode Operation**
- **2.5MHz Force PWM Mode Operation Frequency**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VIN**
- **Integrated 1ms Soft Start Time and Output Discharge**
- **Over-Temperature Protection**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Power Good Indication**
- **Small TDFN2x2-6A and TSOT23-6A Packages**

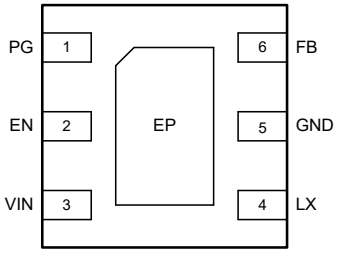
General Description

The APW9170C is a 2A synchronous buck converter that uses constant on time mode control scheme to convert wide input voltage of 2.7V to 5.5V to outputs as low as 0.6V while providing excellent output voltage regulation.
The APW9170C is also equipped with Power-on-reset, internal soft start and complete protections (under-voltage, over temperature and current-limit) into low cost TDFN2x2-6A and TSOT23-6A packages. The IC also provides output capacitor discharge when it is disabled via the discharge MOSFET.

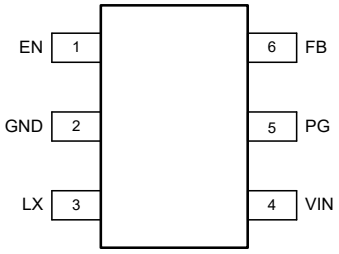
Applications

- **Wireless Module**
- **Low Voltage System Power**
- **General Networking Application**
- **Solid State drive**

Pin Configuration (Top View)

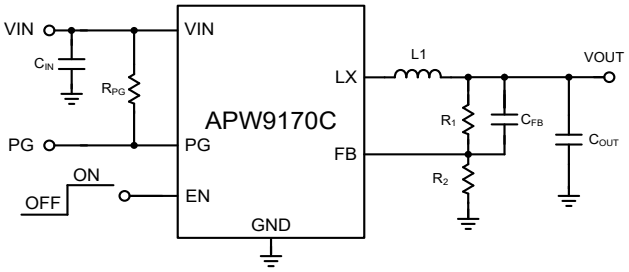


TDFN2x2-6A



TSOT23-6A

Simplified Application Circuit



Ordering and Marking Information

APW9170C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN2x2-6A CT : TSOT23-6A Operating Ambient Temperature Range I : -40 to 85 ℃ Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW9170C QB :  X - Date Code	APW9170C CT :  X - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN to GND		-0.3 ~ 6	V
V_{LX}	LX to GND Voltage	< 20ns pulse width	-3 ~ 7	V
		> 20ns pulse width	-0.3 ~ VIN+0.3	V
$V_{I/O}$	FB, EN, PG to GND Voltage		-0.3 ~ 6	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2)	TDFN2x2-6A	43.6	°C/W
θ_{JT}	Junction-to-Top Resistance (Note 2)		8.3	°C/W

Note 2: θ_{JA} and θ_{JT} are measured on Anpec evaluation board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Control and Driver Supply Voltage	2.7 ~ 5.5	V
V_{EN}	EN Input Voltage	0 ~ 5	V
I_{OUT}	Converter Output Current	0 ~ 2	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.3V. T_A=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY POWER						
I_{SHDN}	VIN Shutdown Supply Current	V_{EN}=GND	-	-	1	μA
	VIN POR Voltage Threshold	V_{IN} Rising	-	2.6	-	V
	VIN POR Hysteresis		-	0.3	-	V
EN THRESHOLD						
	EN Enable Threshold	To Enable IC	1.2	-	-	V
	EN Shutdown Threshold	To Disable IC	-	-	0.4	V
R_{EN}	EN Pull Low Resistor	V_{EN}=2V	-	1.65	-	MΩ
R_{DIS}	Discharge FET On Resistor	V_{IN}=5V, V_{LX}=1.2V, V_{EN}=0	-	45	-	Ω
REFERENCE VOLTAGE						
Tss	Soft Start Time	V_{OUT} from 0% to 90%	-	1	-	ms
V_{REF}	Reference Voltage	T_A=25°C	594	600	606	mV
I_{FB}	FB Input Current		-	0.1	-	μA
OSCILLATOR						
F_{SW}	Switching Frequency	V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A (Note 4)	-	2.5	-	MHz
POWER MOSFET						
R_{ON_H}	High Side MOSFET Resistance	V_{IN}=3.3V, T_A=25°C	-	130	-	mΩ
R_{ON_L}	Low Side MOSFET Resistance	V_{IN}=3.3V, T_A=25°C	-	80	-	mΩ
	High Side MOSFET Leakage Current		-	1	-	μA
	Low Side MOSFET Leakage Current		-	1	-	μA
PROTECTIONS						
I_{LIM}	Low Side MOSFET Current-Limit	Valley Current	-	2.5	-	A
	Over-Temperature Trip Point	(Note 4)	-	150	-	°C
	Over-Temperature Hysteresis	(Note 4)	-	30	-	°C
	Over Voltage Protection		-	120	-	%V_{OUT}
	Under Voltage Protection		-	50	-	%V_{OUT}
POWER GOOD (PG)						
	PG Threshold	PG in from Lower (PG is Pulled High)	-	95	-	%V_{OUT}
		PG Low Hysteresis (PG Goes Low)	-	5	-	%V_{OUT}
		PG out from Normal (PG Goes Low)	-	110	-	%V_{OUT}
		PG High Hysteresis (PG is Pulled High)	-	5	-	%V_{OUT}
	PG Delay Time	PG is Pulled High	-	55	-	μs
		PG Goes Low	-	30	-	μs
V_{PG}	PG Output Low Voltage	V_{FB}=0.5V, sink 1mA	-	-	0.25	V

Note 4: Guarantee by design.

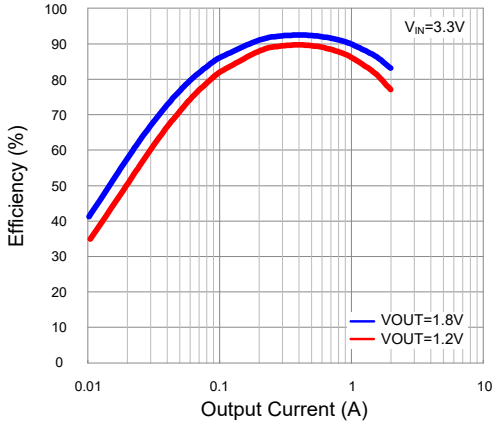
Pin Descriptions

PIN			FUNCTION
TDFN2x2-6A NO.	TSOT23-6A NO.	NAME	
1	5	PG	Output Power Good Indicator Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage for the PG function.
2	1	EN	Enable Input Pin. Drive EN high to turn the converter on and drive it low to turn it off.
3	4	VIN	Power Input Pin. VIN supplies the power to the buck converter and the internal control circuitry.
4	3	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
5	2	GND	Power Ground. This pin must be connected directly to the ground plane of the PCB using low inductance vias.
6	6	FB	Output Feedback Pin. FB Pin senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.

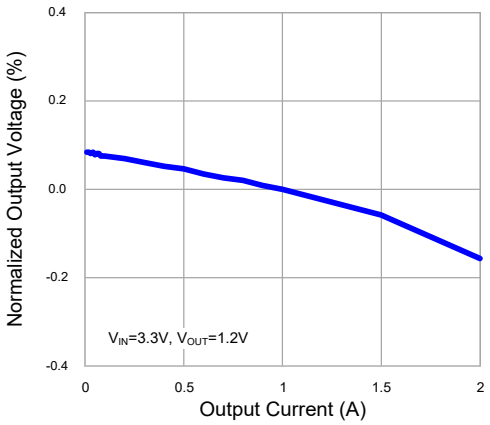
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A=25°C unless otherwise specified.

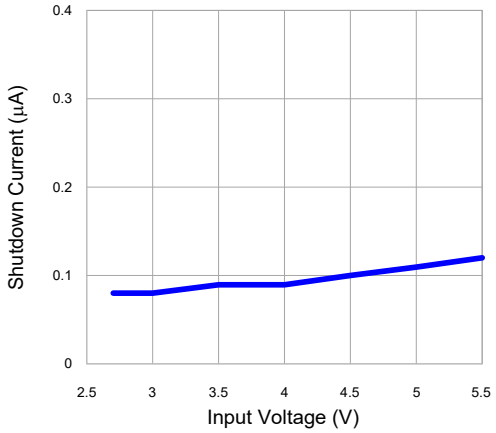
Efficiency vs. Output Current



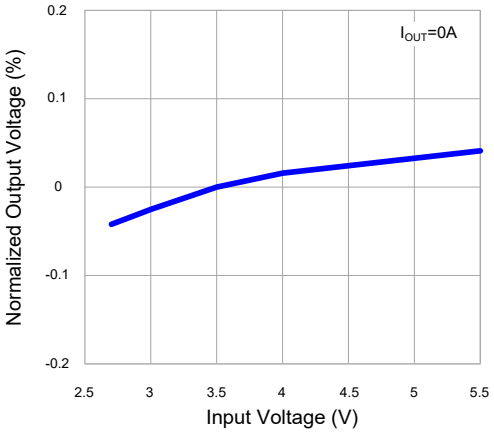
Load Regulation



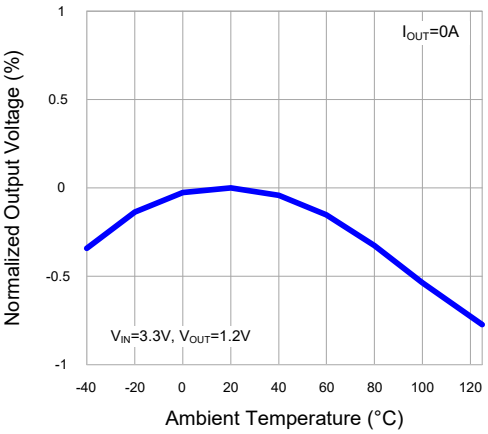
Shutdown Current vs. Input Voltage



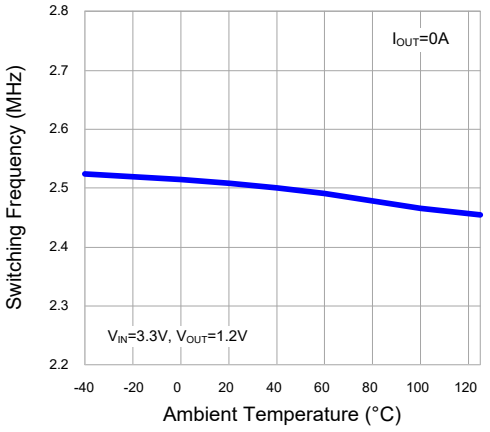
Line Regulation



Output Voltage vs. T_A

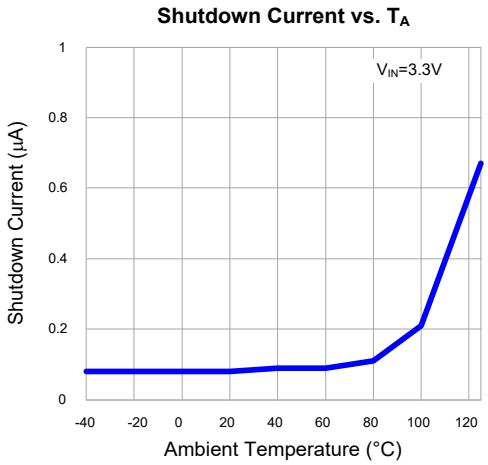


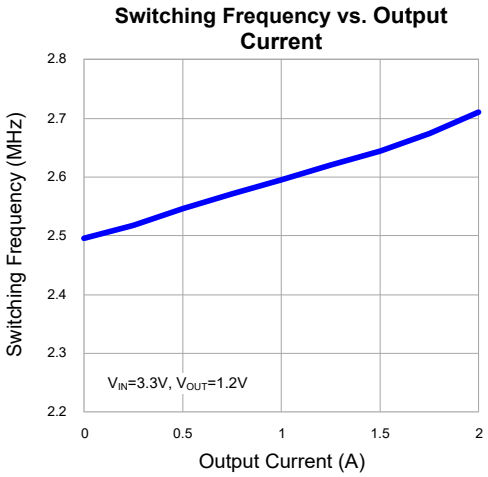
Switching Frequency vs. T_A



Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A=25°C unless otherwise specified.

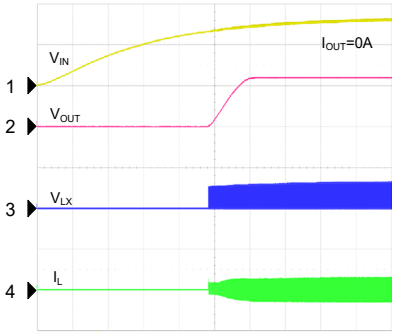




Operating Waveforms

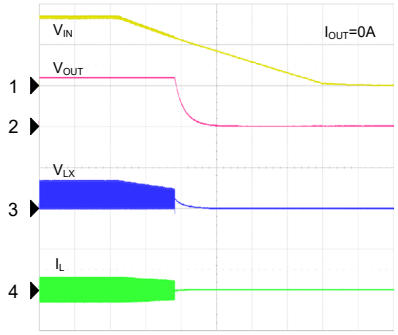
Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A=25°C unless otherwise specified.

Start-Up by VIN



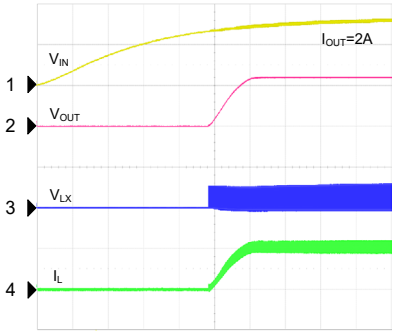
CH1: V_{IN}, 2V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 1ms/Div

Shutdown by VIN



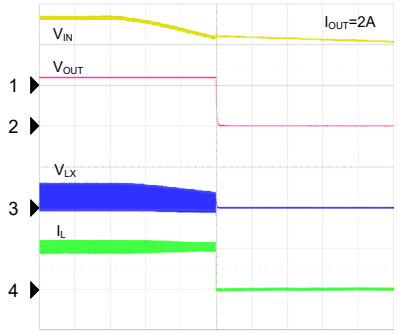
CH1: V_{IN}, 2V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 5ms/Div

Start-Up by VIN



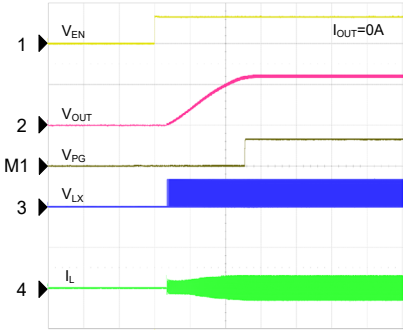
CH1: V_{IN}, 2V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
Time: 1ms/Div

Shutdown by VIN



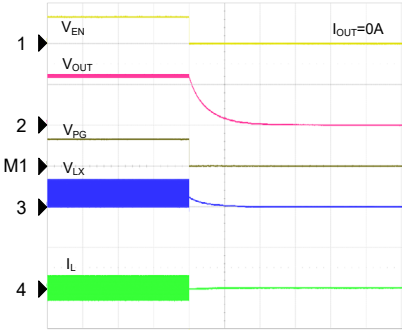
CH1: V_{IN}, 2V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
Time: 500µs/Div

Start-Up by Enable



CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
M1: V_{PG}, 5V/Div
Time: 500µs/Div

Shutdown by Enable

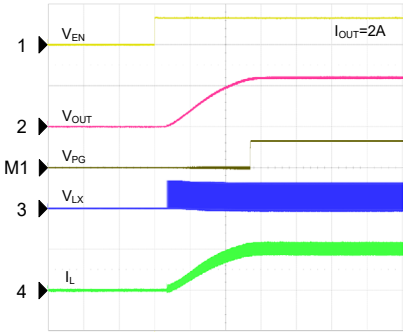


CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
M1: V_{PG}, 5V/Div
Time: 2ms/Div

Operating Waveforms (Cont.)

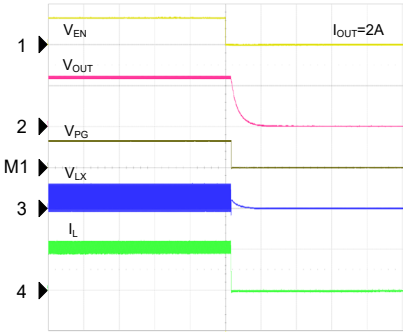
Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A=25°C unless otherwise specified.

Start-Up by Enable



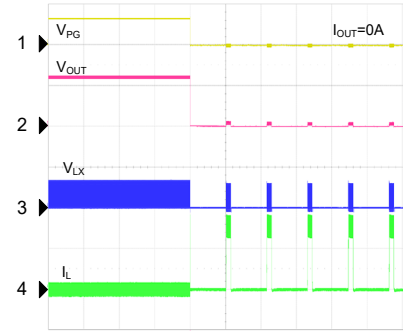
CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
M1: V_{PG}, 5V/Div
Time: 500µs/Div

Shutdown by Enable



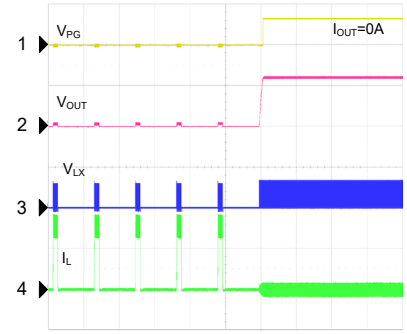
CH1: V_{EN}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
M1: V_{PG}, 5V/Div
Time: 50µs/Div

Short Entry



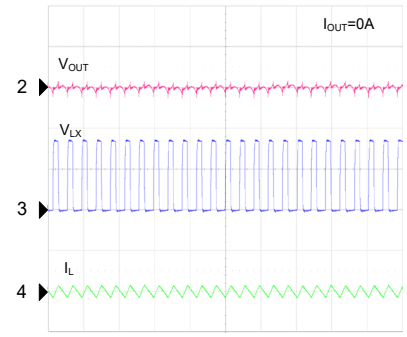
CH1: V_{PG}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
Time: 10ms/Div

Short Recovery



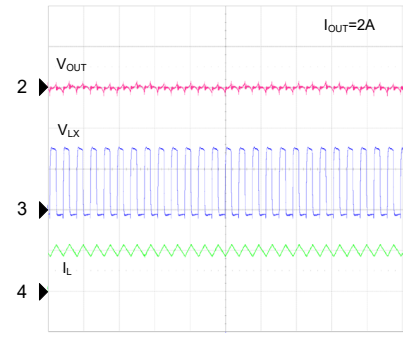
CH1: V_{PG}, 5V/Div
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 2A/Div
Time: 10ms/Div

Steady State



CH2: V_{OUT}, 10mV/Div, AC
CH3: V_{LX}, 2V/Div
CH4: I_L, 2A/Div
Time: 1µs/Div

Steady State

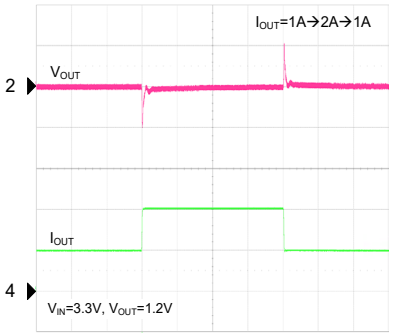


CH2: V_{OUT}, 10mV/Div, AC
CH3: V_{LX}, 2V/Div
CH4: I_L, 2A/Div
Time: 1µs/Div

Operating Waveforms (Cont.)

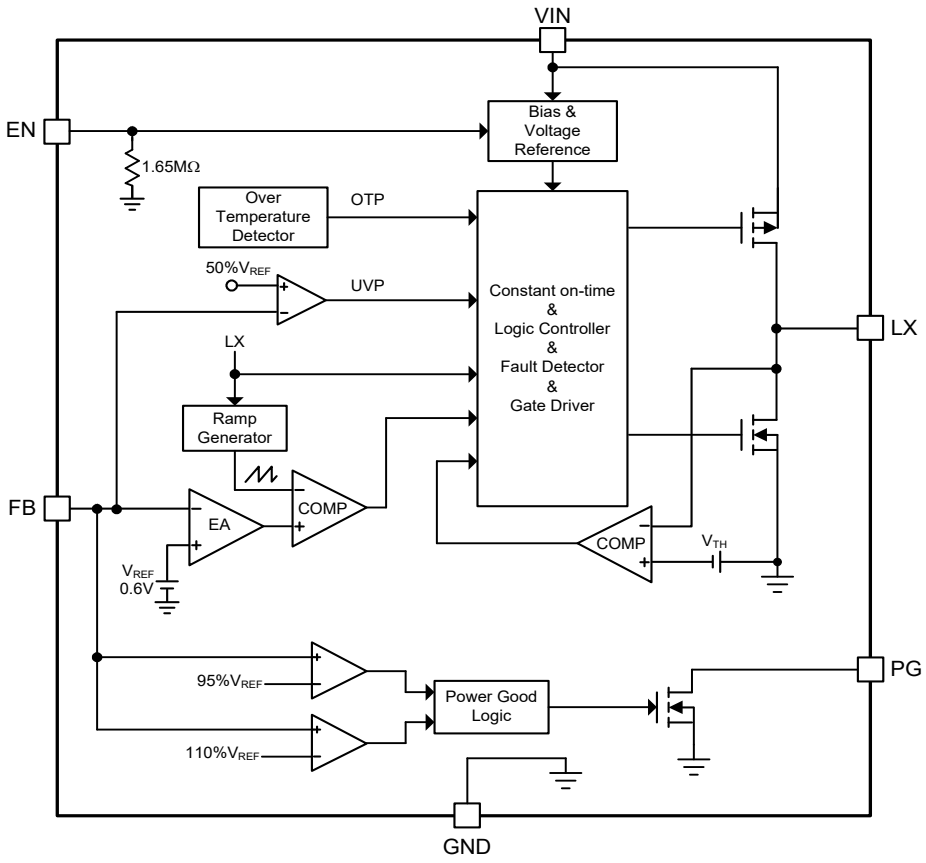
Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A=25°C unless otherwise specified.

Load Transient Response



CH2: V_{OUT}, 20mV/Div, AC
CH4: I_{OUT}, 1A/Div
Time: 50µs/Div

Block Diagram



Typical Application Circuit

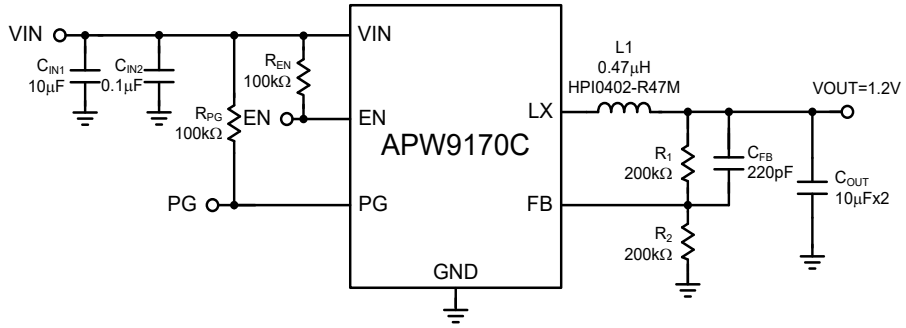


Figure 1. VOUT=1.2V

Components Selection for Different Output Voltage

VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
3.3	1.2	0 ~ 2A	10µ // 0.1µ	0.47µ	10µ × 2	200k (1%)	200k (1%)	220p
3.3	1.8	0 ~ 2A	10µ // 0.1µ	0.47µ	10µ × 2	200k (1%)	100k (1%)	220p
5	3.3	0 ~ 2A	10µ // 0.1µ	0.47µ	10µ × 3	200k (1%)	44.2k (1%)	Option

Function Descriptions

The APW9170C integrates a synchronous buck PWM controller and high/low side power MOSFETs to generate VOUT. It offers the lowest total solution cost that can provide up to 2A continuous output current over wide input supply range. Input voltage range of the PWM converter is 2.7V to 5.5V. User defined output voltage is possible and can be adjustable from 0.6V to VIN.

Constant-On-Time PWM Controller

This IC uses constant on-time control, has a simple control loop, and allows it to use ceramic-type output capacitors for excellent transient response. This architecture is pseudo-fixed frequency with input voltage feed forward. On-time is inversely proportional to input voltage and proportional to output voltage. When the voltage on FB is lower than the internal reference voltage, the high-side switch will be turned on for a calculated on-time. The on-time can be estimated as (V_{IN}=3.3V, V_{OUT}=1.2V):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.4\mu s$$

In addition, a minimum off-time is set to prevent the inductor current from running out of control during load transients.

VIN Power-On-Reset (POR)

The IC continuously monitors the voltage on the VIN pin. The soft start is activated when the VIN voltage and the EN voltage are above their respective POR thresholds. VIN POR is used to protect the IC from erroneous operation with insufficient VIN voltage. VIN POR also has hysteresis to resist ripple on the VIN voltage.

Enable and Shutdown

The IC provides the EN pin, which is a digital input that turns the converter on or off. Drive EN high to turn the converter on and drive it low to turn it off.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Discharge

When the EN signal goes low or the VIN voltage falls below the POR threshold, the IC is turned off and the output soft stop is triggered.
A discharge MOSFET, between the LX of the converter and ground is turned on, allowing the output capacitor to be discharged through this MOSFET. This is mainly important when there is no load to discharge the output capacitors.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Power Good (PG)

The IC has an open-drain PG pin to indicate the output voltage. PG goes high when VOUT reaches 95% of the target value. When VOUT is below 90% of the target voltage, the PG pin will be pulled low. And when VOUT exceeds 110% of the target value, PG is also pulled low. When VOUT is below 105% of the target voltage, the PG pin will go high. Since PG is an open-drain pull-down device, an external pull-up resistor is usually required; however, if this pin is not used, no resistor is required.

Current-Limit Protection and Hiccup

The IC monitors the current through the low-side power MOSFET to limits the valley inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop.
When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode.
In hiccup mode, the converter will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over current condition is removed, the IC will exit the hiccup mode.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(F_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to "Typical Application Circuits" The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Application Information (Cont.)

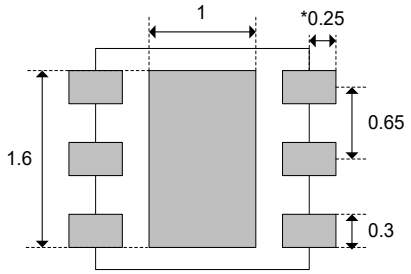
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and GND pins. Connecting the capacitor and VIN/GND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.
2. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
3. The ground of the output capacitor and input capacitor and the GND of the IC should be as close as possible.
4. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
5. For better heat dissipation, it is strongly recommended to enlarge the thermal pad area as much as possible and place a large ground plane on each PCB layer below the thermal pad position, and place as many vias as possible from the top layer to the bottom layer on the thermal pad and around the ground plane.
6. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the GND of the IC.

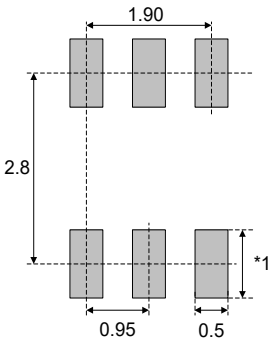
Recommended Minimum Footprint (Top View)

TDFN2x2-6A



Unit : mm * Just Recommend

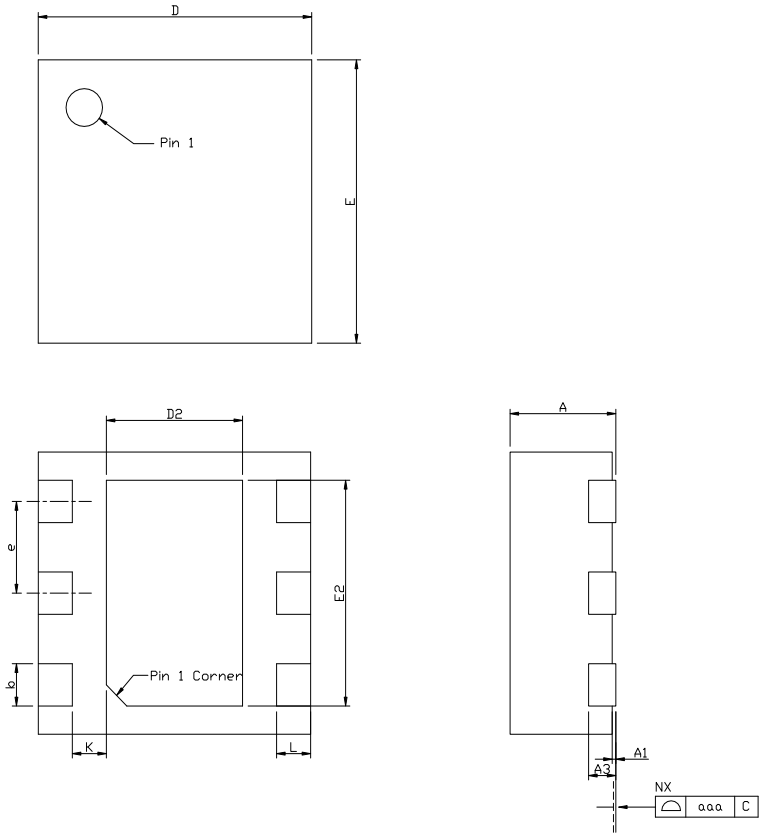
TSOT23-6A



Unit : mm * Just Recommend

Package Information

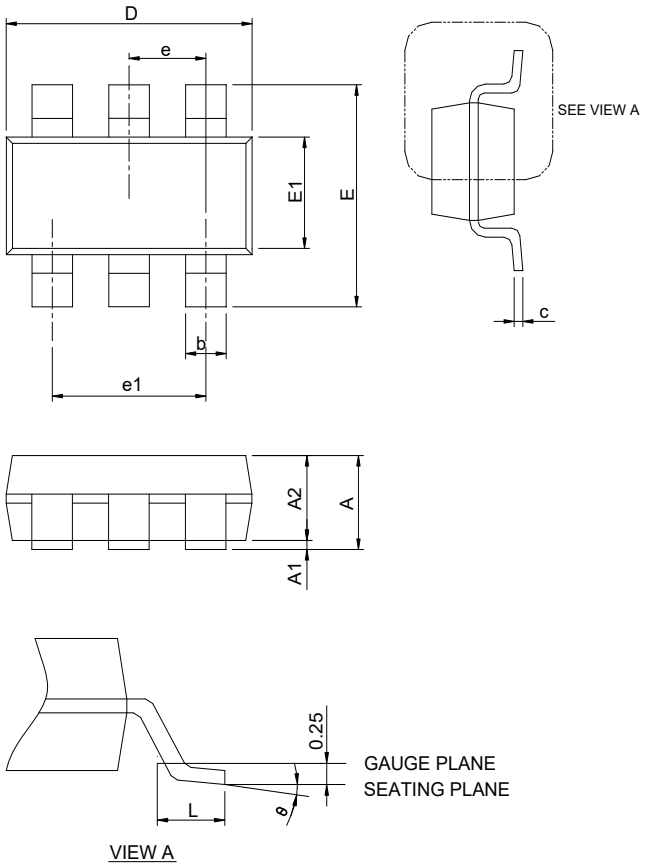
TDFN2x2-6A



SYMBOL	TDFN2*2-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	1.90	2.10	0.075	0.083
D2	0.95	1.05	0.037	0.041
E	1.90	2.10	0.075	0.083
E2	1.55	1.65	0.061	0.065
e	0.65 BSC		0.026 BSC	
L	0.20	0.30	0.008	0.012
K	0.20		0.008	
aaa	0.08		0.003	

Package Information

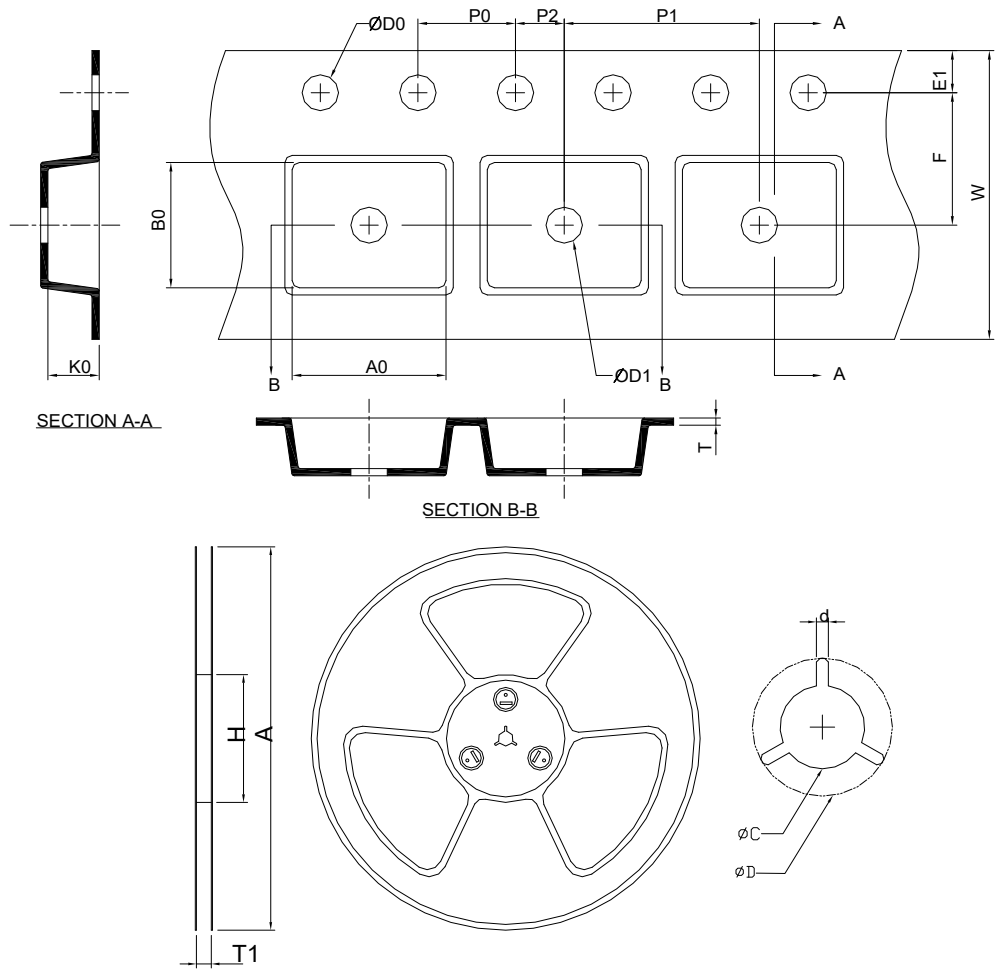
TSOT23-6A



SYMBOL	TSOT-23-6A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.30	0.50	0.012	0.020
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN 2x2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSOT 23-6(A)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

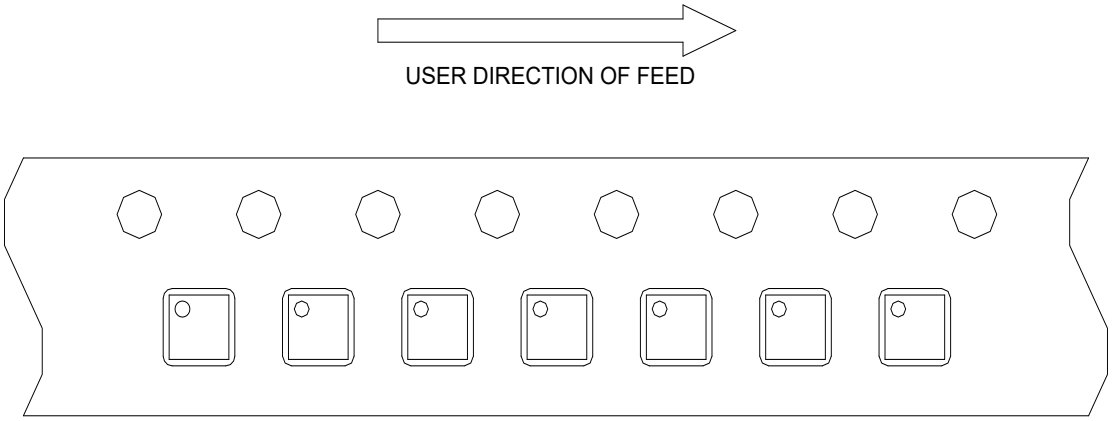
(mm)

Devices Per Unit

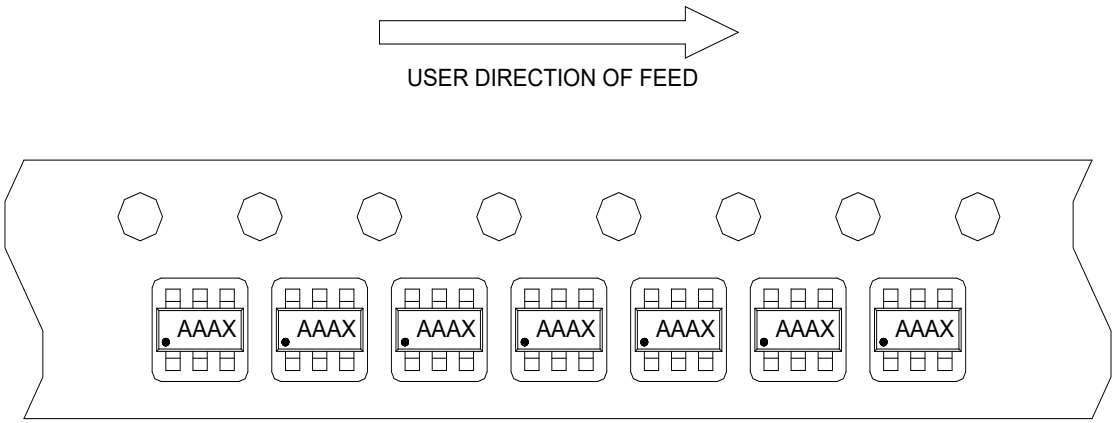
Package type	Packing	Quantity
TDFN 2x2	Tape & Reel	3000
TSOT 23-6(A)	Tape & Reel	3000

Taping Direction Information

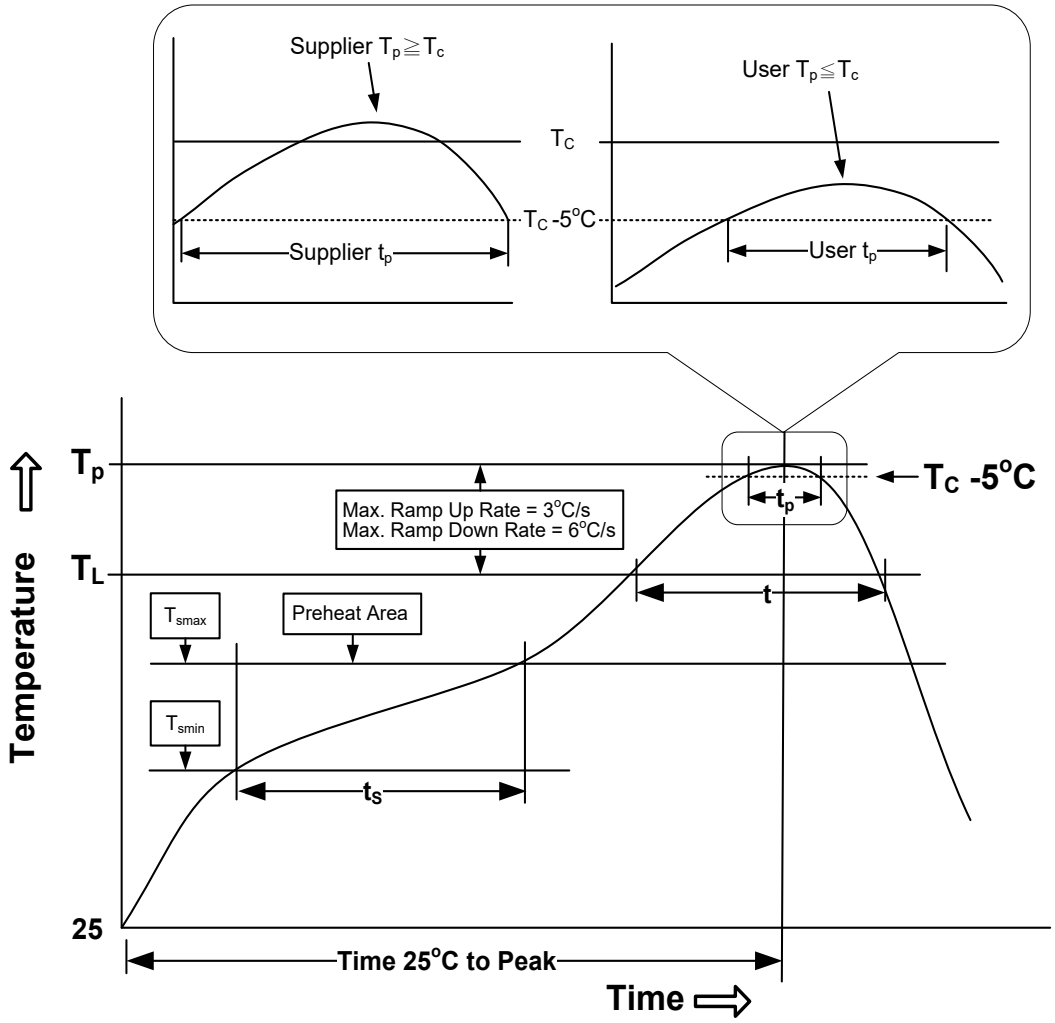
TDFN2x2-6A



TSOT23-6A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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