APW9304H

3-CH Buck Converter, 3-18V Input Voltage, Tiny Package, AEC-Q100 Qualified

Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide input voltage range:**
  - **Channel 1 and 3 from 1.65V to 18V**
  - **Channel 2 from 3V to 18V**
- **3A/2.5A/1.5A Output Current on Channel1/2/3**
- **Typical 0.6V ±1% Internal Reference Voltage**
- **Sync Pin Allows Synchronization to an External Clock from 1.8MHz to 2.4MHz**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **N-CH MOSFET (60 mΩ) for CH1 High Side**
  - **N-CH MOSFET (90 mΩ) for CH2/3 High Side**
  - **N-CH MOSFET (45 mΩ) for CH1 Low Side**
  - **N-CH MOSFET (50 mΩ) for CH2/3 Low Side**
- **Built in OVP, UVP, Current Limit, VIN OVP and OTP**
- **High Performance or Low Cost Configuration, Auto Mode or FPWM can be set by MODE PIN**
- **Spread Spectrum Option and Power On Sequence can be configured by SEQ/SSP PIN**
- **Available in a TQFN 4x4-20D Package with Wettable Flanks**

General Description

The APW9304H is a three-channel synchronous mode PWM converter with 3A continuous current capability for one channel and 2.5A continuous current capability for the other channel and 1.5A continuous current capability for the other one channel.

Although the switching frequency of the APW9304H is fixed at 2.1MHz, it can also change the switching frequency via the EN/SYNC pin.

The APW9304H also provides a 120-degree phase shifting technique and Spread Spectrum option to minimize the noise for reducing EMI.

The output voltage of each channel can be adjusted using an external resistor divider. Other features include VIN OVP, VOUT OVP, UVP, current limit, and OTP.

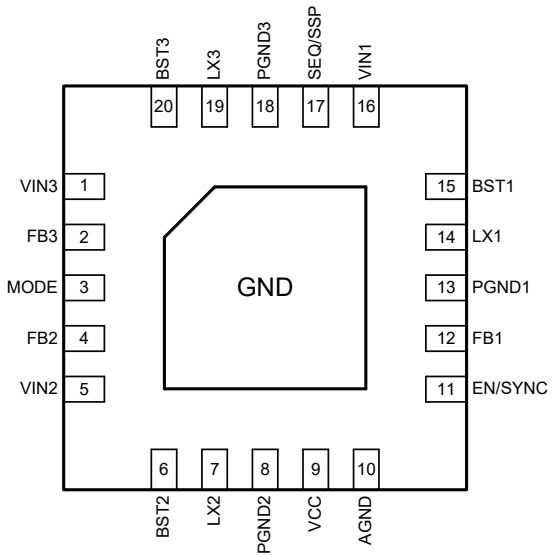
The internal switching frequency is set at 2.1MHz. Other features of the part include VIN OVP, OVP, UVP, Current Limit and OTP.

The APW9304H is available in a TQFN 4x4-20D wettable flanks package with small size and excellent thermal capacity.

Applications

- **Automotive**
- **ADAS**
- **Automotive camera with CMOS sensor**

Pin Configuration



TQFN4x4-20D

Ordering and Marking Information

APW9304H □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-20D Operating Ambient Temperature Range H : -40 to 125℃ Handling Code TR : Tape & Reel Assembly Material G : Green Part
APW9304H QB : 	XXXXX - Date Code

Note: ANPEC's green product compliant RoHS and Halogen free.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}	VIN1/2/3 to PGND1/2/3	-0.3 ~ 21	V
V_{BS}	BST1/2/3 to LX1/2/3	-0.3 ~ 5.5	V
V_{LX}	LX1/2/3 to PGND1/2/3	-1 ~ 20	V
$V_{I/O}$	VCC, FB1/2/3, EN/SYNC, SEQ/SSP, MODE to AGND	-0.3 ~ 6	V
V_{GND}	PGND1, PGND2, PGND3, AGND to GND	-0.3 ~ 0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2)	25.261	°C/W
P_D	Power Dissipation P_D @ TA=25°C	4.95	W

Note 2: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Range	Unit
VIN1, VIN3	VIN1/VIN3 Supply Voltage		1.65 ~ 18	V
VIN2	VIN2 Supply Voltage		3 ~ 18	V
$V_{EN/SYNC}$	EN/SYNC Input Voltage		0 ~ 5	V
VOUT	Converter Output Voltage		0.6 ~ 5	V
I_{OUT}	Converter Output Current	CH1	0 ~ 3	A
		CH2	0 ~ 2.5	
		CH3	0 ~ 1.5	
T_A	Ambient Temperature		-40 ~ 125	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN=12V, $V_{EN/SYNC}$=5V. Typical values are at T_J=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT (for CH1, CH2 and CH3)						
I_{VIN}	VIN Input Current	V_{FB}=0.7V, Auto-mode	-	420	-	uA
I_{VIN_SHDN}	VIN Shutdown Current	$V_{EN/SYNC}$=AGND	-	-	5	uA
UNDER VOLTAGE LOCKOUT (for CH1, CH2 and CH3)						
V_{UVLO2_R}	UVLO2 Upper Threshold Voltage	VIN2 Rising	-	2.8	-	V
V_{UVLO2_Hys}	UVLO2 Hysteresis Voltage	VIN2 Falling	-	0.2	-	V
$V_{UVLO1/3\_R}$	UVLO1/3 Upper Threshold Voltage	VIN1/3 Rising	-	1.6	-	V
$V_{UVLO1/3\_Hys}$	UVLO1/3 Hysteresis Voltage	VIN1/3 Falling	-	0.2	-	V
REGULATOR AND VCC (for CH1, CH2 and CH3)						
V_{REF}	Reference Voltage	T_J=25°C	594	600	606	mV
V_{POR}	VCC POR Threshold Voltage	VCC Rising	-	2.8	-	V
V_{POR_Hys}	VCC POR Hysteresis Voltage	VCC Falling	-	0.2	-	V
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A (Note 4)	-	5	-	V
t_{SS}	Output Soft Start Time		-	1	-	ms
R_{DIS}	Internal Discharge Resistor		-	150	-	Ω
EN/SYNC THRESHOLD (for CH1, CH2 and CH3)						
$V_{EN/SYNC\_H}$	EN/SYNC Input Threshold High Voltage	For Enable Chip	-	1	1.15	V
$V_{EN/SYNC\_Hys}$	EN/SYNC Input Hysteresis Voltage	For Shutdown Chip	-	0.25	-	V
$T_{DB\_EN\_OFF}$	EN/SYNC Turn Off Debounce Time		-	20	-	us
T_{D_EN}	EN/SYNC Turn On Delay Time	When EN/SYNC High to LX Switching	-	350	-	us
$I_{EN/SYNC}$	EN/SYNC Input Current	$V_{EN/SYNC}$=2V	-	2	-	uA
	EN/SYNC Input High Level	for SYNC Function	1.8	-	-	V
	EN/SYNC Input Low Level	for SYNC Function	-	-	0.25	V
OSCILLATOR AND SYNCHRONIZATION FREQUENCY (for CH1, CH2 and CH3)						
F_{OSC}	Oscillator Frequency		-	2.1	-	MHz
	Frequency Accuracy		-20	-	+20	%
	Minimum on Time	For CH2	-	-	53	ns
		For CH1/3	-	-	60	ns
	Maximum Duty		-	80	-	%
F_{SYNC}	SYNC Frequency Range		1.8	-	2.4	MHz

Note 4: Internal use only.

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN=12V, $V_{EN/SYNC}$=5V. Typical values are at T_J=25°C.

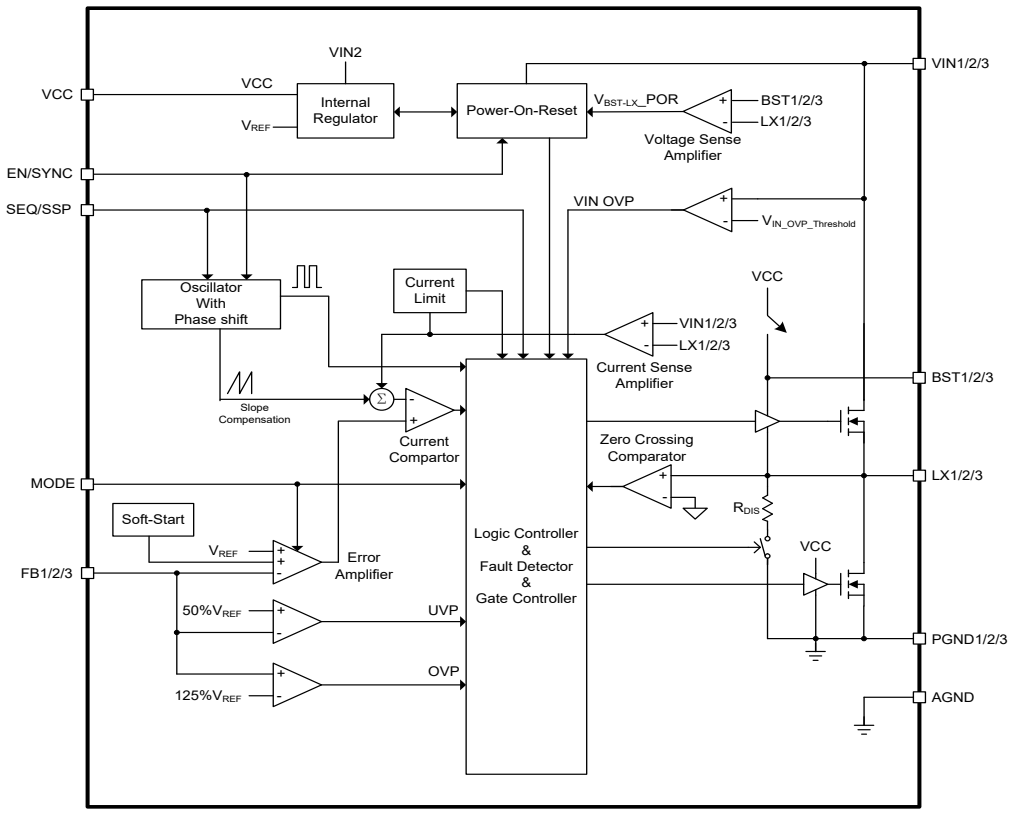
Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
POWER MOSFET (for CH1, CH2 and CH3)						
	CH1 High Side MOSFET Resistance		-	60	-	mΩ
	CH1 Low Side MOSFET Resistance		-	45	-	mΩ
	CH2 High Side MOSFET Resistance		-	90	-	mΩ
	CH2 Low Side MOSFET Resistance		-	50	-	mΩ
	CH3 High Side MOSFET Resistance		-	90	-	mΩ
	CH3 Low Side MOSFET Resistance		-	50	-	mΩ
	High Side MOSFET Leakage Current	$V_{EN/SYNC}$=0V, V_{LX}=AGND	-	1	-	μA
	Low Side MOSFET Leakage Current	$V_{EN/SYNC}$=0V, V_{LX}=VIN	-	1	-	μA
BOOTSTRAP POWER (for CH1, CH2 and CH3)						
R_{BST}	BST Switch On Resistance		-	10	-	Ω
	BST Leakage Current		-	-	0.1	μA
SEQ/SSP & MODE PIN						
$I_{SEQ/SSP}$	SEQ/SSP Leakage Current		-	-	0.1	uA
I_{MODE}	MODE Leakage Current		-	-	0.1	uA
PROTECTIONS (for CH1, CH2 and CH3)						
I_{LIM}	High Side MOSFET current-limit	For CH1	-	5	-	A
		For CH2	-	4	-	
		For CH3	-	2.5	-	
	Over-temperature Trip Point	(Note 5)	-	160	-	°C
	Over-temperature Hysteresis	(Note 5)	-	20	-	°C
	FB Over Voltage Protection		120	125	130	$\%V_{REF}$
	FB Over Voltage Protection Hysteresis		-	7	-	$\%V_{REF}$
	Under Voltage Protection		-	50	-	$\%V_{REF}$
	VIN Over Voltage Protection		-	20	-	V

Note 5: Guarantee by design.

Pin Description

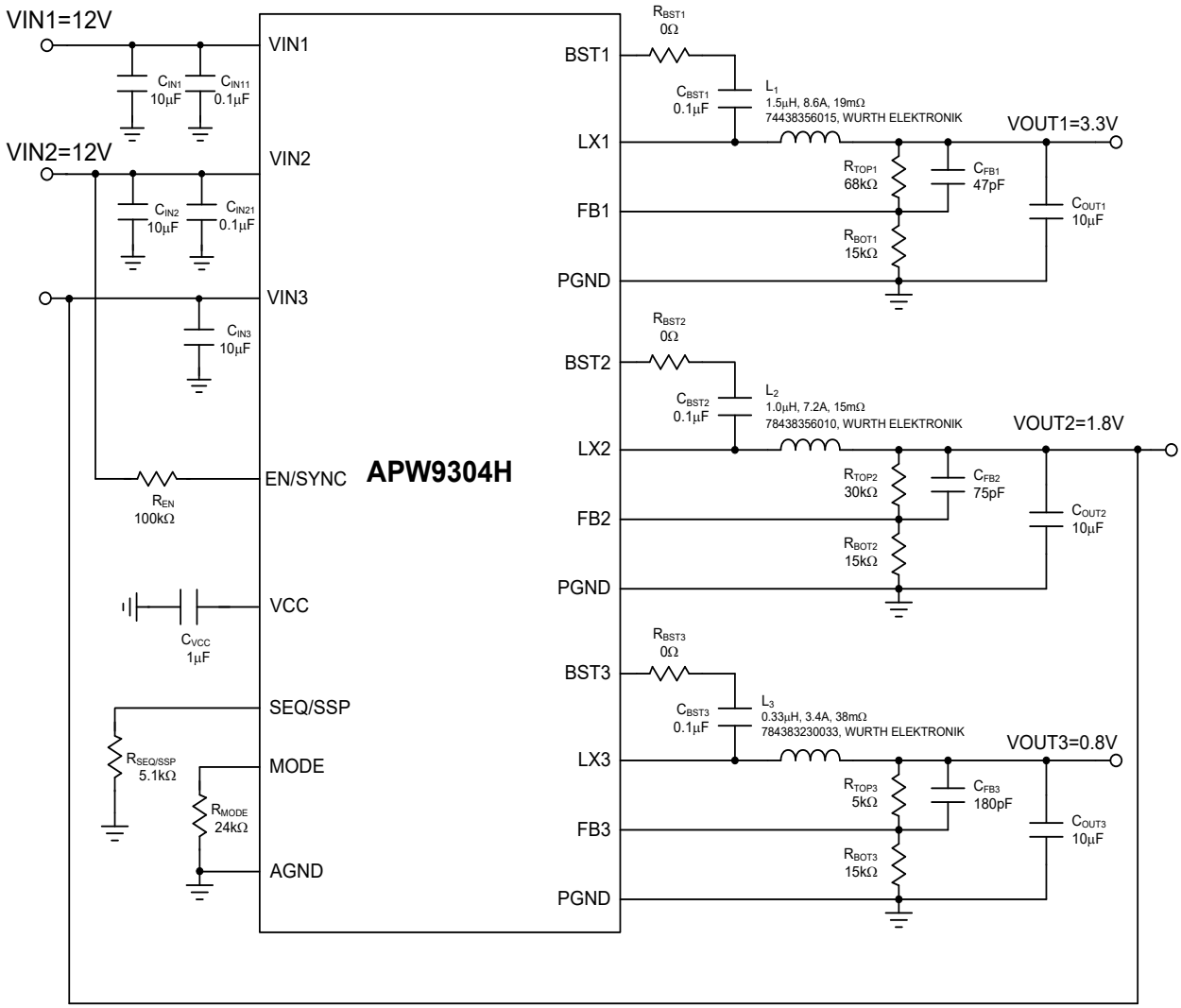
PIN		FUNCTION
NO.	NAME	
1	VIN3	CH3 Power Input Pin. VIN3 supplies the power to the CH3 buck converter.
2	FB3	CH3 Output Feedback Pin. FB3 senses the output voltage of channel3 and regulates it. Connect the resistor divider from the output through FB3 to the ground to set the output voltage.
3	MODE	Mode Pin. Connect a resistor from MODE to ground to set difference mode. If this pin connects a 5.1k ohm resistor, the IC will operate in Low Cost Auto-mode. If this pin connects a 12k ohm resistor, the IC will operate in High Performance Auto-mode. If this pin connects a 24k ohm resistor, the IC will operate in Low Cost FPWM. If this pin connects a 47k ohm resistor, the IC will operate in High Performance FPWM mode.
4	FB2	CH2 Output Feedback Pin. FB2 senses the output voltage of channel2 and regulates it. Connect the resistor divider from the output through FB2 to the ground to set the output voltage.
5	VIN2	CH2 Power Input Pin. VIN2 supplies the power to the CH2 buck converter.
6	BST2	CH2 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX2 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
7	LX2	CH2 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
8	PGND2	CH2 Power Ground. These pins must be connected directly to the GND plane of the PCB using low inductance vias.
9	VCC	Internal Regulator Output Pin. The VCC pin is the output of an internal 5V regulator for internal control circuitry. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
10	AGND	The Ground of IC.
11	EN/SYNC	Enable/Synchronous Clock Input Pin. Drive EN/SYNC high to turn all converters on and drive EN/SYNC low to turn them off. And input an external clock signal to this pin for synchronization function.
12	FB1	CH1 Output Feedback Pin. FB1 senses the output voltage of channel1 and regulates it. Connect the resistor divider from the output through FB1 to the ground to set the output voltage.
13	PGND1	CH1 Power Ground. These pins must be connected directly to the GND plane of the PCB using low inductance vias.
14	LX1	CH1 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
15	BST1	CH1 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX1 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
16	VIN1	CH1 Power Input Pin. VIN1 supplies the power to the CH1 buck converter.
17	SEQ/SSP	Power sequence and Spread-spectrum Pin. Connect a resistor from SEQ/SSP to ground to set difference power sequence mode. If this pin connects a 5.1k ohm resistor, the Power sequence is CH2 -> CH1 -> CH3 without Spread-spectrum. If this pin connects a 12k ohm resistor, the Power sequence is CH2 -> CH3 -> CH1 without Spread-spectrum. If this pin connects a 24k ohm resistor, the Power sequence is CH2 -> CH1 -> CH3 with Spread-spectrum. If this pin connects a 47k ohm resistor, the Power sequence is CH2 -> CH3 -> CH1 with Spread-spectrum.
18	PGND3	CH3 Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
19	LX3	CH3 Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
20	BST3	CH3 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX3 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
-	GND	The GND connect to PGND1, PGND2 and PGND3.

Block Diagram



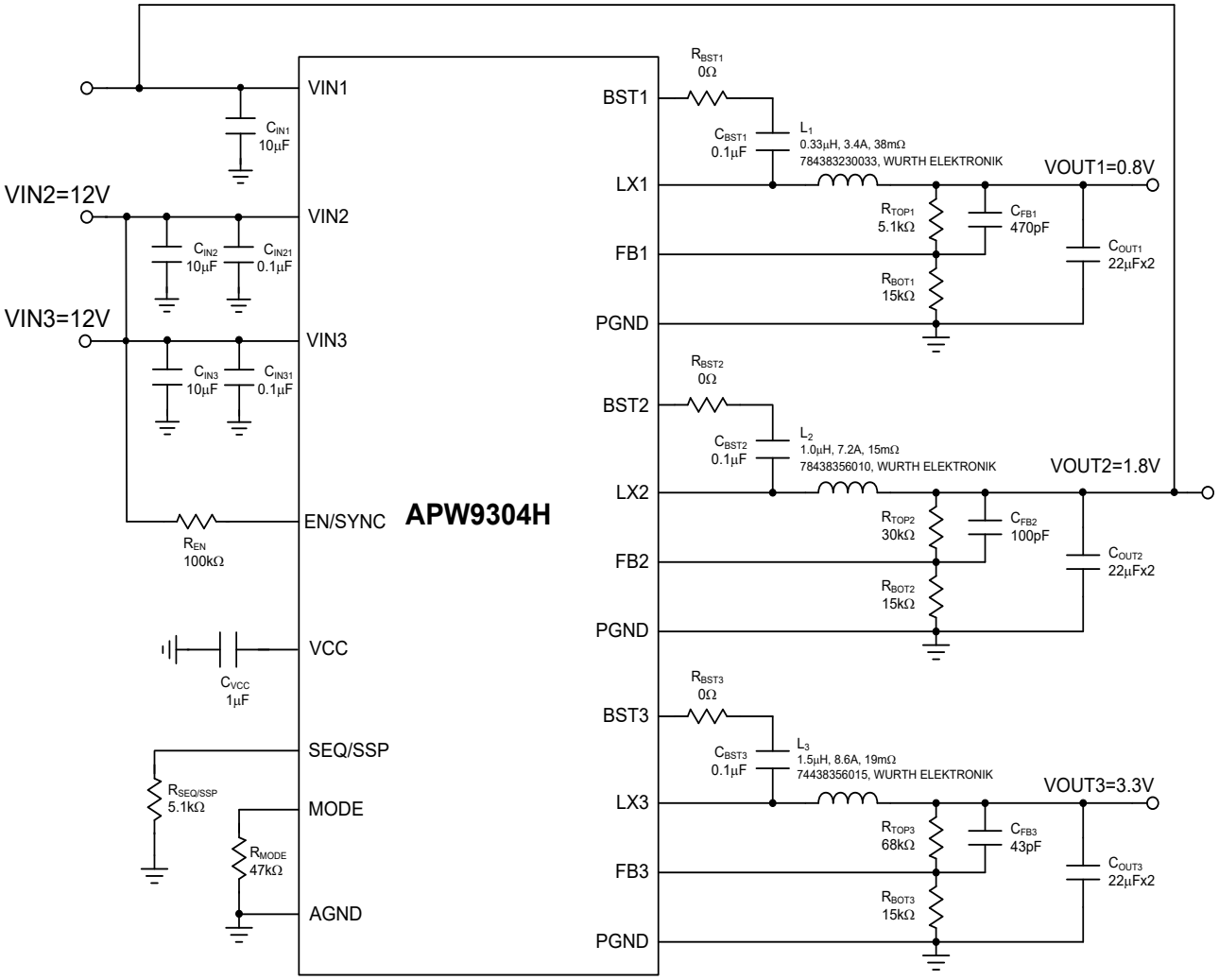
Typical Application Circuit

1. Low Cost BOM + FPWM



Typical Application Circuit (Cont.)

2. High Performance BOM + FPWM



Components Selection for Different Output Voltage

Application	Channel	VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)	R_{MODE} (Ω)	$R_{SEQ/SSP}$ (Ω)
1	1	12	3.3	0 ~ 3	10μ	1.5μ	10μ	68k	15k	47p	24k	5.1k
	2	12	1.8	0 ~ 2.5	10μ	1.0μ	10μ	30k	15k	75p		
	3	1.8	0.8	0 ~ 1.5	10μ	0.33μ	10μ	5.1k	15k	180p		
2	1	1.8	0.8	0 ~ 3	10μ	0.33μ	22μ × 2	5.1k	15k	470p	47k	5.1k
	2	12	1.8	0 ~ 2.5	10μ	1.0μ	22μ × 2	30k	15k	100p		
	3	12	3.3	0 ~ 1.5	10μ	1.5μ	22μ × 2	68k	15k	43p		

Components Selection for Different Operation mode

R_{MODE} (Ω)	Operation mode	C_{OUT} (F)	NOTE
5.1k	Auto-mode	10μ	Low Cost Auto-mode
12k	Auto-mode	22μ × 2	High Performance Auto-mode
24k	FPWM	10μ	Low Cost FPWM
47k	FPWM	22μ × 2	High Performance FPWM

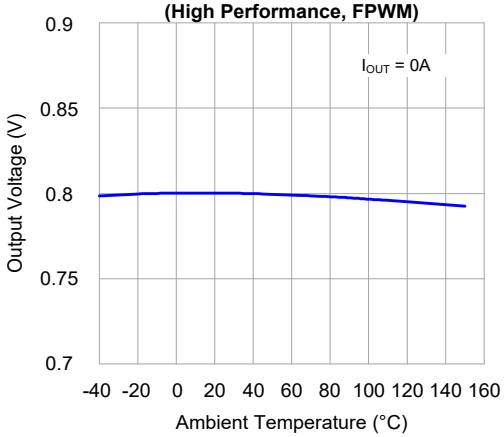
Components Selection for Spread-spectrum Function and Power sequence

$R_{SEQ/SSP}$ (Ω)	Spread-spectrum Function	Power sequence
5.1k	X	CH2 -> CH1 -> CH3
12k	X	CH2 -> CH3 -> CH1
24k	O	CH2 -> CH1 -> CH3
47k	O	CH2 -> CH3 -> CH1

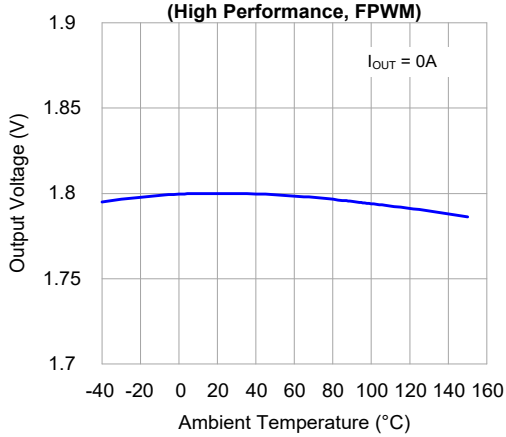
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

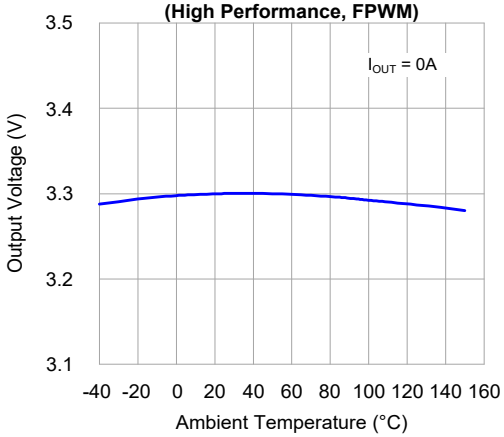
CH1 Output Voltage vs. T_A (High Performance, FPWM)



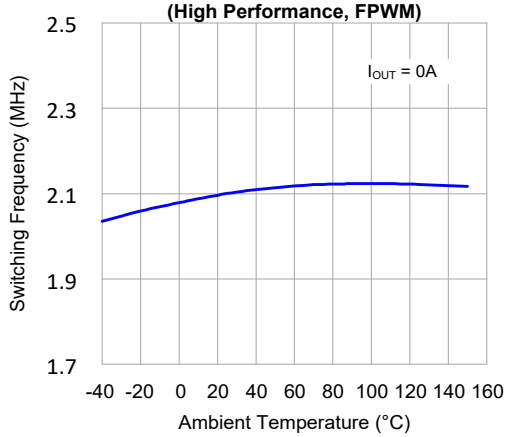
CH2 Output Voltage vs. T_A (High Performance, FPWM)



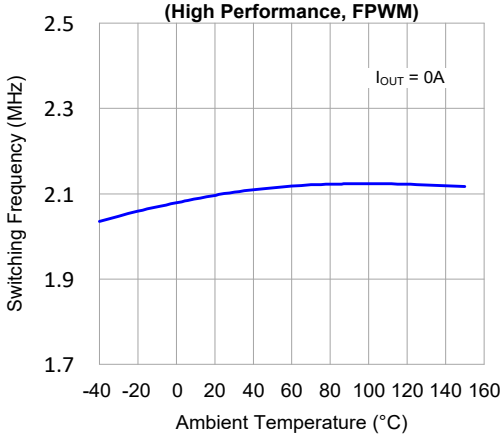
CH3 Output Voltage vs. T_A (High Performance, FPWM)



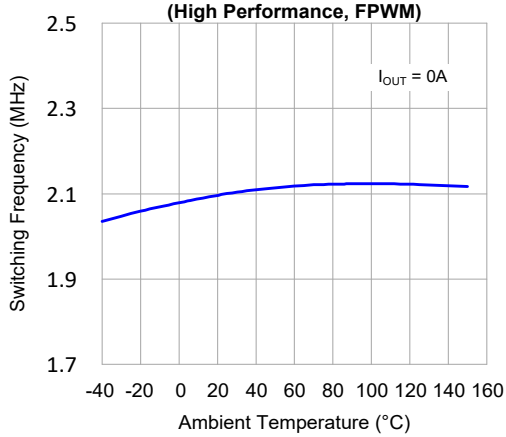
CH1 Switching Frequency vs. T_A (High Performance, FPWM)



CH2 Switching Frequency vs. T_A (High Performance, FPWM)



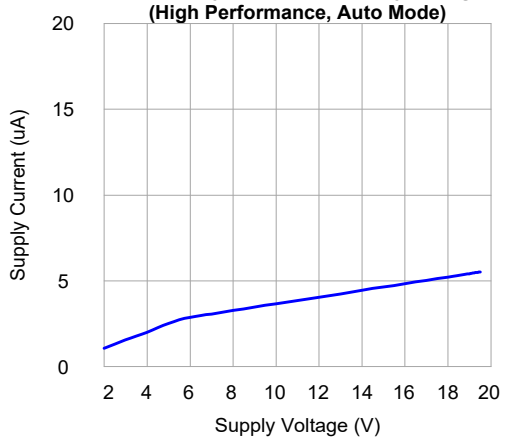
CH3 Switching Frequency vs. T_A (High Performance, FPWM)



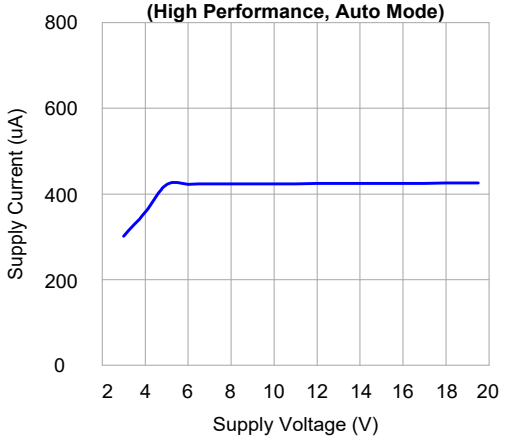
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

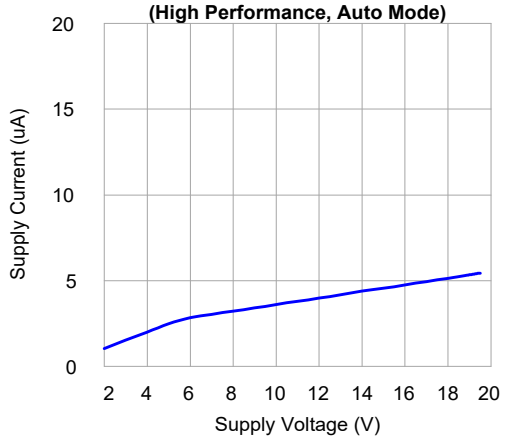
CH1 Supply Current vs. Supply Voltage (High Performance, Auto Mode)



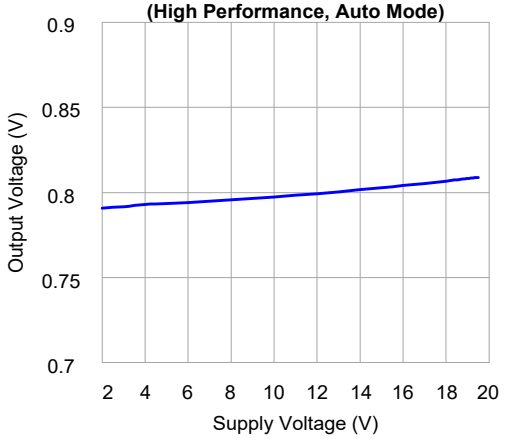
CH2 Supply Current vs. Supply Voltage (High Performance, Auto Mode)



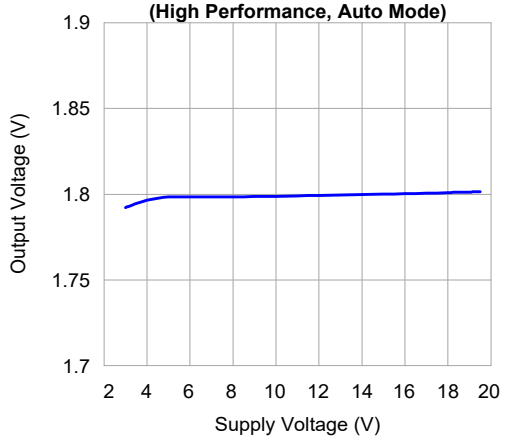
CH3 Supply Current vs. Supply Voltage (High Performance, Auto Mode)



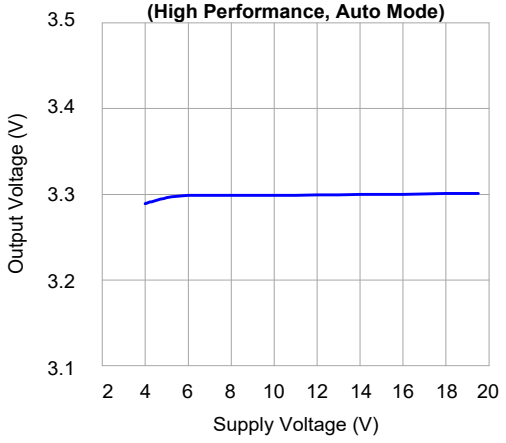
CH1 Output Voltage vs. Supply Voltage (High Performance, Auto Mode)



CH2 Output Voltage vs. Supply Voltage (High Performance, Auto Mode)



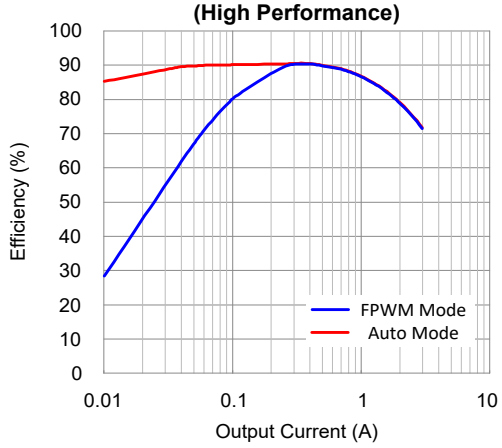
CH3 Output Voltage vs. Supply Voltage (High Performance, Auto Mode)



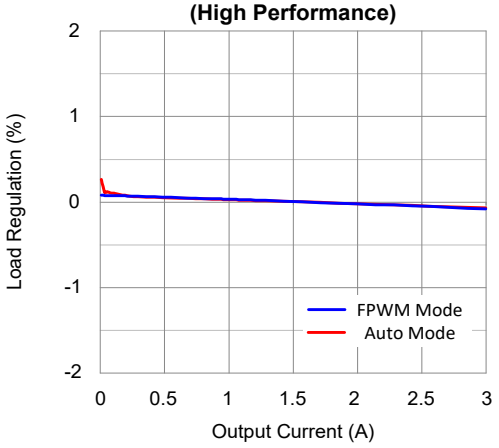
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

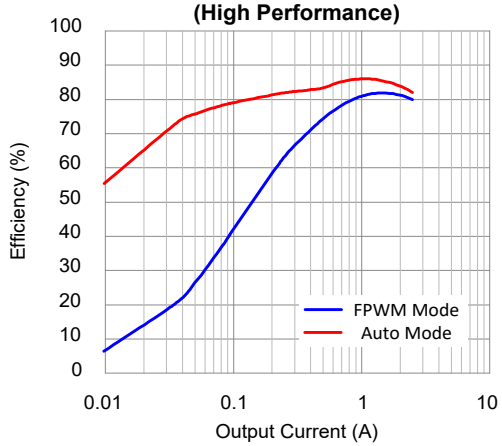
CH1 Efficiency vs. Output Current (High Performance)



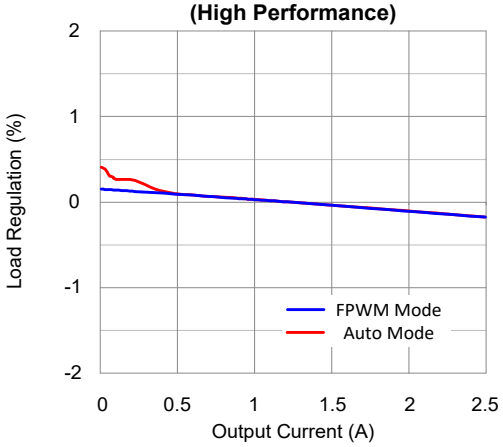
CH1 Regulation vs. Output Current (High Performance)



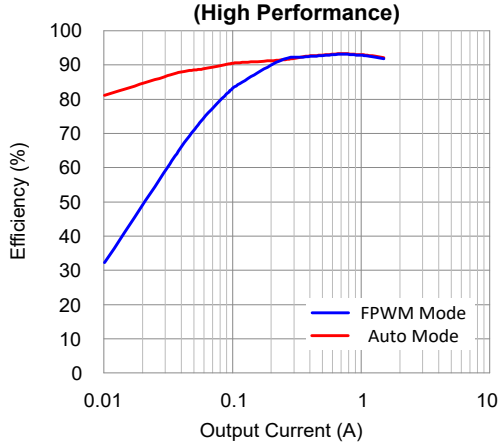
CH2 Efficiency vs. Output Current (High Performance)



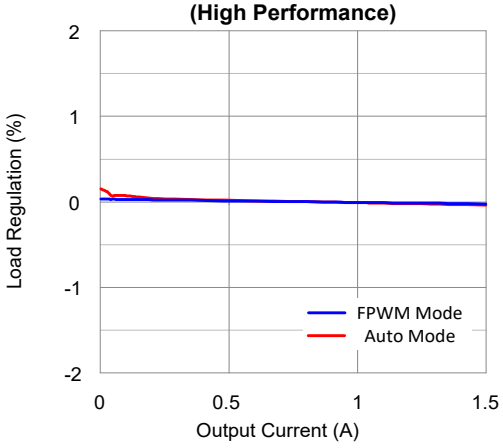
CH2 Regulation vs. Output Current (High Performance)



CH3 Efficiency vs. Output Current (High Performance)



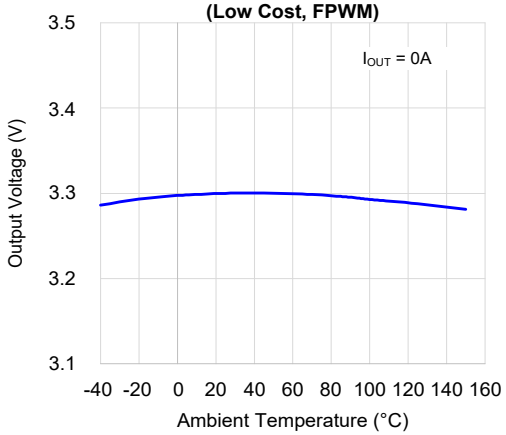
CH3 Regulation vs. Output Current (High Performance)



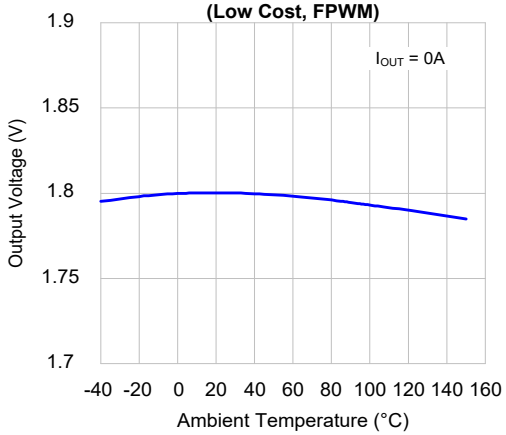
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

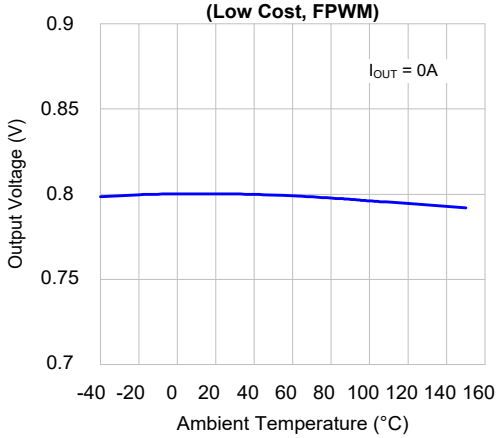
CH1 Output Voltage vs. T_A (Low Cost, FPWM)



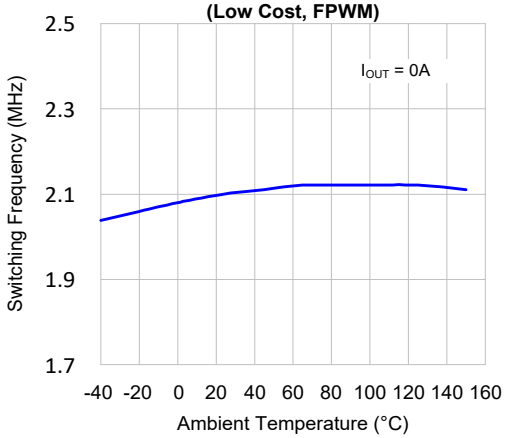
CH2 Output Voltage vs. T_A (Low Cost, FPWM)



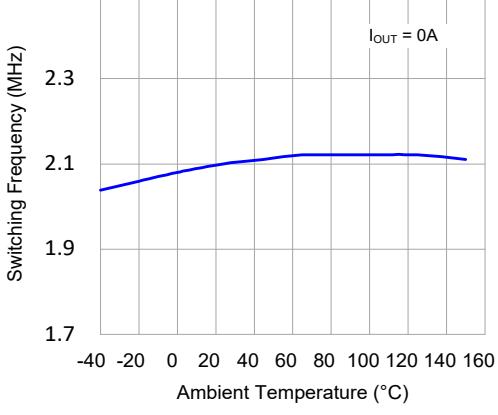
CH3 Output Voltage vs. T_A (Low Cost, FPWM)



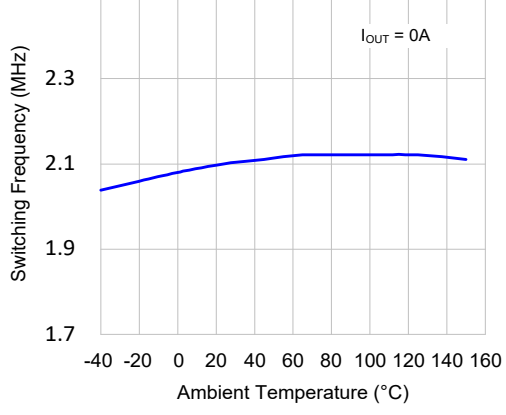
CH1 Switching Frequency vs. T_A (Low Cost, FPWM)



CH2 Switching Frequency vs. T_A (Low Cost, FPWM)



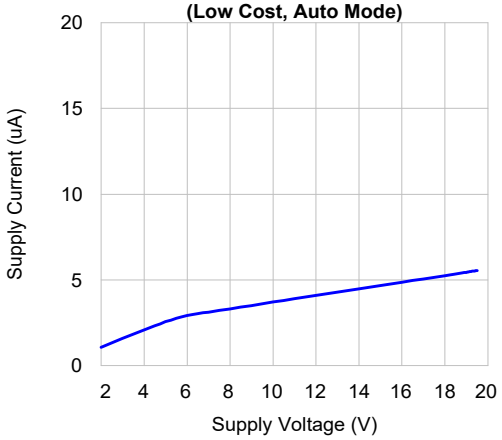
CH3 Switching Frequency vs. T_A (Low Cost, FPWM)



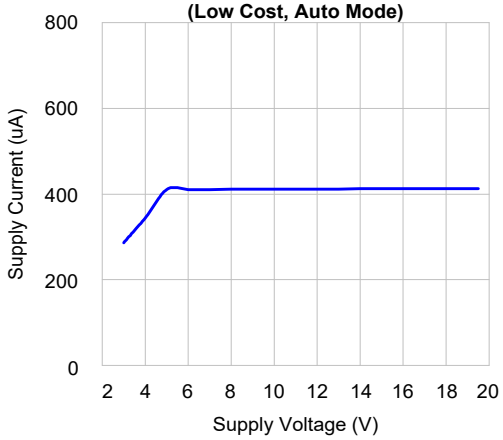
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

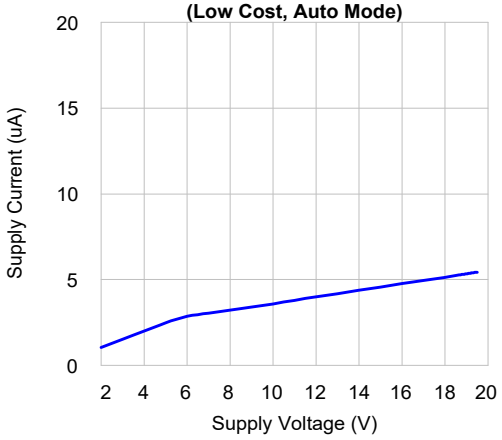
CH1 Supply Current vs. Supply Voltage (Low Cost, Auto Mode)



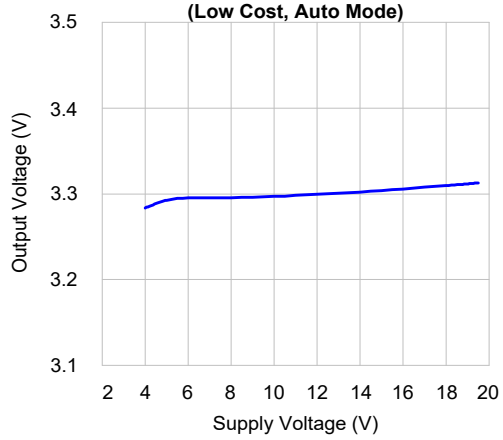
CH2 Supply Current vs. Supply Voltage (Low Cost, Auto Mode)



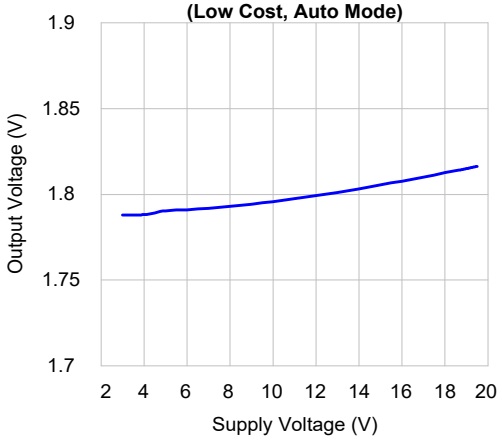
CH3 Supply Current vs. Supply Voltage (Low Cost, Auto Mode)



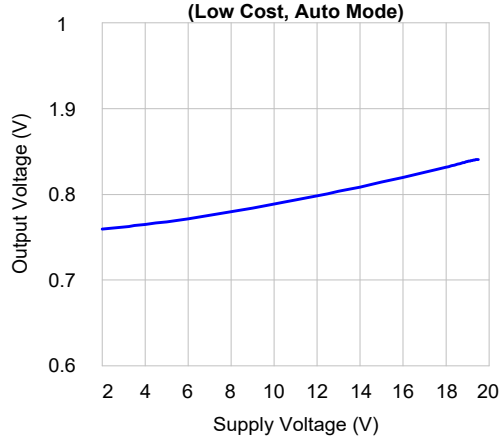
CH1 Output Voltage vs. Supply Voltage (Low Cost, Auto Mode)



CH2 Output Voltage vs. Supply Voltage (Low Cost, Auto Mode)



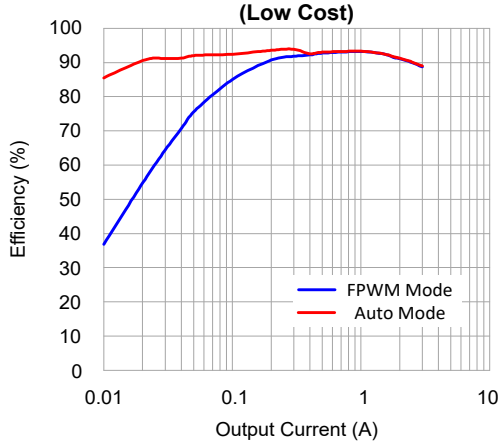
CH3 Output Voltage vs. Supply Voltage (Low Cost, Auto Mode)



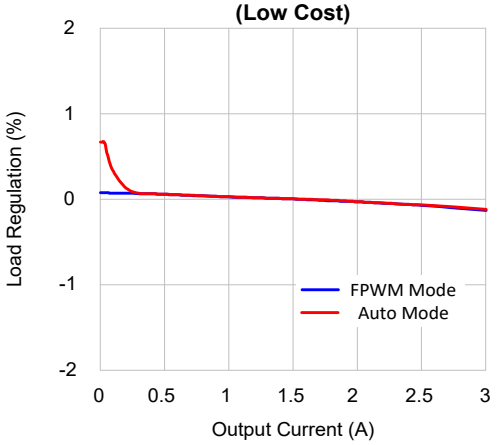
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

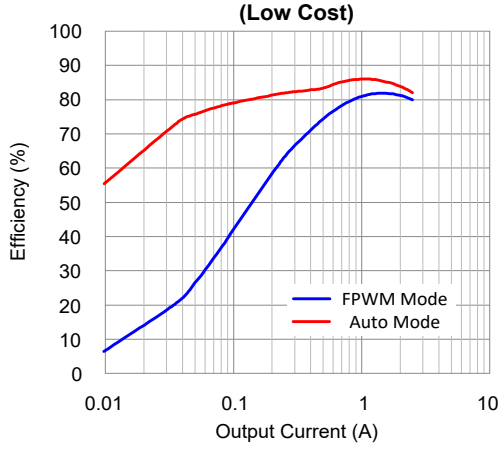
CH1 Efficiency vs. Output Current (Low Cost)



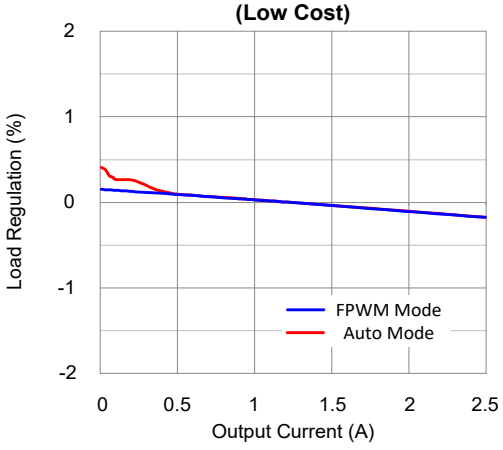
CH1 Regulation vs. Output Current (Low Cost)



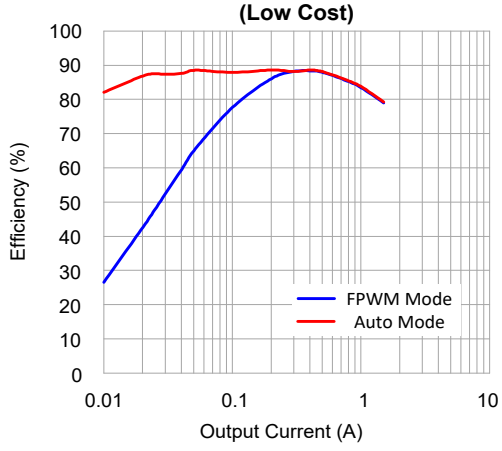
CH2 Efficiency vs. Output Current (Low Cost)



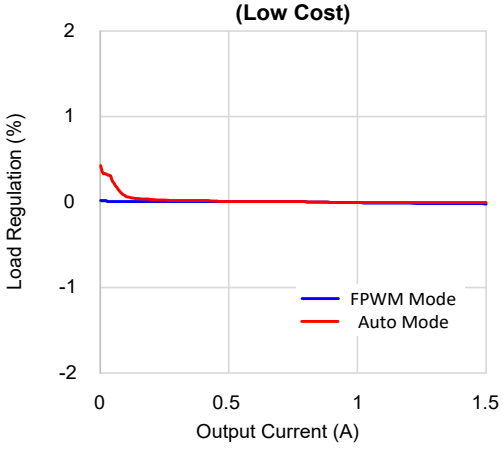
CH2 Regulation vs. Output Current (Low Cost)



CH3 Efficiency vs. Output Current (Low Cost)



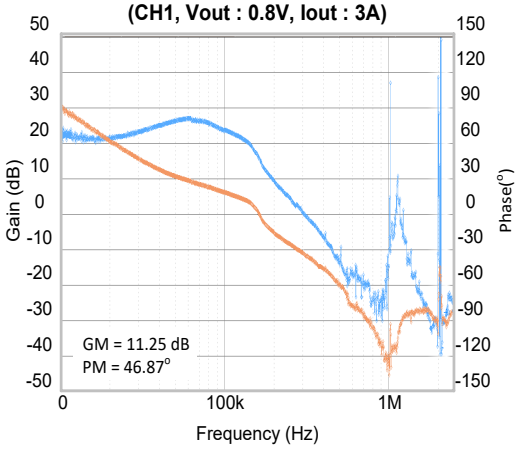
CH3 Regulation vs. Output Current (Low Cost)



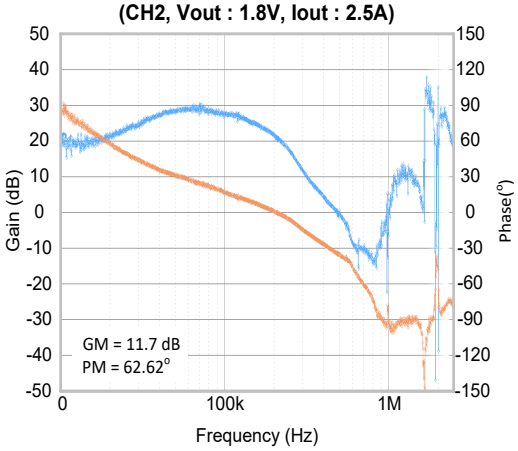
Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

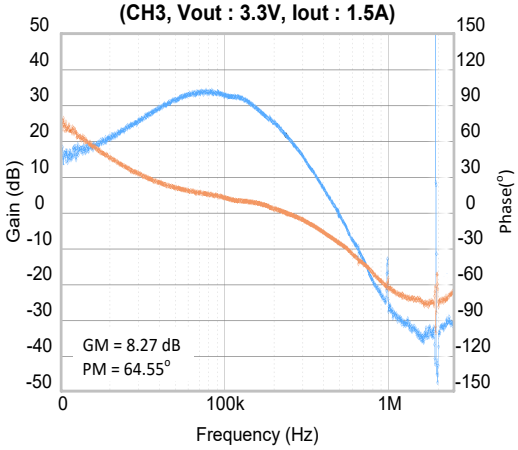
High Performance Bode Plot
(CH1, Vout : 0.8V, Iout : 3A)



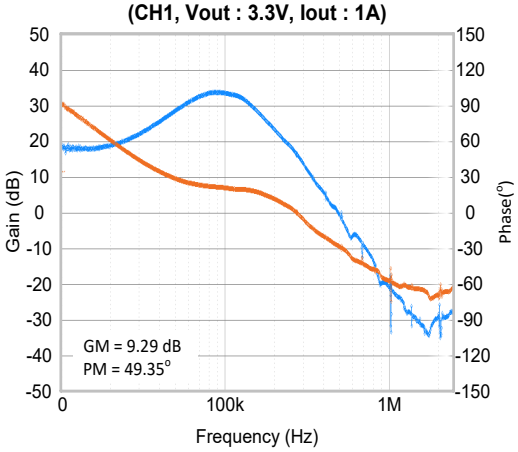
High Performance Bode Plot
(CH2, Vout : 1.8V, Iout : 2.5A)



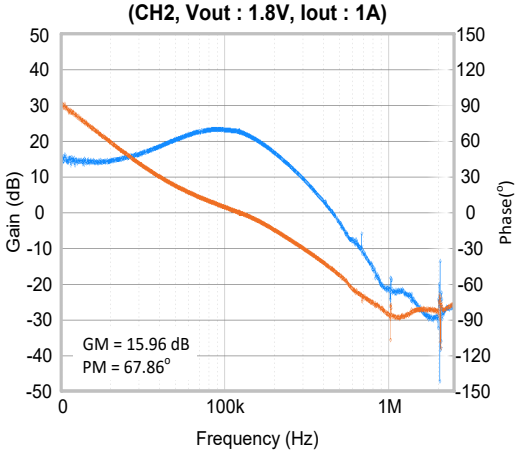
High Performance Bode Plot
(CH3, Vout : 3.3V, Iout : 1.5A)



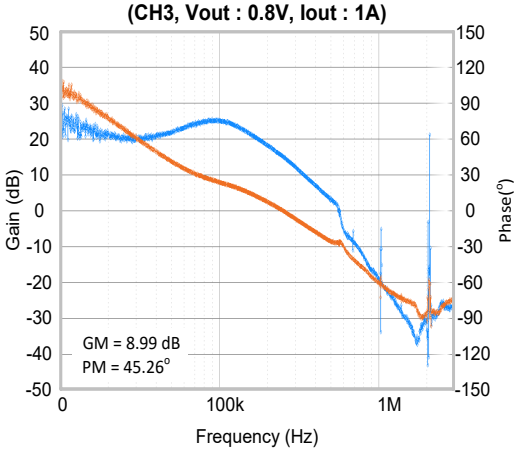
Low Cost Bode Plot
(CH1, Vout : 3.3V, Iout : 1A)



Low Cost Bode Plot
(CH2, Vout : 1.8V, Iout : 1A)



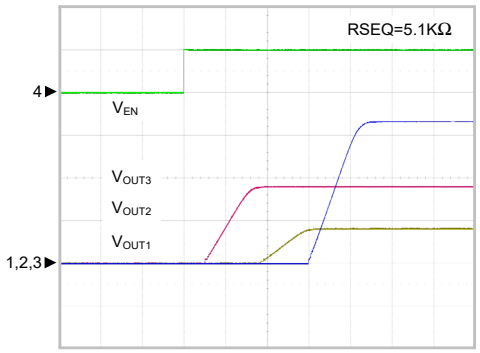
Low Cost Bode Plot
(CH3, Vout : 0.8V, Iout : 1A)



Operating Waveforms (Cont.)

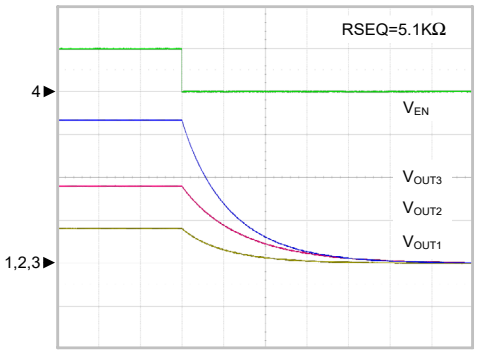
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On Sequence (High Performance)



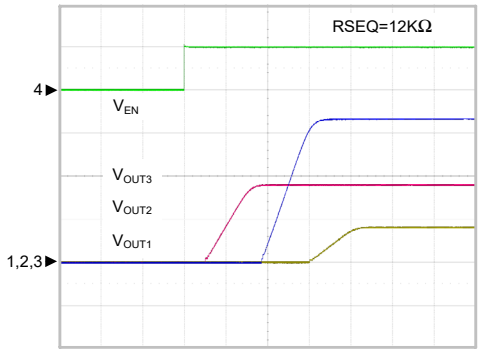
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 1ms/Div

Power Off Sequence (High Performance)



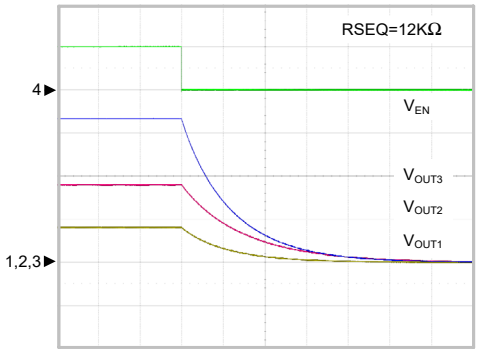
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 5ms/Div

Power On Sequence (High Performance)



CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 1ms/Div

Power Off Sequence (High Performance)

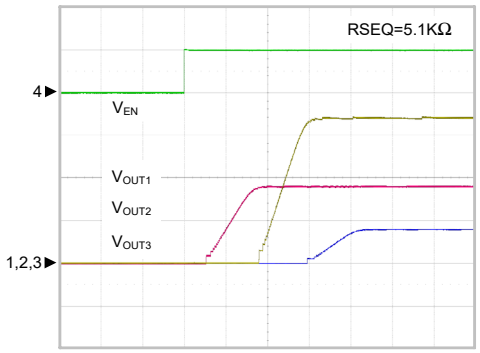


CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 5ms/Div

Operating Waveforms (Cont.)

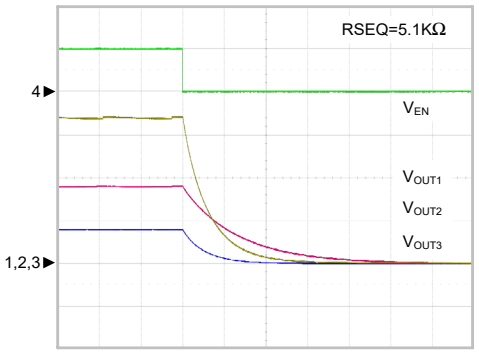
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On Sequence (Low Cost)



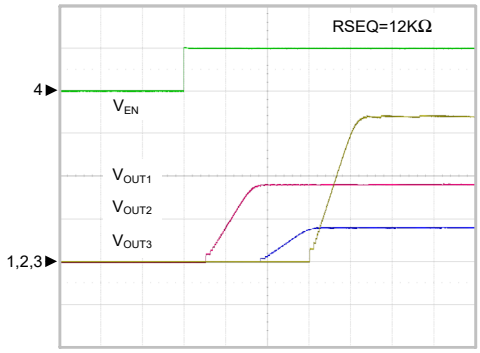
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 1ms/Div

Power Off Sequence (Low Cost)



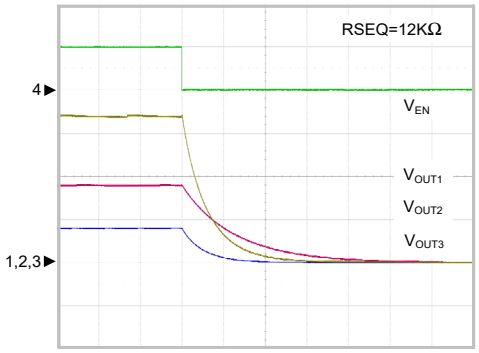
CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 2ms/Div

Power On Sequence (Low Cost)



CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 1ms/Div

Power Off Sequence (Low Cost)



CH1: V_{OUT1}, 1V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{OUT3}, 1V/Div, DC
CH4: V_{EN}, 5V/Div, DC
TIME: 2ms/Div

Function Description

Main Control Loop

The IC uses current mode control to regulate the output voltage.
The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier.
The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage.
The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Under Voltage Lock Out

The IC continuously monitors the voltage on the VIN pin.
The IC provides three $V_{UVLO1/2/3}$ high/low threshold voltage controls (V_{UVLO1} and V_{UVLO2} and V_{UVLO3}) for the three converters (CH1 and CH2 and CH3).
The CH1 or CH3 soft start is activated, when the VIN1 voltage is higher than the V_{UVLO1} threshold and the VIN3 voltage is higher than the V_{UVLO3} threshold. The CH2 soft start is activated, when the VIN2 voltage is higher than the V_{UVLO2} threshold.
If VIN1 or VIN3 is below than their respective $V_{UVLO1/3}$ low threshold voltage, the CH1 and CH3 converter are turned off at the same time.
When VIN2 is below the V_{UVLO2} low threshold voltage, the IC is turned off and the output discharge is triggered.
$V_{UVLO1/2/3}$ is used to protect the IC from erroneous operation with insufficient VIN voltage. $V_{UVLO1/2/3}$ also has hysteresis to resist ripple on the VIN voltage.

VCC Power-On-Reset (POR)

VCC is an internal voltage regulator that is activated when the IC is powered by V_{UVLO2} and $V_{EN/SYNC}$ goes high. The IC continuously monitors the voltage on the VCC pin. The soft start is activated, when the VCC voltage is higher than the POR threshold and the VIN2 voltage is higher than the V_{UVLO2} threshold and the $V_{EN/SYNC}$ voltage is higher than the enable threshold.
When $V_{EN/SYNC}$ is below than the EN/SYNC low threshold voltage, the VCC will go low and the IC is turned off.
VCC POR is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC POR also has hysteresis to resist ripple on the VCC voltage.

Enable/Shutdown and Frequency synchronization

The IC provides the EN/SYNC pin, which is a digital input that turns the converter on or off. Drive EN/SYNC high to turn the converter on and drive it low to turn it off. To synchronize the internal operating frequency of the IC with the external clock, connect the EN/SYNC pin to an external 50% duty cycle clock. The rising edge of the internal clock is synchronized with the rising edge of the external clock.

Single Frequency and Phase shift

The IC has three converters that use the same operating frequency to avoid beat frequencies and improve noise immunity.
But it also increases input current and EMI, so more input capacitors and additional EMI components must be used. Therefore, the IC provides a 120-degree phase shifting technique that allows three high-side power MOSFETs to be turned on at different times to eliminate these defects. It will greatly reduce the RMS input current, resulting in less input capacitance, EMI components and input losses.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN/SYNC pin, and when the converter is restarted from the OTP and hiccup mode.

VIN Over-Voltage Protection (VIN OVP)

The IC monitors the input voltage to implement the VIN OVP function. When the input voltage exceeds the VIN_OVP_Threshold voltage, VIN OVP will be triggered and the IC will be turned off until the V_{IN} voltage is lower than the VIN OVP low threshold voltage. At this time, the VIN OVP will be disabled and the IC will resume normal operation.

Over-Voltage Protection (OVP)

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Current Limit and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode. In hiccup mode, the converter will restart periodically.
This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over-current condition is removed, the IC will exit the hiccup mode.

Function Description (Cont.)

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature.
The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Power Derating Curve

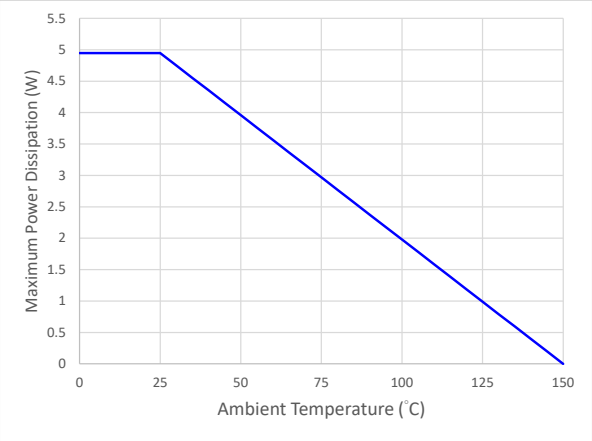
The power derating curve can let designer the maximum power dissipation versus ambient temperature that the converter can dissipate under the maximum junction temperature $T_{J(MAX)}$. The maximum power dissipation can be calculated by equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

The maximum junction temperature $T_{J(MAX)}$ is 150°C, $\theta_{JA}$of the TQFN 4x4-20D wettable flanks package is 25.261 °C/W. Therefore, the maximum power dissipation of APW9304H at TA = 25°C is:

$$P_{D(MAX)} = (150°C – 25°C) / (25.261°C/W) = 4.95W$$

The power derating curve with different ambient temperature is shown below:



Fast Discharge

When the EN/SYNC signal goes low or the VIN1 voltage falls below the V_{UVLO1} threshold or the VIN3 voltage falls below the V_{UVLO3} threshold, the CH1 and CH3 converter are turned off and the CH1and CH3 output fast discharge are triggered.
When the EN/SYNC signal goes low or the VIN2 voltage falls below the V_{UVLO2} threshold, the IC is turned off and the CH1/CH2/CH3 output fast discharge is triggered.
The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to “Typical Application Circuit”. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Application Information (Cont.)

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/PGND to capacitor less than 2mm respectively is recommended.

2. Place the VCC capacitor to VCC pin and AGND pin as close as possible.

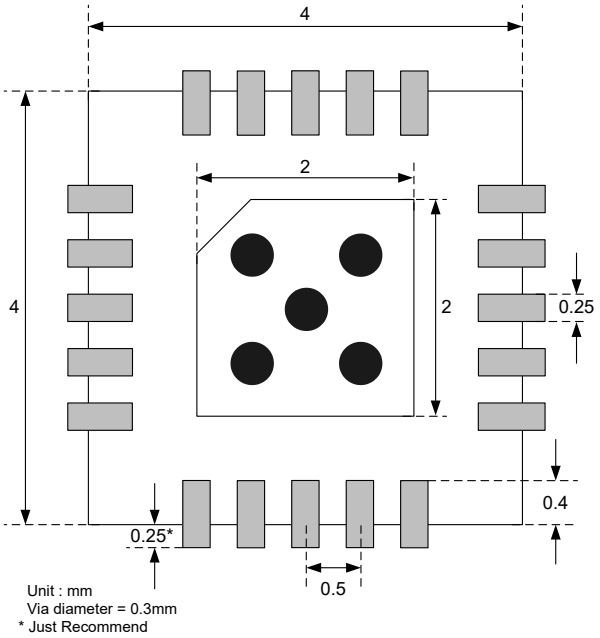
3. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.

4. The output capacitor's ground should be close to the grounds of the input capacitor.

5. Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces.

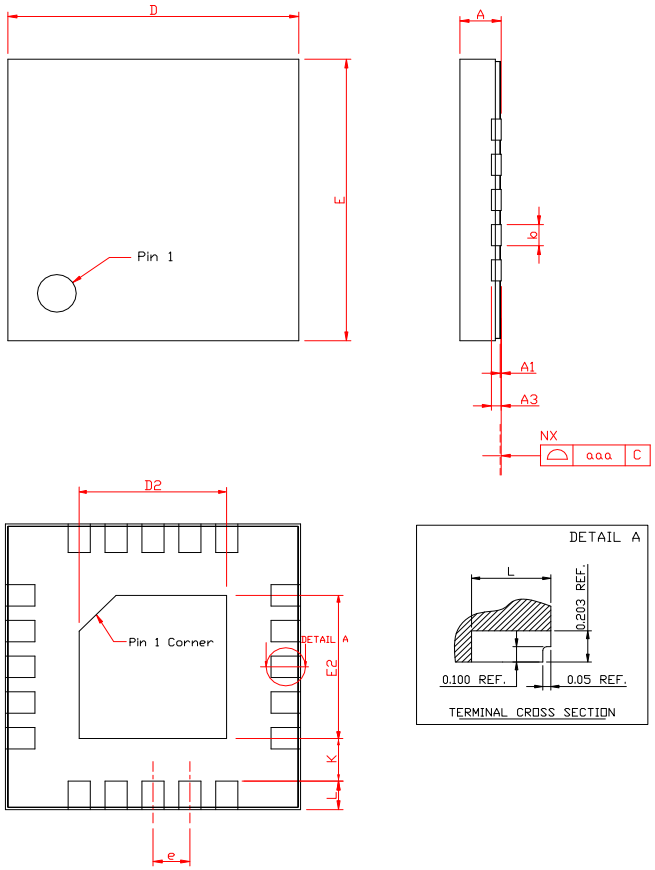
6. A star ground connection or ground plane minimizes ground shifts and noise is recommended. It is also highly recommend to have the same or larger size GND plan below thermal pad at all PCB layers.

Recommended Minimum Footprint (Top View)



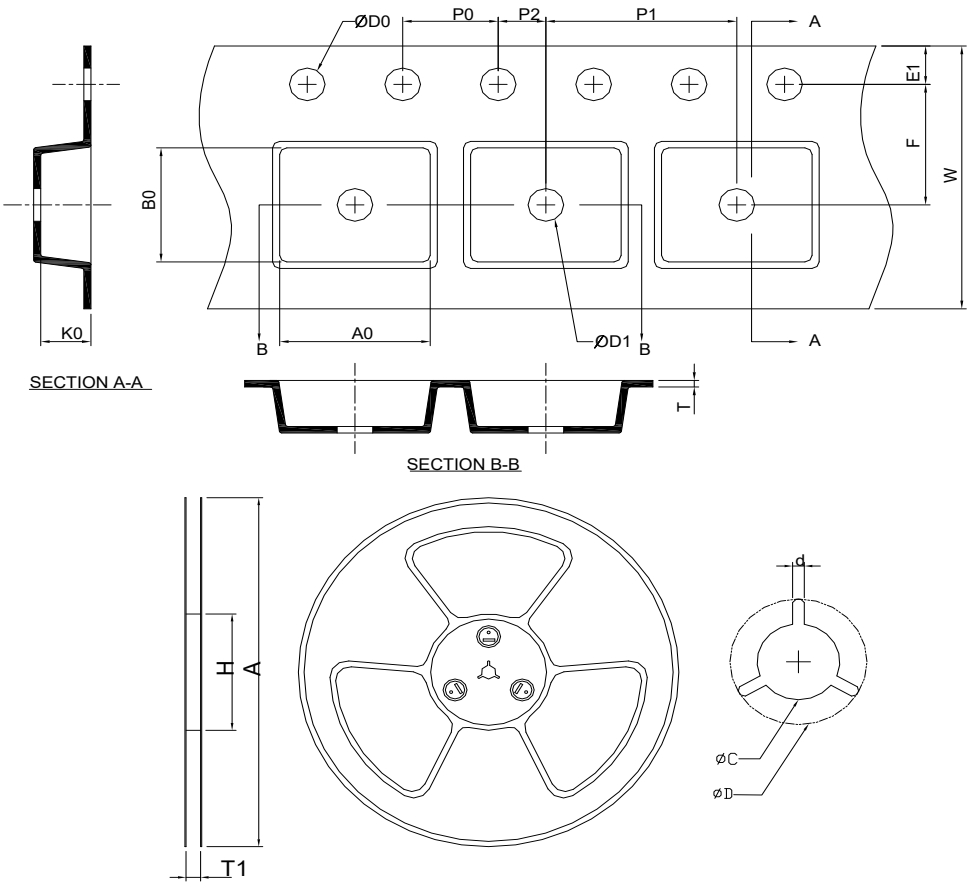
Package Information

TQFN4x4-20D



SYMBOL	TQFN4*4-20D			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	1.95	2.05	0.077	0.081
E	3.90	4.10	0.154	0.161
E2	1.95	2.05	0.077	0.081
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

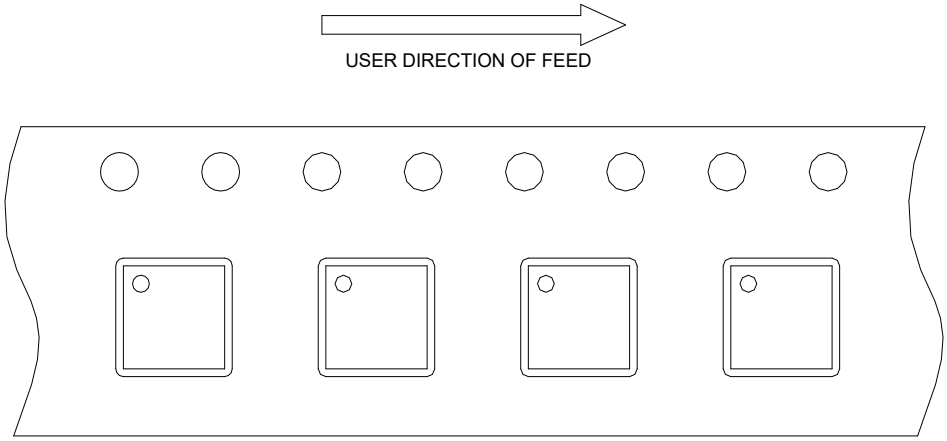
(mm)

Devices Per Unit

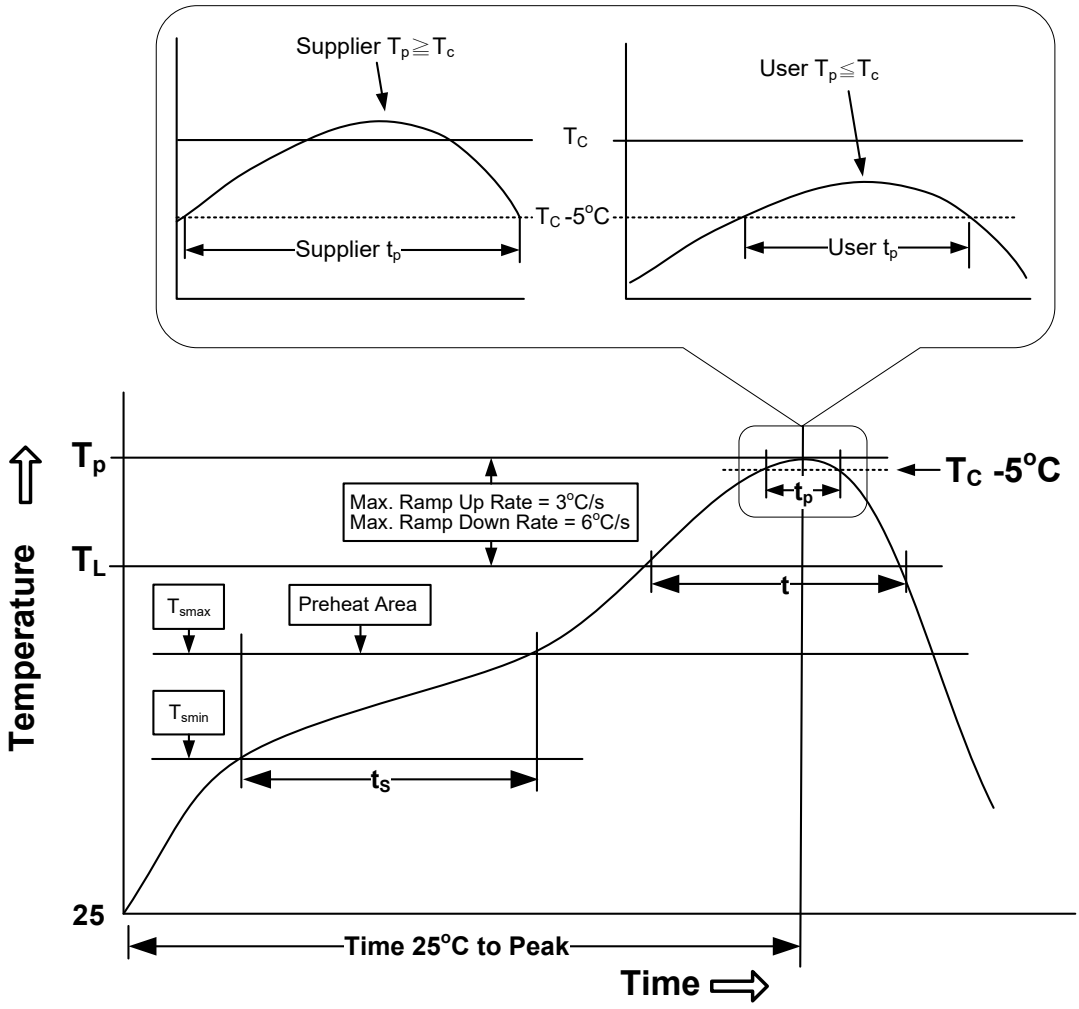
Package type	Packing	Quantity
TQFN 4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-20D



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100°C 150°C 60-120 seconds	150°C 200°C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Note: ANPEC's green products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235°C	220°C
≥2.5 mm	220°C	220°C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
≥2.5 mm	250°C	245°C	245°C

AEC-Q100 Reliability Test Program

No.	Stress	Abv.	Ref. No	Test Method	Conditions
A	Moisture Sensitivity Level Test	MSL	A1	JESD22-A113	30°C/ 60%RH, 192H
B	Highly Accelerated Temperature and Humidity Stress Test	HAST	A2	JESD22-A110	130°C, 85%RH, 96H
C	Unbiased Highly Accelerated Temperature and Humidity Stress Test	UHST	A3	JESD22-A118	130°C, 85%RH, 96H
D	Temperature Cycling Test	TCT	A4	JESD22-A104	-55°C~150°C, 1000 Cycles
E	Power Temperature Cycling	PTC	A5	JESD22-A105	-40°C~125°C, 1000 Cycles
F	High Temperature Storage Life Test	HTSL	A6	JESD22-A103	150°C, 1000H
G	High Temperature Operating Life Test	HTOL	B1	JESD22-A108	125°C, 1000H
H	Early Life Failure Rate Test	ELFR	B2	AEC-Q100-008	125°C, 48H
I	ESD	HBM	E2	AEC-Q100-002	≧ ± 2000V
		CDM	E3	AEC-Q100-011	≧ ± 500V
J	Latch-Up	LU	E4	AEC-Q100-004	≧ ± 100V

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